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A Novel approach to Layout Design of 2-bit Binary Ripple Carry Adder using CMOS NAND Gates

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ABSTRACT: A good deal of ingenuity can be exercised and a vast amount of time has been wasted for exploring layout topologies to minimize the size of a gate or other circuitry such as an construction of adder or memory element in an integrated circuit. This paper represents a simple and compact layout design for two bit binary parallel ripple carry adder using only CMOS NAND gates with the help of Microwind as a tool for design and simulation. Construction of this adder for fabricating involves the design of 2-input, 3-input, 4-input NAND gates and CMOS NAND inverters. The performance parameters for this design are analyzed from the simulation responses and characteristics curves of the proposed design. The optimization of the design towards single P+ or N+ diffusion, single +Vdd and single –Vdd supply contributed to lesser area and improved functionality of the adder circuits performance.

KEYWORDS: CMOS NAND inverter,2-input CMOS NAND gate,3-input CMOS NAND gate,4-input CMOS NAND gate,Final NAND ADDER.

I. INTRODUCTION

In the past few years a remarkable rise in VLSI fabrication has lead to increase.The densities of integrated circuits by decreasing the device geometries. Such high density circuits support high design complexities and very high speed but susceptible to power consumption. Circuits with excessive power dissipation are more susceptible to run time failures and give rise to reliability problems. The other factors behind low power design are growing class of hand-held devices, e.g., as portable desktops, digital pens, audio and video based multi-media products and wireless communication such as PDA's and smartcards etc. These devices and systems demand high speed and complex design functionalities. The performance of these devices is limited by size, weight and lifetime of portable batteries.

The need to integrate more functions within a given silicon area, reduce the fabrication cost, increase operating speed and dissipate less power, the trend of CMOS (Complementary Symmetry Metal Oxide Semiconductor) technology has been improved. Past few years have seen the introduction of nano-scale technologies for industrial production of high performance integrated circuits (IC).High noise immunity and low static power consumption are the two important characteristics of CMOS devices. Significant power is only drawn when the transistors in the CMOS device are switching between on and off states. Consequently, as some form of devices such as transistortransistor logic (TTL) or NMOS logic CMOS devices do not produce as much waste heat. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in VLSI chips.

Microwind is a CMOS circuit editor and simulation tool for logic and layout-level design, running on Microsoft Windows. It has been developed since 1998 through several versions, and is available as a freeware (lite version [6]) for educational purpose. In this paper, a 2-bit binary parallel adder based on CMOS NAND gate layout is designed using Microwind 3.1. First of all the individual components, the NAND inverter, 2-input, 3-input and 4-input NAND gates were designed, aligned and connected properly. The overall design diagram, 3D view of the layout and performance graphs are presented for a greater understanding.

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II. THEORY OF FULL ADDER

A full adder is a digital circuit that performs addition operation. These are implemented with logic gates in hardware. A full adder adds three one- binary numbers, two operands and a carry bit. The adder outputs two numbers, a sum and a carry bit. The term is contrasted with a half adder, whch adds two binary digits.Consider A_n,B_n and C_{n-1} these three bits.In this An and Bn are the nth order bits of the numbers A and B respectively and Cn-1 is the carry generated from the addition of (n-1)th order bits. Table 1 shows the truth table and figure 1 shows the logic diagram of a 1-bit full adder. Logical circuit using multiple full adders to add N-bit numbers can be created. Each full adder inputs a Cin, which is the Cout of the the previous adder. This kind of adder is a ripple carry adder, since each carry bit "ripples" to the next full adder.

Inputs			*Outputs*	
A_n	B_n	C_{n-1}	S_n	C_n
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 1: Truth table 1-bit full adder

SUM AND CARRY EQUATIONS OF FULL ADDER

$$\text{Sum, } S_n = H_K \cdot \overline{C_{k-1}} + \overline{H_k} \cdot C_{k-1}$$
$$\text{New Carry, } C_k = A_k \cdot B_k + H_k \cdot C_{k-1}$$
$$\text{Where, half sum, } H_k = \overline{A_k \oplus B_k}$$
$$= \overline{A_k} \cdot B_k + A_k \cdot \overline{B_k}$$

LOGIC DIAGRAM OF 1-BIT FULL ADDER

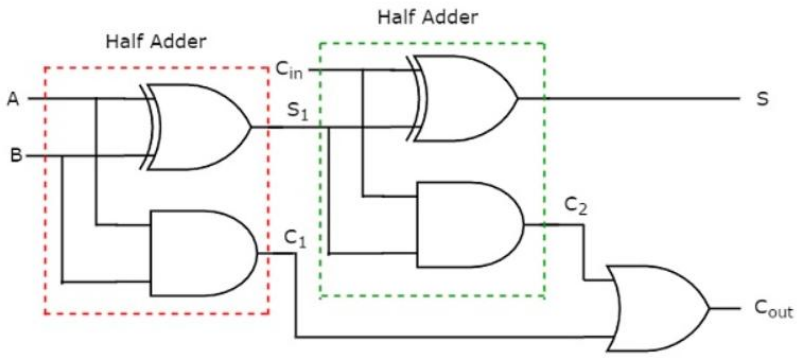

fig 1. Logic diagram of full adder

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The above figure is called full adder.For the implementation of full we require two half adder and one OR gate.If C_{in}=0 then full adder becomes half adder.But by this construction the requirement of area will be more which leads to more expensive.By performing k-maps on sum and carry functions , the sum and carry funtions in the terms of NAND function can be realized .So that construcion of full adder will be implemented using CMOS NAND gates which is less cost and require less area.

Table 2. K-map for S_n

C_{n-1} \ A_nB_n	00	01	11	10
0		1		1
1	1		1	

Table 3. K-map for C_n

C_{n-1} \ A_nB_n	00	01	11	10
0			1	
1		1	1	1

B_nC_{n-1} A_nC_{n-1}

The minimized Boolean Expression for Sn and Cn are

$$S_n = \overline{A}_n B_n \overline{C}_{n-1} + \overline{A}_n \overline{B}_n C_{n-1}$$

$$A_n \overline{B}_n \overline{C}_{n-1} + A_n B_n C_{n-1}$$

$$C_n = A_n B_n + B_n C_{n-1} + A_n C_{n-1}$$

By using these equations sum bit and carry bit can be illustrated as figure shown below

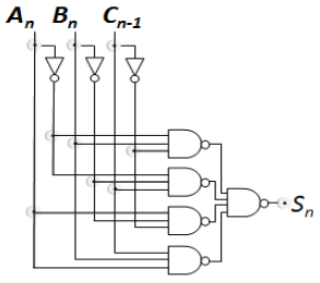

Fig 2. NAND realization of S_n

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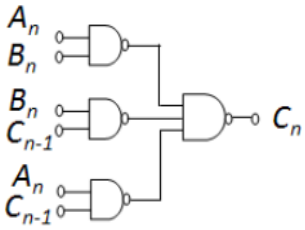

Fig 3.NAND realization of C_n

III.DESIGN OF ADDER

The design of a 2-bit binary parallel adder involved the design of CMOS NAND inverters, 2-input NAND gates, 3input NAND gates and 4-input NAND gates. Finally these components were arranged side by side and necessary interconnections were established to perform the specified logical operation.

REALIZATION OF CMOS NAND INVERTER

This inverter is designed using a 2-input CMOS NAND gate shown in figure. The 2 inputs of this are shorted to obtain inverted output. The two parallel PMOS gates are designed in a single P+ diffusion region. The design is developed using 250nm standard fabrication technology. The gate length and width are 2λ and 6λ respectively where λ is the measure of linear distance between the dots shown in fig 4 -8. There are provisions for applying input signal at either side of the Polysilicon. This is for the simplicity of the overall design.

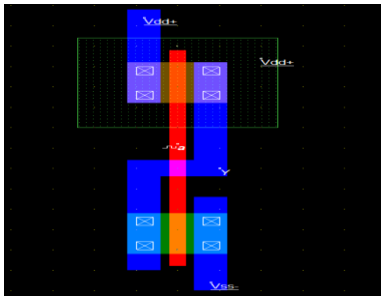

Fig 4. Layout design of NAND inverter

REALIZATION OF 2 INPUT CMOS NAND GATE

Figure 5 shows the realization of a 2-input CMOS NAND gate. This is same as the design in figure 4 except the two separate input nodes. This design also provides options for applying input signals and obtaining the output signal from either side. The gate lengths (2λ) are kept very short and widths (6λ) are kept high enough to obtain the rise time and fall time sufficiently small. The output is taken out using metal layer 2 to avoid unnecessary interconnections

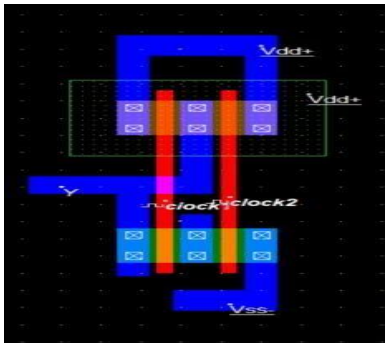

Fig 5 . Layout design of 2 input CMOS NAND gate

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REALIZATION OF A 3-INPUT CMOS NAND GATE

The 3-input CMOS NAND gate shown in figure 6 is designed exactly the same way as the 2-input NAND gate in figure 5. The parallel PMOS gates are located in a single P+ diffusion layer. This design excludes the use of extra Polysilicon as used in conventional design layout.

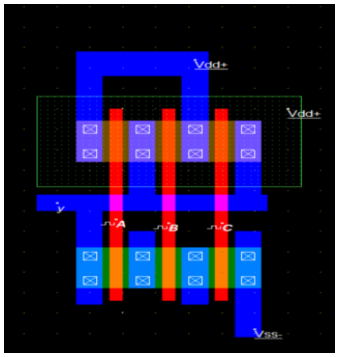

Fig 6. Layout design of 3 input CMOS NAND gate

REALZATION OF 4- INPUT CMOS NAND GATE

The 4-input CMOS NAND gate presented in figure 7 is also designed exactly the same way as the designs in figure 4, figure 5 and figure 6. Use of single P+ diffusion layer contributed towards elimination of redundant Polysilicon.

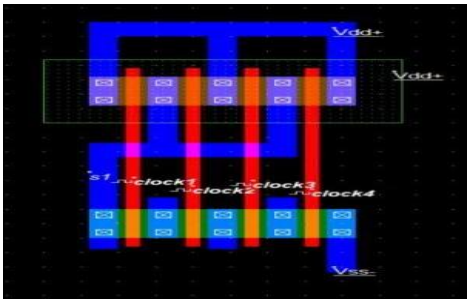

Fig 7. Layout design of 4-input CMOS NAND GATE

REALIZATION OF SUM FUNCTION

The sum function is designed using 3 inverters,four 3-input CMOS NAND gates and one 4-input CMOS NAND gate.These are arrranged and made connections properly for better performance of the function.

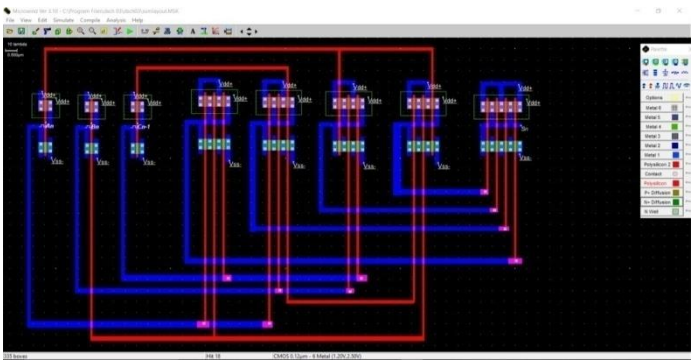

Fig 7. Formation of SUM function

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REALIZATION OF CARRY FUNCTION

The carry function can be realized using three 2-input CMOS NAND gates and one 3-input CMOS NAND gate.By using these gates and arranging properly a carry function can be realized.

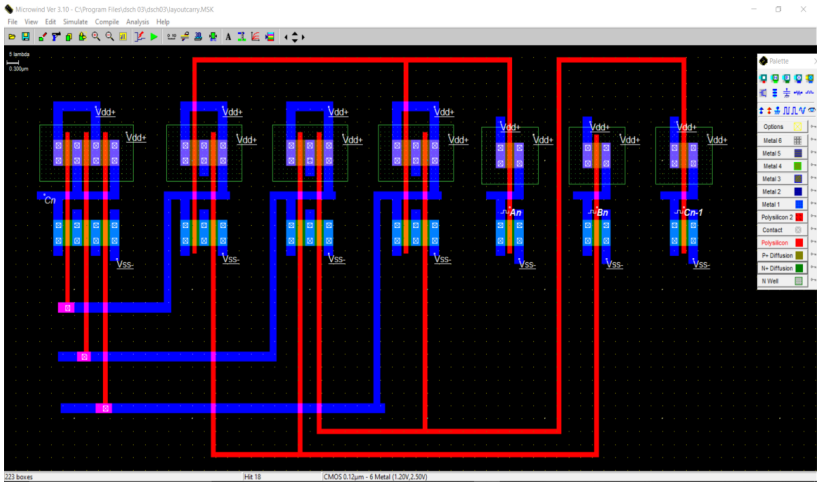

Fig 8.Formation of CARRY function

FINAL LAYOUT OF 2-BIT NAND ADDER

When all the 4 types of logic gates were designed they were simply copied and pasted side by side in such a way as to resemble the figure 1 to design a 1 bit full adder. The 3 (2 binary bits and a carry bit) input signals were fed from a horizontal metallic bus line at the top of the design into 3 CMOS inverters. The inverted outputs were also available at 3 different bus lines. At this stage the necessary interconnections were achieved carefully in a regular fashion. The whole 1 bit full adder was copied and pasted side by side to form a 2 bit adder. The final design was optimized to form single P+ diffusion, single +Vdd and single –Vss supply. Figure 8 shows the final diagram and figure 9 represents the end of the process 3D architecture of the designed layout.

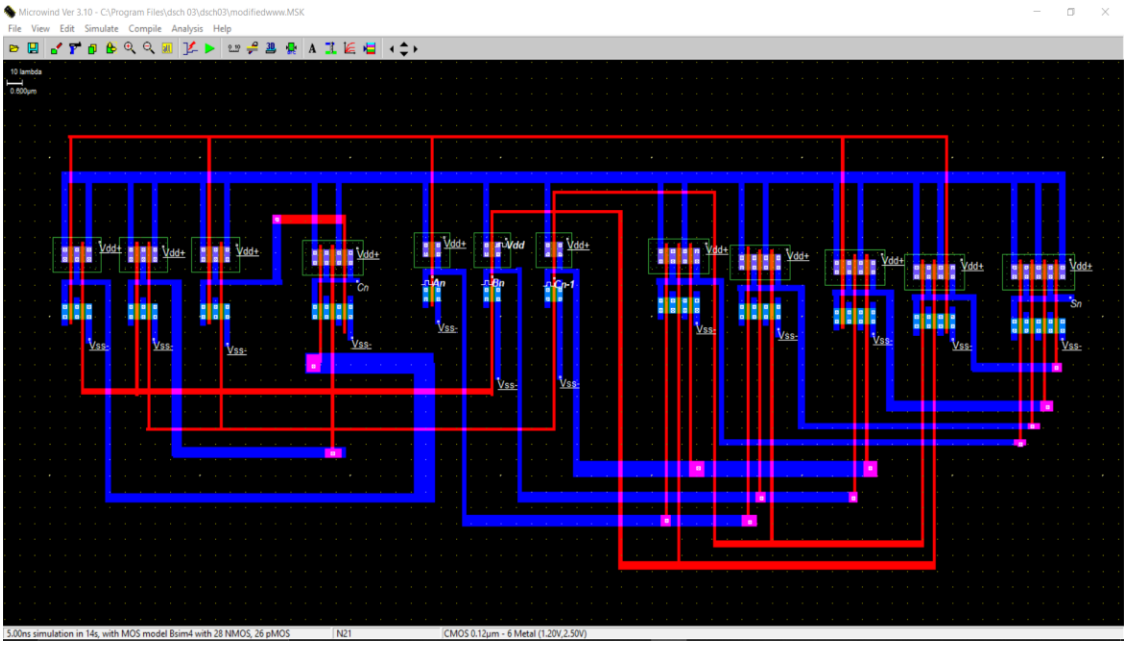

Fig 8. Final formation of NAND ADDER

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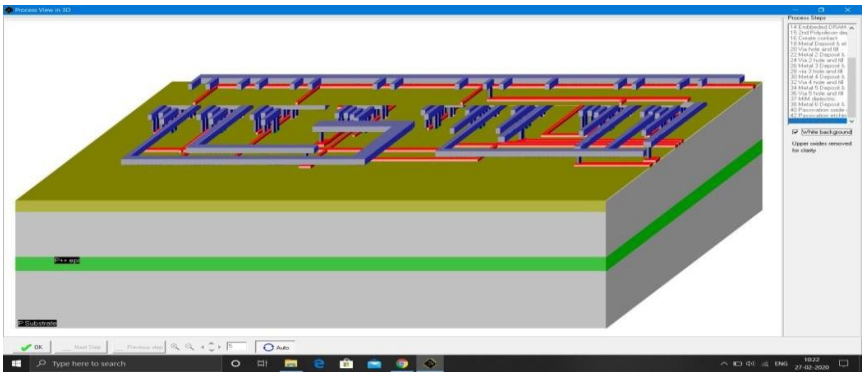


Fig 9. 3-D view of designed layout

Figure 9 shows the 3D view of the designed layout. The design involved the steps of Substrate preparation, N diffusion, SiO2 trench isolation, Polysilicon deposition, N+ and P+ implantation, creating metal contacts, 3 layers of metal deposition, etching, and respective via hole filling

IV. PERFORMANCE OF THE ADDER

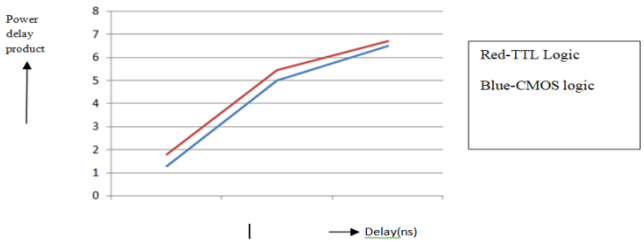
CMOS logic dissipates less power than any other logic circuits. This is because CMOS dissipates power only when switching (“dynamic power”). On the other hand, NMOS logic dissipates power whenever the output is low ("static power"), because there is a current path from Vdd to Vss through the load resistor and the n-type network . The performance parameters of the design comes from the direct comparison of CMOS or TTL family gates.

COMPARISION BETWEEN CMOS AND TTL

PARAMETER	TTL	CMOS
Power	1.3mw	0.488mw
Delay	5ns	0.45ns
Power Delay Product	6.5p	0.21P

Table 4. Comparision between CMOS and TTL

GRAPHICAL REPRESENTATION



From this graphical representation we can see that the performance of CMOS is better while compared to TTL in terms of power.

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V. SIMULATION RESULTS

Fig 10.Waveform of final NAND adder

VI. CONCLUSION AND FUTURE SCOPE

In this the design of compact formation of a 2-bit binary parallel adder using only CMOS NAND gates. Improvement of this layout is possible by designing the gate lengths and widths using more optimization factors. The ripple carry adders are generally slower than other types of adder since the output waits until the carry is generated from previous blocks. The other types of adders such as Carry Select adder, Carry Skip Adder, Carry look ahead adder etc. often require more area than the ripple carry adder. That's why there is always a scope to tradeoff between the speed and the size of the device while designing any adder circuit.

Although we have many advantages from CMOS such as high noise immunity, low power consumption, low static power dissipation but the delay in CMOS is high so that speed of operation will be reduced. So hybrid **Single Electron Transistor- Complementary Metal Oxide Semiconductor (SET-CMOS)** is used to design the ripple carry adder to increase the perfomance.

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