ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijircce.com

Vol. 5, Issue 1, January 2017

Design and Novel Approach towards Adders and Subtractors Using Quaternary Logic

R.N.Uma Mahesh

Asst. Professor, Dept of ECE, ATME College of Engineering, Mysuru, India

ABSTRACT: At beginning era of digital design, the binary logic is used in all industrial applications. The binary logic uses 2 states i.e. 0's and 1's to represent each state. Since the binary logic uses 2 states, it requires more number of bits to represent a number. For example, the number 25 is represented in $(11001)_2$ this format. So this number 25 requires 5 bits to represent it. And also occupies more area and more power in the circuit. Therefore ternary logic is introduced. Here the ternary logic uses less number of bits to represent a number compare to binary logic. It also reduces the area and also the power of the circuit.The ternary logic uses 3 states i.e. 0,1,2 where logic 0 is considered as low state and logic 1 is considered as middle state and logic 2 is considered as high state. The same number 25 to represent in ternary logic requires 3 bits. i.e. It is represented as $(221)_3$ in ternary logic. The quaternary logic uses 4 states i.e. 0,1,2,3 states. The quaternary logic further reduces number of bits and also enhances the power compare to binary and ternary logic. The number (25) in quaternary logic is represented as $(121)_4$ in this format.

KEYWORDS*:* radix,state,binary,ternary,quaternary number.

I. INTRODUCTION

The digital design has different kinds of number systems.it includes binary number system, octal number system, decimal number system, hexadecimal number system. Every number system has different kinds of radix indices. For example the radix of binary number system is 2. similarly the radix of octal number system is 8. The radix of decimal number system and hexadecimal number system is 10 and 16 respectively. Here the quaternary adders and subtractors are designed. The radix of quaternary number system is 4.i.e each decimal number is represented using 4 digits. i.e. by using 0,1,2,3 digits. In quaternary logic, the logic zero state is taken as low state and logic 3 is considered as high state and logic 1 and logic 2 are considered as middle states. The quaternary adders include quaternary half adder and quaternary full adder. The quaternary subtractors include quaternary half subtractor and quaternary full subtractor. Compare to binary and ternary logic number system, the quaternary logic number system reduces number of bits to represent a number and also reduces area required for IC design and also reduces the power for the circuit. Therefore quaternary logic is more useful for all industrial applications.Further, the quaternary microprocessor and microcontroller can also be designed for the advancement of technology. Therefore this quaternary logic helps for the advancement of digital design and electronic world.

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijircce.com

Vol. 5, Issue 1, January 2017

II. METHODOLOGY

Here the design of quaternary half adder and half subtractor is represented. It's truth table is as shown below.

QUATERNARY HALF ADDER

A	B	Sum	carry
0	0	0	0
0	1	1	0
0	2	2	0
0	3	3	0
1	0	1	0
1	1	2	0
1	2	3	0
1	3	0	1
2	0	2	0
2	1	3	0
2	2	0	1
2	3	1	1
3	0	3	0
3	1	0	1
3	2	1	1
3	3	2	2

TABLE 1.-TRUTH TABLE OF HALF ADDER

The truth table of quaternary half adder is as shown in above table-1. The output carry is one whenever the sum results exceed more than four. The quaternary full adder is similar to half adder except the difference is full adder has 3 inputs.

K-MAP FOR QUATERNARY HALF ADDER

SUM

A \ B	0	1	2	3
0	0	1	2	3
1	1	2	3	0
2	2	3	0	1
3	3	0	1	2

$$SUM=A^0B^1+A^0B^2+A^0B^3+A^1B^1+A^1B^2+A^2B^0+A^2B^1+A^2B^3+A^3B^0+A^3B^2+A^3B^3$$

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijircce.com

Vol. 5, Issue 1, January 2017

CARRY

A \ B	0	1	2	3
0	0	0	0	0
1	0	0	0	1
2	0	0	1	1
3	0	1	1	2

$CARRY=A^3B^3+A^3B^2+A^3B^1+A^2B^2+A^2B^3+A^1B^3$

QUATERNARY HALF SUBTRACTOR

The quaternary half subtractor has 2 inputs and 2 outputs. The outputs are difference and borrow variables. The truth table of quaternary half subtractor is as shown below in table-3.

A	B	Diff	Borrow
0	0	0	0
0	1	3	1
0	2	2	1
0	3	1	1
1	0	1	0
1	1	0	0
1	2	3	1
1	3	2	1
2	0	2	0
2	1	1	0
2	2	0	0
2	3	3	1
3	0	3	0
3	1	2	0
3	2	1	0
3	3	0	0

TABLE-3 TRUTH TABLE OF QUATERNARY HALF SUBTRACTOR

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijircce.com

Vol. 5, Issue 1, January 2017

The k-map for diff and borrow outputs of quaternary half subtractor is as shown below. The quaternary full subtractor is similar to half subtractor except the difference is full subtractor has 3 inputs and the outputs are represented by same variables.

K-MAP FOR QUATERNARY HALF SUBTRACTOR

DIFF

A \ B	0	1	2	3
0	0	3	2	1
1	1	0	3	2
2	2	1	0	3
3	3	2	1	0

$DIFF=A^0B^1+A^0B^2+A^0B^3+A^1B^0+A^1B^2+A^1B^3+A^2B^0+A^2B^1+A^2B^3+A^3B^0+A^3B^1+A^3B^2$

BORROW

A \ B	0	1	2	3
0	0	1	1	1
1	0	0	1	1
2	0	0	0	1
3	0	0	0	0

$BORROW=A^0B^1+A^0B^2+A^0B^3+A^1B^2+A^1B^3+A^2B^3$

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijircce.com

Vol. 5, Issue 1, January 2017

III. CONCLUSION

The quaternary logic helps to reduce the number of bits in a number. The quaternary half adder and half subtractor are as shown above in respective truth tables. The quaternary logic has lot of advantages compare to binary logic and ternary logic. The binary logic occupies more area and requires more power consumption compare to quaternary logic. The quaternary logic also helps for the advancement of technology like designing of quaternary microprocessor and quaternary microcontroller. Like this, the quaternary logic is another approach in digital design and electronic world.

REFERENCES

[1] M.Yoeli, G. Rosenfeld, “Logical Design of ternary switching circuits”, IEEE Trans. Comput., vol. C-14, pp. 19-29, Feb. 1965.
[2] S.L. Hurst, "Two decades of multiple valued logic- an invited tutorial," in Proceedings of IEEE International Symposium on Multiple-Valued Logic, p. 164, May1988.
[3] Michitaka Kameyama, "Toward the Age of' Beyond-Binary Electronics and System”, IEEE Proceedings of 20th International Symposium on MVL, pp.162-166, May 1990.
[4] Subrata Das, Parthasarathi Dasgupta and Samar Sensarma, “Arithmetic Algorithms for quaternary Number System”, Indian Institute Of Management Calcutta Working Paper Series, WPS No. 714, September 2012
[5] K. C. Smith, “The prospects for multi valued logic: A technology and application view,” IEEE Trans on Cornp, vol. C-30, pp. 619-634, Sept. 1981.
[6] H.T. Mouftah and I.B. Jordan, "Integrated circuits for ternary logic," in Proc. ISMVL-74, (Morgantown, WV), pp. 285-302, May 1974.
[7] H.T. Mouftah and I.B. Jordan, "Design of ternary COS/MOS memory and sequential circuits," IEEE Trans. Computers, vol. C-26, pp. 281-288, March 1977.
[8] H.T. Mouftah, "A study on the implementation of three valued logic," in Proc. ISMVL-76, (Bloomington, IL), pp. 123-126, May 1976.
[9] Mouftah, H.T., and Smith, K.C.: ‘Design and implementation of three-valued logic systems’, IEE Proc. G, Electron. Circuits & Syst., 1980, 127, (4). pp. 165-168