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A Review: Design of Improved High Performance of High Valency Ling Adder

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ABSTRACT: Two-operand binary addition is the most widely used arithmetic operation in modern data path designs. Parallel prefix adders are used for economical VLSI implementation of binary variety additions. Parallel-prefix adders offer a highly efficient solution to the binary addition problem and are well-suited for VLSI implementations. The look and implementation details for such lower complex quick parallel prefix adders supported Ling theory of resolving. Specifically, valency or node indicates number of inputs given to a particular node in a carry tree. Ling design offers a quicker carry computation stage compared to the standard parallel prefix adders by projecting a replacement methodology to solve Ling adders, which helps to cut the complexity and also the delay of the adders.

KEYWORDS: Parallel prefix adders; Area; Delay;Valency; Node;

I. INTRODUCTION

Binary addition is one of elemental operation in electronic circuit. Several circuits contain many adder unit for applications like arithmetic logic unit, thus, there's a substantial interest to style less advanced and better speed and adder architectures. Within the past few decades, numerous architectures of adders are planned to optimize the delay of the adder, examples embrace, carry-look ahead, ripple carry and parallel prefix adder.

The parallel prefix adder is one in all the foremost in style architectures and offers sensible compromise among power, space and speed. This sort of adder implements a logic performs to see whether or not every bit position kills the carry or propagates it or generates it. Then these generate and propagate/not kill functions are hierarchically combined to cipher the carry into every bit position forming a carry tree .

A large variety of algorithms and implementations have been proposed for binary addition. Speed is required for high operation tree structures, like parallel-prefix adders, are used. Parallel-prefix adders are suitable for VLSI implementation since they rely on the use of simple cells and maintain regular connections between themSeveral variants of the carry-lookahead equations, like Ling carries, can be presented that simplify carry computation and can lead to faster structures Adders form an almost indispensable component of every contemporary integrated circuit.

To cope with varying requirements of time and area efficiency, several adder architectures have appeared ranging from the smallest ripple-carry adders with the linear to the operand length delay up to the Carry Look-Ahead (CLA), conditional-sum and parallel-prefix adders which provide the fastest possible implementations at the expense of the largest circuit sizes. Between these two categories lie the carry-skip and carry-select architectures, which give a good alternative, since they combine relatively small area and substantially reduced delays. Ling design offers a quicker carry computation stage compared to the standard parallel prefix adders.

II. LITERATURE REVIEW

1]Sabyasachi Das , Sunil P. Khatri

S. Das and S. P. Khatri, “A novel hybrid parallel-prefix adder architecture with efficient timing-area characteristic”.

Author concluded that a hybrid approach of implementing an adder block based on the fast parallel prefix architecture. The proposed adder exhibits very efficient timing area tradeoff characteristics. It works seamlessly with

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adder blocks of different widths and across different technology domains adder also shows marginally faster performance than the fast koggestone adder with significant area savings

2]Giorgos Dimitrakopoulos and Dimitris Nikolos
"High-Speed Parallel-Prefix VLSI Ling Adders"
A systematic methodology for designing parallel-prefix Ling adders has been introduced. The proposed adders preserve all the benefits of the traditional parallel-prefix carry- computation units, while, at the same time, offering reduced delay and fanout requirements. Hence, high-speed datapaths of modern microprocessors can truly benefit from the adoption of the proposed adder architecture. In this paper, a novel framework is introduced, which allows the design of parallel-prefix Ling adders. The Area and Delay Estimates for Lander-Ficher adderand kogge-stone adder are 23654um^{2}and 0.86ns, 28385um^{2}and 0.81ns.

3]C. Huang, J. Wang, C. Yeh and C. Fang, "The CMOS carry-forward adders"
Author concluded that The carry farward adder is based on the dynamic ripple-carry adder (DRCA) and a cost-effective race-rescue method to preserve area efficiency, while diagonal forwarding is combined with multilevel folding for dramatic speed improvement of the DRCA. Based on all the proposed techniques, a 32-bit dynamic carry-forward adder (CFA32) with two-level carry forwarding was designed and fabricated.

III. PREVIOUS WORK

The structure of the prefix network specifies the type of the PPA. The Prefix network described by, Sabyasachi Das , Sunil P. Khatri,Giorgos Dimitrako poulos and Dimitris Nikolos,Chung-Kuan Cheng In has the minimal depth for a given 'n' bit adderOptimal logarithmic adder structures with a fan-out of two for minimizing the area-delay product is presented by Matthew Ziegler and Mircea Stan previous method hybrid approach of implementing an adder block based on the fast parallel prefix architecture.

IV. PROPOSED WORK

Throughout the rest of this paper, parallel prefix adder and ling adder is introduced. kogge stone adder and lander adder are type of parallel prefix adder. these adder are implemented by using the logic level implementation of basic cell. there are three of logic level implementation of basic cell.

A. Basic cell

- Implementation of first basic cell

In proposed adder, square represents the first basic cell. The internal structure of first basic cell is given below

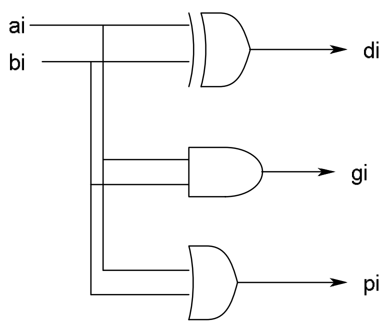

Fig**1:**Basic cell structure

In this, we use three logic gates
a)EX-OR gate b) AND gate c)OR gate where, di represent the output of EX-or gate gi represent the output of AND gate pi represent the output of OR gate

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- Implementation of second basic cell

In proposed adder, dark circle represents the second basic cell. The internal structure of second basic cell is given below

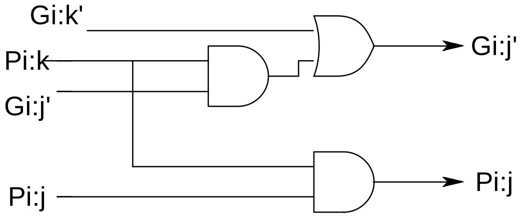

Fig2:Basic cell structure

The output of first basic cell is given input to the second basic cell and Gi:j’ and Pi:j is the output of the second basic cell.

- Implementation of third basic cell

In proposed adder, diamond represents the third basic cell. The internal structure of third basic cell is given below

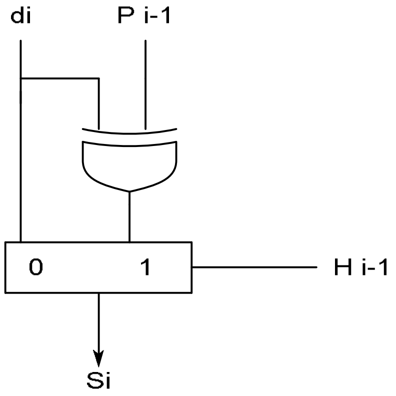

Fig3:Basic cell structure

B.Kogge stone adder

Kogge-Stone adder is a parallel prefix form carry look ahead adder. Kogge-Stone prefix adder is a fast adder design. Kogge-stone adder has best performance in VLSI implementations. Kogge-Stone adder has large area with minimum fan-out. The Kogge- Stone adder is widely known as a parallel prefix adder that performs fast logical addition. Kogge-Stone adder is used for wide adders because of it shows the less delay among other architectures.

Diagram shows the kogge stone adder, five layer of basic cell are used. The first layer indicate the first basic cell which having the two input and three output. Second, third, fourth layer indicate the second basic cell and fifth layer indicate the third basic cell of kogge- stone adder.

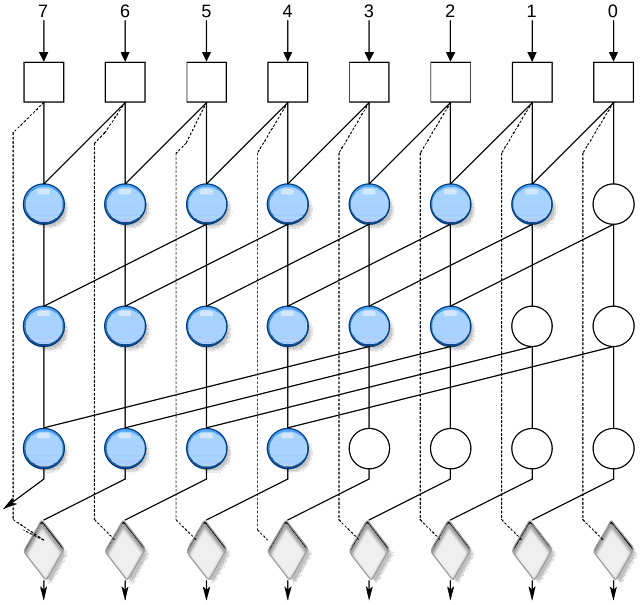

Fig 4: Kogge stone adder

C. Lander-Fischer adder

Ladner- Fischer adder is a parallel prefix adder. This was developed by R. Ladner and M. Fischer in 1980.Ladner-Fischer adder has minimum logic depth but it has large fan-out . Ladner- Fischer adder has carry operator nodes.
Diagram shows the lander-Fischer adder, five layer of basic cell are used. The first layer indicate the first basic cell which having the two input and three output. Second, third, fourth layer indicate the second basic cell and fifth layer indicate the third basic cell of Lander-Fischer adder

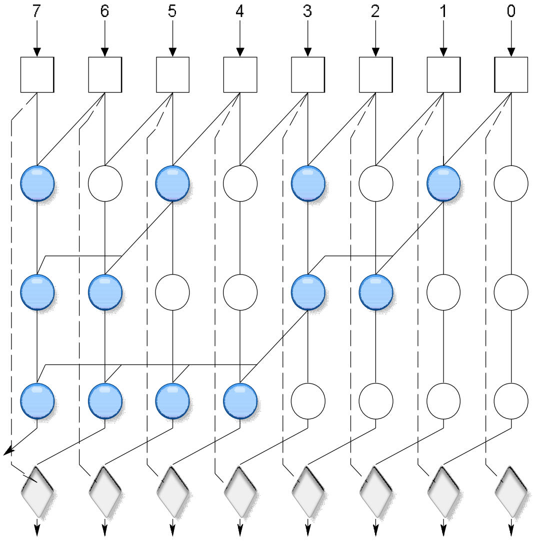

Fig5: Lander- Fischer adder

D. Ling adder

Ling architecture offers a faster carry computation stage compared to the conventional parallel prefix adders. which helps to reduce the complexity as well as the delay of the adder further. This paper discusses the design and implementation details for such lower complexity, fast parallel prefix adders based on Ling theory of factorization. In particular, valency or radix, the number of inputs to a single node, is explored as a design parameter. Ling adders have superior area×delay characteristics over previously reported Ling-based or non-Ling adders for the same input size.
The generation of the intermediate generate and propagate pairs (Gi*, Pi-1) and the new cell used for the computation of the sum bits in the case of a Ling adder.

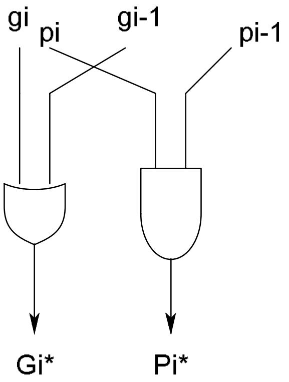

Fig 6:Basic cell of ling adder

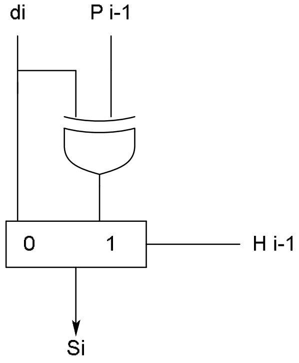

Fig 7:Basic cell of ling adder

Diagram shows the ling adder, six layer of basic cell are used. The first layer indicate the first basic cell which having the two input and three output. Second, third, fourth and fifth layer indicate the second basic cell and six layer of ling adder is shown above.

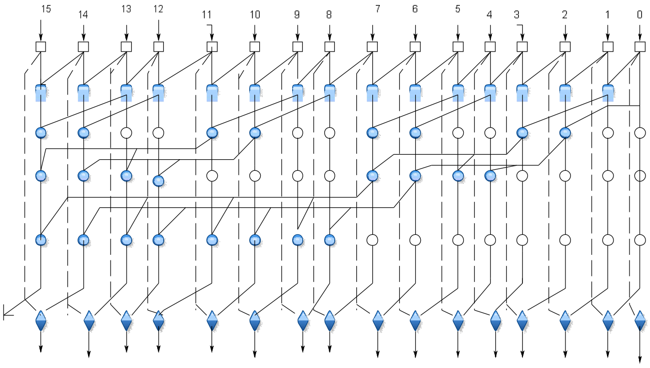

Fig 8:Ling adder

V. CONCLUSION

A systematic methodology for designing parallel-prefix Lingadders has been introduced in this paper. The proposed adderspreserve all the benefits of the traditional parallel-prefix carry computation units, while, at the same time, offering reduced delay and fanout requirements. Hence, high-speed datapaths of modern microprocessors can truly benefit from the adoption of the proposed adder architecture

REFERENCES

1. A. Weinberger and J. L. Smith, "A logic for high speed addition", National Bureau of Standards, Circulation 591, pp. 3-12, 1958.
2. T. Lynch and E. Swartzlander, "A spanning tree carry look ahead adder", IEEE Trans. on Computers, vol. 41, no. 8, pp. 931-939, 1992
3.] G. Yang, S. Jung, K. Baek, S. Kim, S. Kim, S. Kang, "A 32-bit carry lookahead adder using dual-path all-N logic", IEEE Trans. on VLSI Systems,vol. 13, no. 8, pp. 992-996, 2005.
4. S. Hauck, M. Hosler and T. Fry, "High performance carry chains for FPGAs", IEEE Trans. on VLSI Systems, vol. 8, no. 2, pp. 138-147, 2000.
5. C. Huang, J. Wang, C. Yeh and C. Fang, "The CMOS carry-forward adders", IEEE Journal of Solid-State Circuits, vol. 39, no. 2, pp. 327-336,2004.
6. R.E. Ladner and M.J. Fischer, "Parallel prefix computation", Journal of ACM, vol. 27, no.4, pp.831-838, Oct. 1980.
7. S. Knowles, "A family of adders", Proc. 14th IEEE Symp. On Computer Arithmetic, pp.3034, 1999.
8. P.M. Kogge and H.S. Stone, "A parallel algorithm for efficient solution of a general class of recurrence equations",IEEE Trans. On Computers, vol. C-22, no. 8, pp.786-793, Aug. 1973
9. H. Ling, "High speed binary adder", IBM Journal of Research and Development, vol. 25, no. 3, pp. 156-166, 1981.
10. S. Das and S. P. Khatri, "A novel hybrid parallel-prefix adder architecture with efficient timing-area characteristic", IEEE Trans. On VLSI Systems, vol. 16, no. 3, pp. 326-331, 2