Low Power High Speed Body Bias Controlled Current Latch Sense Amplifier

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ABSTRACT: Sense amplifiers are extensively used in memory. Sense amplifiers are one of the most vital circuits in the periphery of CMOS memories. We know that memory is the heart of all digital systems. Today all worlds are demanding high speed and low power dissipation as well as small area. We know that speed and power dissipation of memory is overall depends upon the sense amplifier we used and their performance strongly affects both memory access time, and overall memory power dissipation. So it is important to design a good sense amplifier which performs well in both speed and power dissipation. In this dissertation, an implementation of a most efficient sense amplifier is done by comparing the best known sense amplifier in today. The dissertation focuses on design, simulation and performance analysis of sense amplifiers.

I. INTRODUCTION

Digital system design in an amazing and emerging field now days. Each and every digital system has adequate memories. In memory today the CMOS memories are used in a much greater quantity than all the other types of semiconductor integrated circuit. SRAMs are used as large caches in microprocessor cores and serve as storage in various inputs on a system-on-chip like graphics, audio, video and image processors. SRAMs also used in high performance microprocessors and graphics chips so for each generation to bridge the increasing divergence in the speeds of the processor and the main memory we need high speed requirements. At the same time, SRAMs used in application processors which go into mobile, handheld and consumer devices have very low power requirements. So power dissipation has become an important consideration both due to the increased integration and operating speeds, as well as due to the explosive growth of battery operated appliances. As with other integrated circuits today, CMOS memories are required to increase speed, improve capacity and maintain low power dissipation.

Necessity of Sense Amplifier
In the memory, it is common to reduce the voltage swing on the bit lines to a value significantly below the supply voltage. This reduces both the propagation delay and the power consumption. Noise and other disturbances may be occurred in the memory array for this sufficient noise margin is obtained even for these small signal swings. During the interfacing of the memory to the external field, the amplification of the internal swing is required. This is achieved by the sense amplifiers. Design of a high performance and efficient sense amplifier is very important for design SRAMS but with increasing parameter variations, the developing of a reliable and fast sense amplifier is a big problem in itself Sense amplifiers play a major role in the functionality, performance and reliability of memory circuit. Reduction in delay and power is acquired by using sense amplifier in memory circuits.
The designed sense amplifier should be standard and capable to support the current SRAM design without significantly affecting the other devices of peripherals of SRAM.

II. BASIC OF SENSE AMPLIFIER

A sense amplifier is an active analog circuit that reduces the time of signal propagation from an accessed memory cell to the logic circuit located at the periphery of the memory cell array, and used to detect small variation on bitlines of memory and produce full voltage swing it means that converts the arbitrary logic levels occurring on a bitline to the digital logic levels of the peripheral Boolean circuits. The sense amplifier circuit has to operate within the conditions

which are set by the operation margins. Operation margins in a digital circuit are those domains of voltages, current and charges. These domains unambiguously represent data throughout the entire operation range of the circuit. Operation margin depends on the circuit design, processing technology and environmental conditions. Sense amplifiers, used with memory cells, are key elements in defining the performance and environmental tolerance of CMOS memories. Because of their great importance in memory designs, sense amplifiers became a very large circuit-class. CMOS memories are used in a much greater quantity than all the other types of semiconductor integrated circuits, and appear in an amazing variety of circuit organizations.
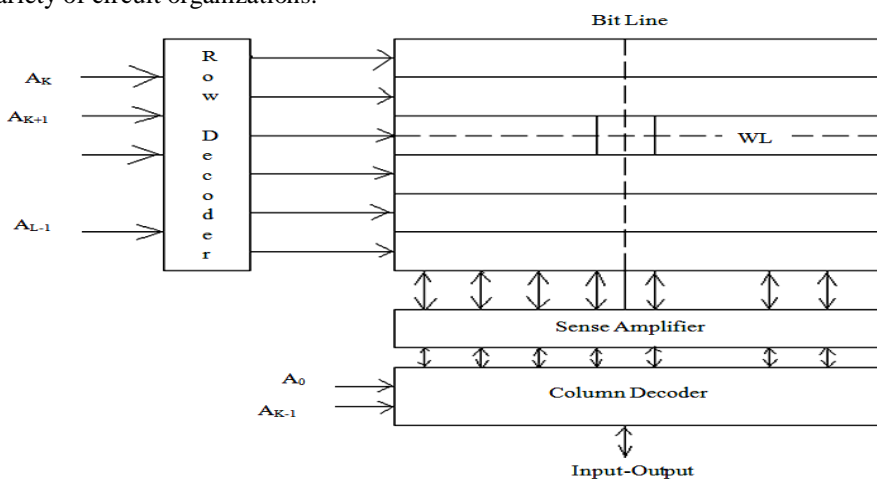

Fig. 1 Memory Architecture

Functions of Sense Amplifier
1. Amplification: In certain memory structure, amplification is required for proper functionality since the typical circuit swing is limited. In other memories, it allows resolving data with small bit line swings, enabling reduced power dissipation and delay.
2. Delay reduction: The amplifier detects and amplifies small transition on the bit line to large signal output swings, due to which a small swing input is used and the delay will Reduce
3. Power reduction: Reducing the signal swing on bit lines can eliminate a substantial part of power dissipation related to charging and discharging the bit lines

III. DESIGN IMPLEMENTATION AND SIMULATION OF SENSE AMPLIFIERS

On the modern trends quick memories are highly required with low power consumption. The low power and low voltage CMOS techniques were applied extensively in analog and mixed mode circuits for the compatibility with the present IC technologies. Low power consumption can be achieved by using sense amplifiers which are main part of CMOS memory. Parasitic capacitance is much higher if memory is of high density. The large capacitance is an issue to make our each cell more energy to charge means low to sense amplifier. To achieve a faster memory and less power dissipation we have to design sense amplifiers as. Increase in number of cells per bit line which will increase the parasitic capacitance. Minimize supply voltage lead to short noise margin that affects the sense amplifier reliability. To maintain small voltage swing over the bit line, increase the area of each cell for design more memory on the chip which decreased the load on bit line. The wide range of applications of sense amplifier as it provides a photovoltaic system which usually stores enough energy for uncertainty in availability of solar radiation due statically nature of biosphere. These typical ICs are the complex component to measure the charge battery and discharge current. sense amplifiers plays a very smart role to maintain the reliability , accuracy and extended battery life by cutting power down over certain region to control heat. Mainly two types of SRAM sense amplifier linear amplifier and latch type amplifier.

Current Latch Sense Amplifier (CLSA)

Latch-type sense amplifiers, or sense amplifier based flip-flops, are very effective comparators. They achieve fast decisions due to a strong positive feedback and their differential input enables a low offset. The sense amplifiers circuit is the heart of memory. The sense amplifiers are mainly designed to read the memory contents and amplify them to proper level using at logic circuits around memory. Sense amplifiers (SA) are hence widely applied in, for example, memories, A/D converters, data receivers and lately also in on-chip transceivers have become especially popular because of their high input impedance, full-swing output and absence of static power consumption. A good SA has the following properties namely, minimum sense delay, minimum power consumption, proper gain for amplification, minimum layout area, highly reliable, less number of cascading of transistors from source voltage to ground for low voltage operation and tolerable to environment. This kind of sense amplifier circuit is designed for increased speed, sensitivity with reduced power consumption. This design combines aspects from the latch based voltage mode sense amplifier and the differential
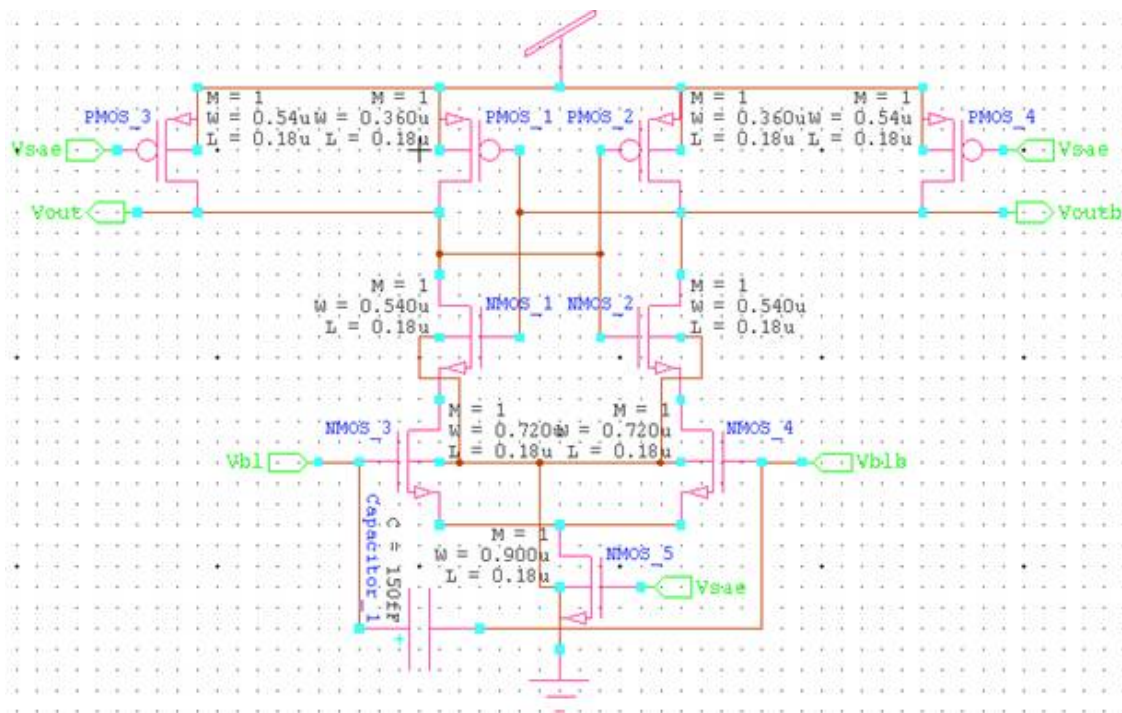

Fig. 2 Current Latch Sense Amplifier (CLSA)

It consists of 5 nMOS and 4pMOS transistors namely MN1, MN2, MN3, MN4, and MN5. MN1, MP1, MN2 and MP2 make two inverters connected in cross coupled manner give positive feedback in circuit.MN3 and MN4 are used to couple bitlines to CLSA amplifier.MP3 and MP4 are precharge transistors. The capacitor C represents the column capacitance of bitlines for filling of SRAM in circuit. The sense amplifier has following ports namely Vsae, vout, voutb, bl, blb. The bl and blb are column bit lines of SRAM. The signals are given to the **Vsae** which control the precharge and enable CLSA.The amplified output is taken from **Vout** node and complimentary output at **Voutb** node.

Latch Operation

In gives the circuit of cross coupled inverters working as latch also shown its voltage transfer characteristics. If the circuit working at one stable state then if we want to change it state change we use the sufficient external voltage applied to inputs.
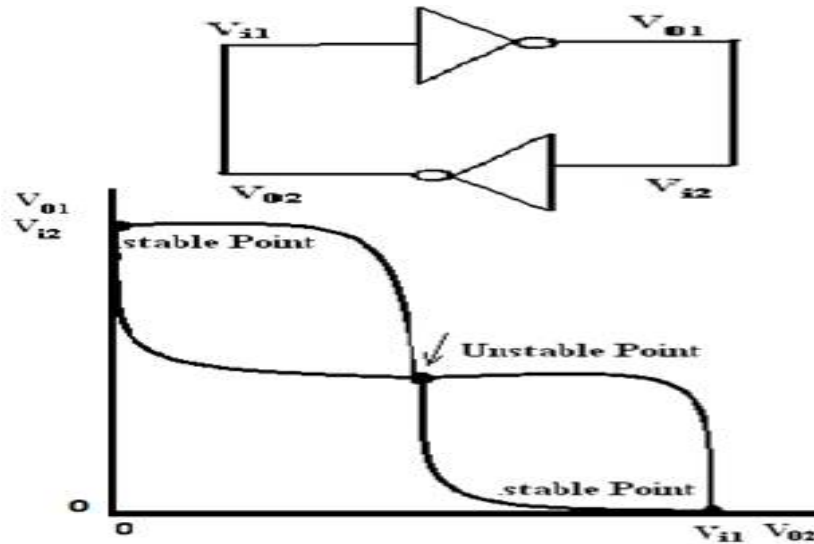
Fig. 3 Inverter latch and it's Voltage Transfer Characteristic

The Sizing Consideration

The main aim of sizing is

- Sense amplifiers dissipate low power.
- Work faster at low delay.

Sizes will be so selected that which minimize the power consumption while maintain amplifier stability and at low delay. The two parameters may be considered during the sizing process are the channel Width and channel length.

The CLSA has 9 transistors. These transistors MN1, MP1 and MN2, MP2 make a cross coupled inverter latch so that MN1and MN2 sized equal similarly MP1and MP2 sized equal. For equal threshold voltages, V_{TH} of inverters have equal value. Because μ_p and μ_n are different so W/L ratio selected such that k_n must be equal to k_p where k is parameter defined by these equations

$$k_n = \frac{\mu_n C_{ox} W_n}{L_n} \quad , \qquad k_p = \frac{\mu_p C_{ox} W_p}{L_p}$$

Subscript n and p used for electrons and holes respectively. Because $2\mu_p \approx \mu_n$ so the width of the pMOS should be double the width of the pMOS to kept the parameter k_p equals k_n. In inverters transistors for minimum delay and area we take the channel length L minimum to CMOS process other requirement is fulfilled by channel width W.

For precharge pMOS transistors we take large width W_p than channel length Lp due to this large drain current flow thru circuit which rapidly charge the node which is only limited by current source nMOS transistor.

To reduce the power consumption the flow of current thru this current source minimum for these nMOS transistors which used as current source larger channel length L_n and width is kept as possible as low which also fulfills our requirements. We take the following W/L ratio for this CLSA in this dissertation which is shown in this table.

Table 4.1 Channel Width W and Channel length L

S.No	Transistors	W in μ meter	L in μ meter	W/L Ratio
1	MN1	540	180	540/180=3
2	MN2	540	180	540/180=3
3	MN3	720	180	720/180=4
4	MN4	720	180	720/180=4
5	MN5	900	180	900/180=5
6	MP1	360	180	360/180=2
7	MP2	360	180	360/180=2
8	MP3	900	180	900/180=5
9	MP4	900	180	900/180=5

IV. RESULT ANALYSIS AND COMPARISON

Current Latch Sense Amplifier (CLSA)

In this section I show the simulation results of Current Latch Sense Amplifier (CLSA). The simulation time is taken for CLSA amplifier is 60 neno seconds. The simulation waveform of the CLSA is shown in(a) shows the simulation waveform of the CLSA at V_{DD}=5Volt. V_{sae} given in pulses of 0.5 duty cycle with time period of 10n seconds both rise and fall time is 1n seconds. Similarly bit input to V_{bl} is in bit form and in sequence of 10101 and inverse of this is V_{blb}.The total simulation time is 60n seconds.
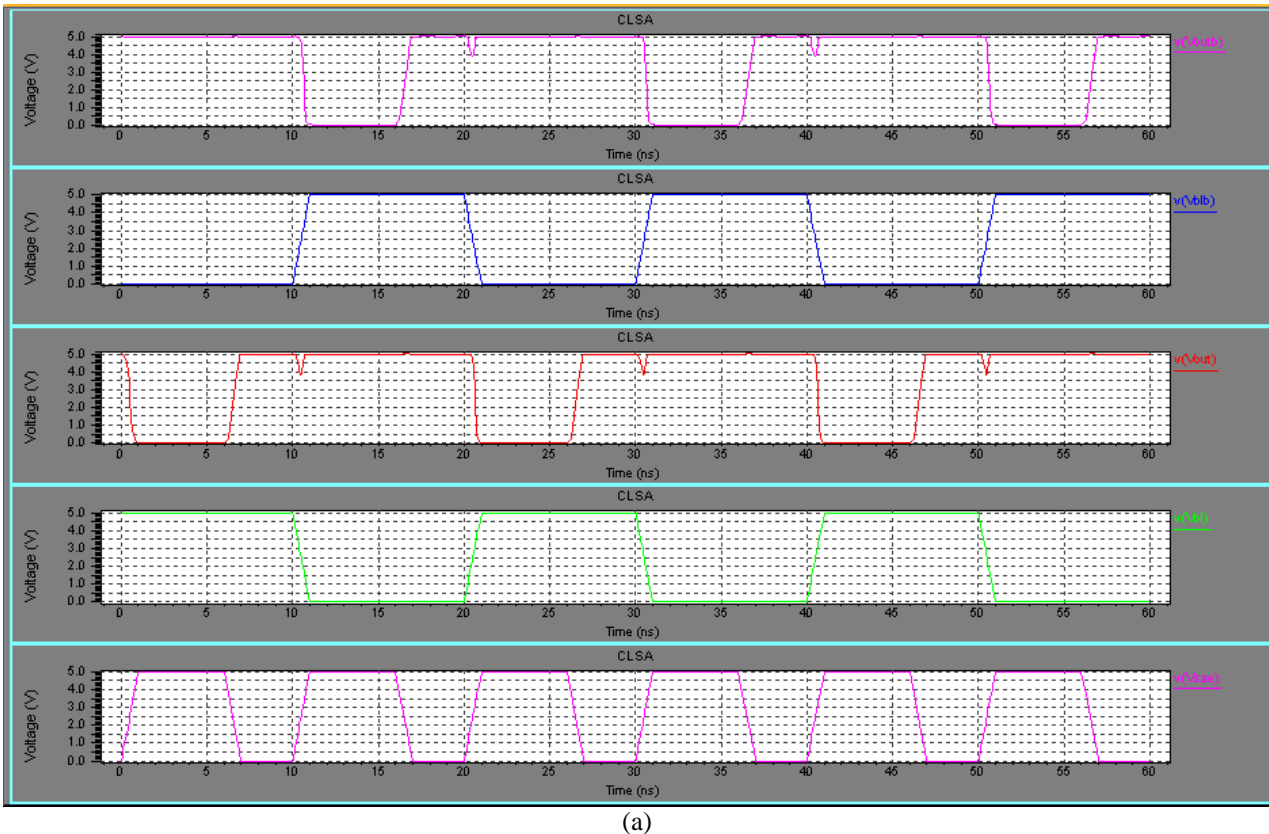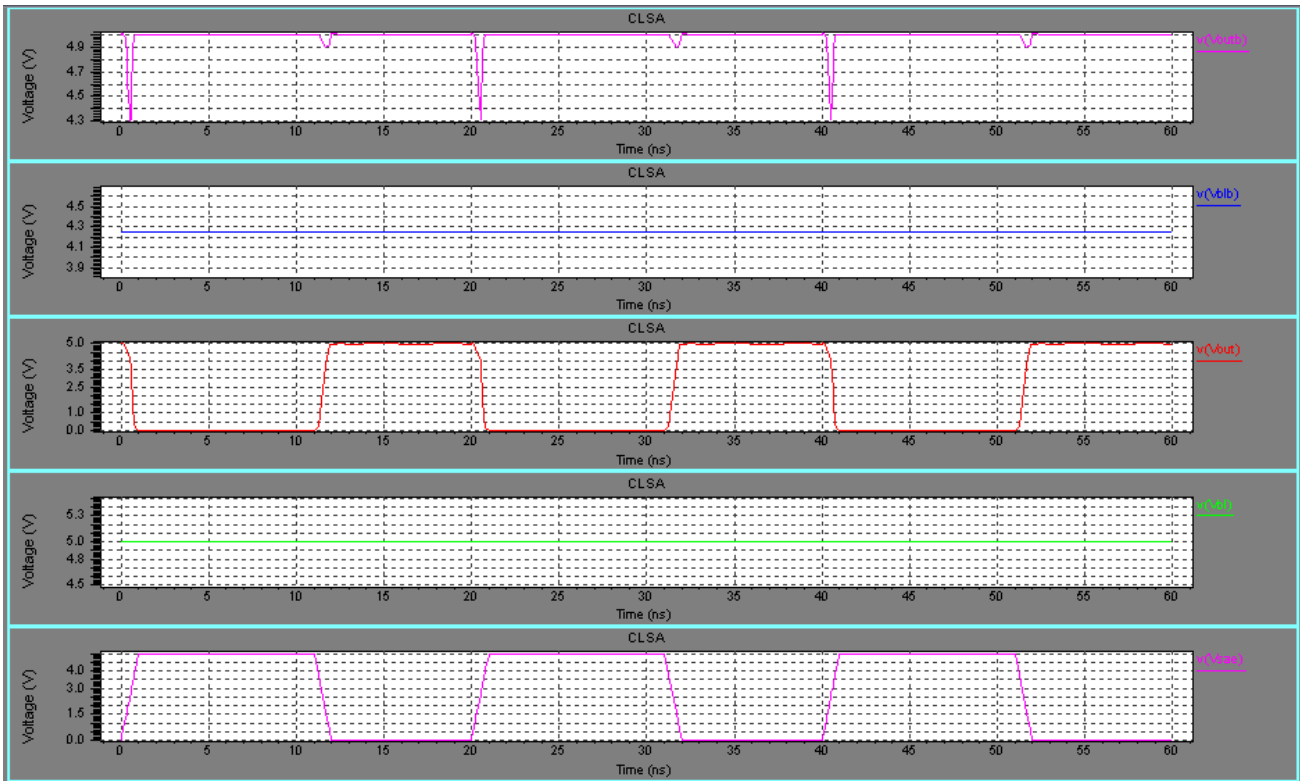

(a)

(b)

Fig. 4 Simulation waveforms of the Current Latch Sense Amplifier (CLSA) (a) for Bit Voltage (b) For Constant Voltage Difference

Similarly shows the wave form at VDD at 5 volts, Vbl at 5 volts and Vblb taken at 4.25 volts. The functionally this is shown in waveform that when Vsae is at low volts seen in v (Vase), the amplifier pre-charged to VDD. When Vsae is at high level then sense amplifier is in sensing mode so Vout should be 0volt if Vbl is at 5volt otherwise if Vblb is at 5 volts its value at full swing value which is 5volts. We obtained reverse value for Voutb node which is shown as Voutb value.

Table 2 CLSA operation

Vsae	Vbl	Vblb	Vout	Voutb	Remark
5V	5V	4.5 V	0V	5V	In sense mode
0V	5V	4.5 V	5V	5V	In pre-charge mode
5V	4.5V	5 V	5V	0V	In sense mode
0V	4.5V	5 V	5V	5V	In pre-charge mode

This is also true for pulse inputs.

Figure 5 shows the VTC of Current Latch Sense Amplifier. This result gives the noise margin of Current Latch Sense Amplifier.
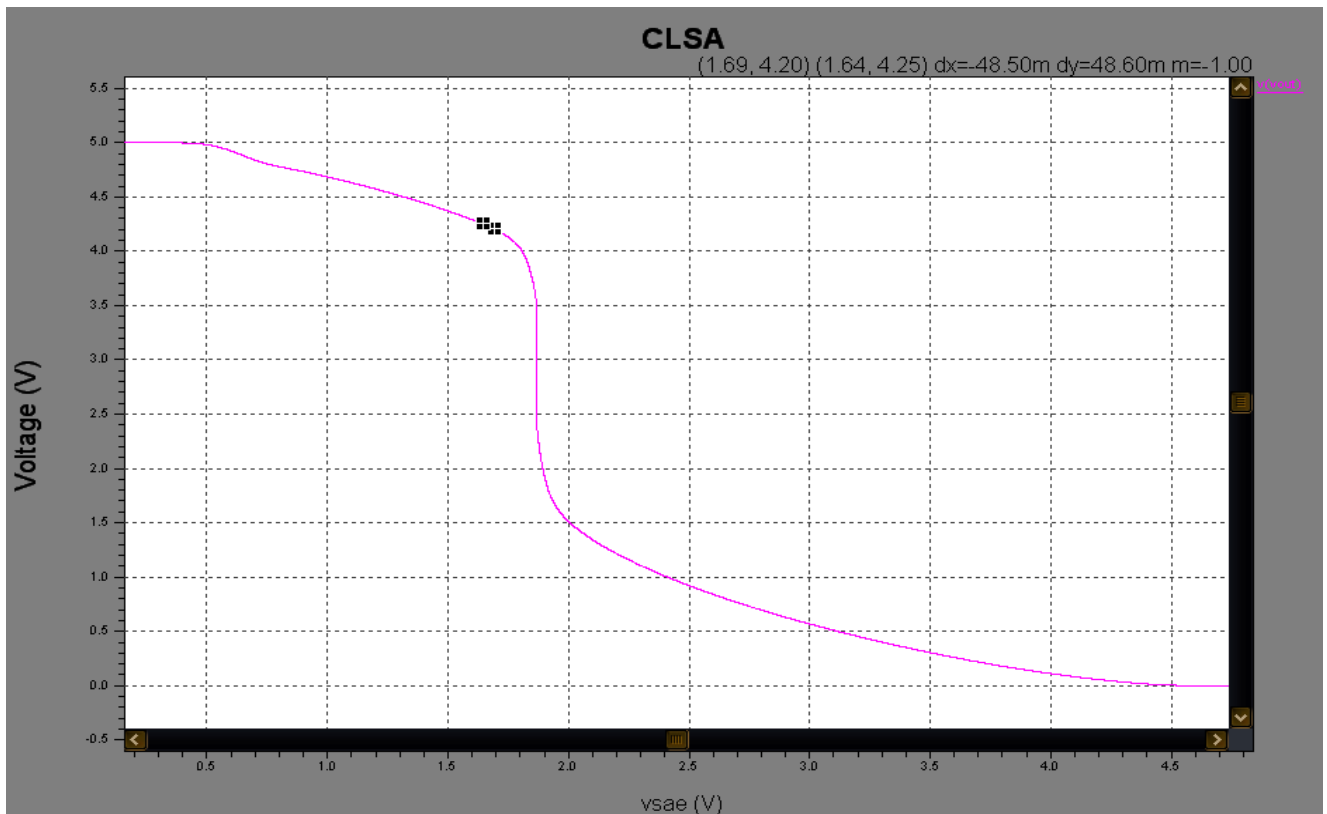
Fig. 5 Simulation waveform of VTC of CLSA

V. CONCLUSION AND FUTURE SCOPE

Conclusion

In this paper Body Bias Controlled Current Latch Sense Amplifier has been designed and simulated using 180nm CMOS technology of tanner tool at a various supply voltage from1.0V to 5.0V. A Sense Amplifier is specially proposed in this dissertation as it is the heart of the Memory. Especially I proposed a BB-CLSA for low power and high speed operations in SRAM. This proposed Sense amplifier is compared with nearest basic Current Latch Sense amplifier as

- The power consumption of proposed BB-CLSA has been reduced from 47% to 87% compared to conventional CLSA.
- Speed of proposed Sense amplifier is increased by 10% as compared to conventional CLSA.
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- Body Bias method is used for high speed at low power dissipation operation.

Only 44% more transistors are used to reduce about 87% power dissipation and to get 10% more high speed operation.

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