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# Design and Implementation of ADDER Circuit using Quantum Dot Cellular Automata (QCA)

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**ABSTRACT**: Recent experiments in the field of VLSI designing and Nanotechnology have demonstrated a working cell suitable for implementing the Quantum-dot Cellular Automata (QCA). QCA is a transistor less computational model which is expected to provide high density nanotechnology implementations of various CMOS circuits. QCA has been constrained by the problem of meta-stable states. QCA adder with comparatively less number of cells and area has been proposed in this paper. This paper also demonstrates a reversible logic synthesis for one bit adder which gives a superior solution for side channel attack based on power analysis in security applications. The new proposed hybrid method reduces cell counts and area and uses conventional form of QCA cells. QCA implementation provides efficient design methodology for faster speed, smaller size and low power consumption when it compared to technology imposed by transistors. QCA provides ability to quickly layout a QCA design by providing an extensive set of CAD tools.

**KEYWORDS:** component: adiabatic switching, combinational circuits, majority gates, meta-stable modular, quantum-dot cellular automata (QCA), quantum cost and reversible logic.

## I.INTRODUCTION

Prior studies suggest that design complexity can be substantially influenced by the majority gate count. The number of majority gates also indirectly determines the cell count due to QCA wires in a design. It is therefore of interest to design methods that involve systematic reduction of majority gates and inverters [6-7]. To the best of our knowledge, there has been no prior work on deriving simplified expressions involving majority gates and inverters for various types of adders. But one basic problem with QCA is that, in settling to the ground state, systems may become trapped in meta-stable states for arbitrarily long periods other than the system's state of least energy. QCAs are never free from fabrication imperfections. The influence of imperfections stem from:

1) Changes of intercellular distance
2) Changes of the height of the inter dot barriers
3) Presence of stray charges

The proposed implementation uses the advantage of both the stable state of QCA and the reversible logic. Minimization of the number of reversible gates, quantum cost and garbage outputs is the focus of research of this paper. In Section II, I-corner implementation of QCA Adder is done. In Section III, basics of adders using QCA as well as their implementation is shown. Performance analysis of the proposed Adder with the previous designs is in section III. Conclusions are presented in last Section.

In QCA-based design, a single device (QCA-cell) is used for the construction of all components of an entire circuit (computational elements and wires). The schematic diagram of a four-dot QCA cell is shown in Figure 1. The cell consists of four quantum dots positioned at the corners of a square and contains two free electrons. A quantum dot is a region where an electron is quantum-mechanically confined (Figure 1(a)). Columbic repulsion will cause classical

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models of the electrons to occupy only the corners of the QCA cell, resulting either in polarization $P = -1$ (logic 0) or in $P = +1$ (logic 1) as shown in Figure 1(b).

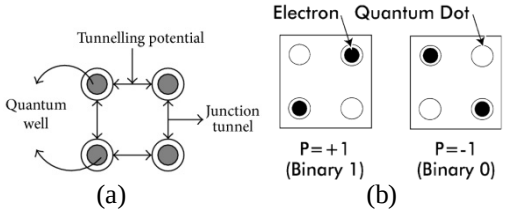


Fig 1:(a) QCA cell and (b) QCA cell with two different polarizations

Timing/synchronization in QCA is accomplished by the cascaded clocking of four distinct and periodic phases as shown. In the first (switch) phase, the tunnelling barrier between two dots of a QCA cell starts to rise. This is the phase during which computation takes place. The second (hold) phase is reached when the tunnelling barriers are high enough to prevent electrons from tunnelling. In the third (release) phase, barrier falls from high to low. The final phase (relax) ensures there is no inter dot barrier and the cell remains unpolarised. Each cell has to pass either of these clocking zones.

## II PROPOSED METHOD

Quantum Dot Cellular Automata (sometimes referred to simply as quantum cellular automata or QCA) are proposed models of quantum computation, which have been devised in analogy to conventional models of cellular automata introduced by von Neumann. Standard solid state QCA cell design considers the distance between quantum dots to be about 20 nm, and a distance between cells of about 60 nm. Just like any CA, Quantum (-dot) Cellular Automata are based on the simple interaction rules between cells placed on a grid. A QCA cell is constructed from four quantum dots arranged in a square pattern. These quantum dots are sites electron can occupy by tunnelling of them.

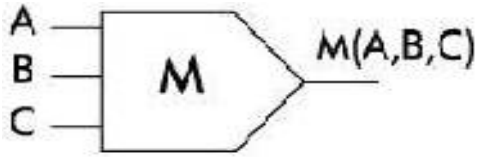


Fig 2: Structure of Majority gate

The QCA majority gate performs a three-input logic function. Assuming the inputs are A, B and C, the logic function of the majority gate is

$$M=AB+BC+CA$$

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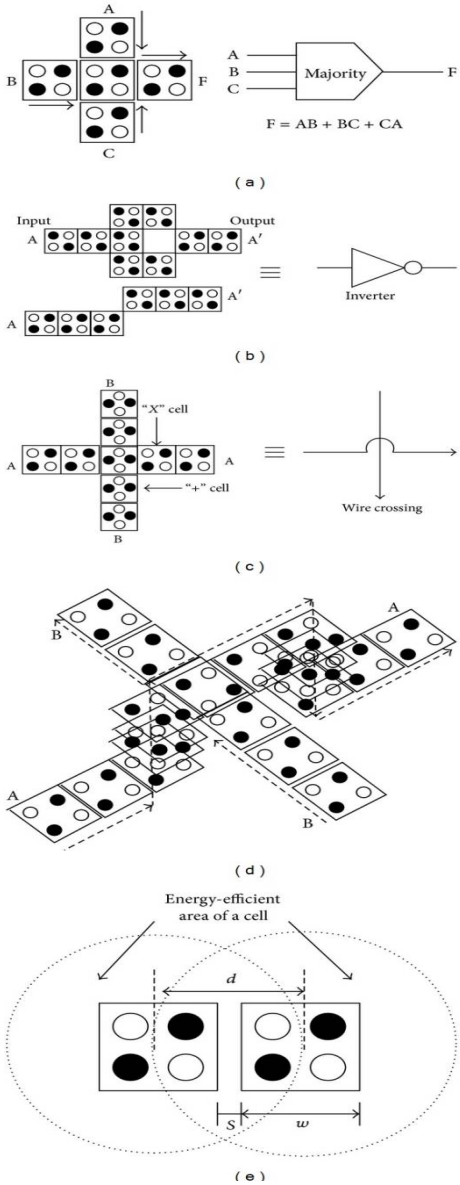


Fig 3:(a) Majority voter, (b) inverter, (c) coplanar wire crossing, (d) multilayer wire crossing and(e) area under induced effect of majority cell

The basic structure realized with QCA is the 3-input majority gate, M(A, B, C) = AB + BC + CA (Figure 2(a)). The majority gate can also function as a 2-input AND or a 2-input OR by fixing one of the three input cells to $P = -1$ or $P = 1$, respectively. Inversion can be done within the wire by slightly off-centring the wire. Thus, it is realized in two different orientations as shown in Figure 2(b). In, the constraints imposed by the radius of effect of each cell are described which defines the distance *d* that can affect the operation of certain structures in QCA array. That is, two in-line QCA cells interact if d=dN=w+s,

Where ***w*** is the width (and height) of (square) cell and *s* is the measure of separation between two consecutive cells

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(Figure 3(e)). The other different radius of effect for nearest diagonal/next to neighbour is described.

In QCA, two kinds of QCA wire crossings are possible to be found, like coplanar (Figure 2(c)) and multilayer (Figure 2(d)). Coplanar wire crossing in QCA requires two different orientations, a 90° (×−cell) and a 45° (+−cell) structure whereas multilayer wire crossing has no such strict orientation limit. A multilayer crossover is quite straightforward from the design perspective and the signal connection is steadier. The probability of undesirable crosstalk between any two crossing lines can be avoided by introducing multilayer wire crossing. Also, in a coplanar crossing, there is a possibility of a loose binding of the signal which causes a discontinuity of the signal propagation, and there is the possibility of back propagation from the far side constant input. So putting enough clock zones between the regular cells across the rotated cells is required. In this paper, all the designs are established mostly on multilayer wire crossing.

## IIIDESIGN OF EFFICIENT FULL ADDER

The most important mathematical operation is addition. Other operations such as subtraction, multiplication, and division are usually implemented by adders. So an efficient adder can be of great assistance in designing arithmetic circuits. Recently, it is shown that 1-bit full adder can be realized with 3 majority gates and one inverter [24]. The total circuit delay is of 1 clock a (4 clock zones) for generating the outputs.

In order to minimize the number of majority gates and inverters, a multilayer design using 5-input majority gate is proposed here (Figure 3). A five-input majority gate is a Boolean gate whose output is 1 only if 3 or more of its inputs is 1. The Boolean function of a five-input majority gate is F(A, B, C, D, E) = ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + BDE + CDE. A 3-input majority has been implemented using only one design to date. However, a 5-input majority gate can be implemented using various designs. The block diagram of our proposed 5-input majority gate is as shown in Figure 3(b). QCA cell layout and its simulation of 5 input majority voter is shown in Figure 4. The comparative analysis establishes that this structure is more compact than the other reported 5-input majority gate designs (Table 1). This gate covers 0.0096 $\mu m^2$ and uses the least clock zone required.

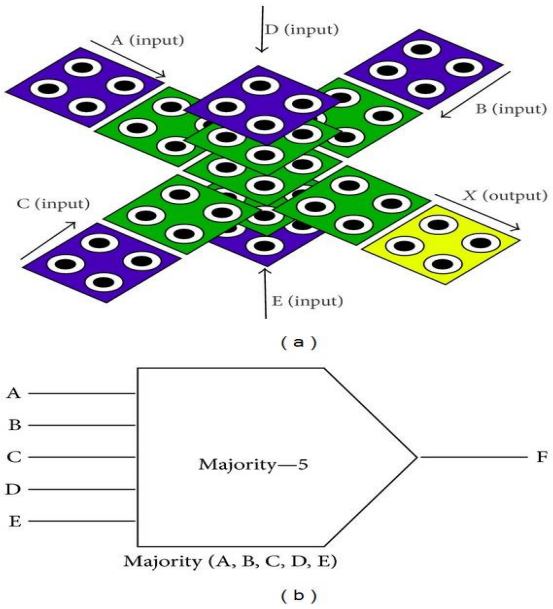


Fig 4: Block diagram of five-input majority gate.

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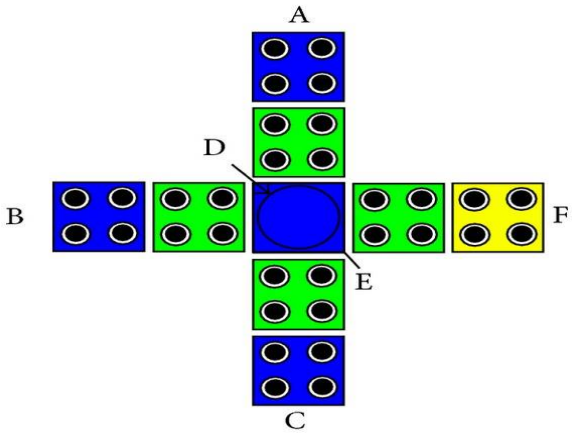
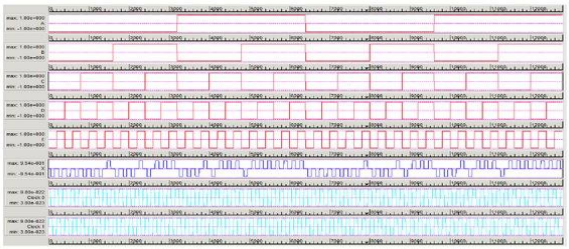
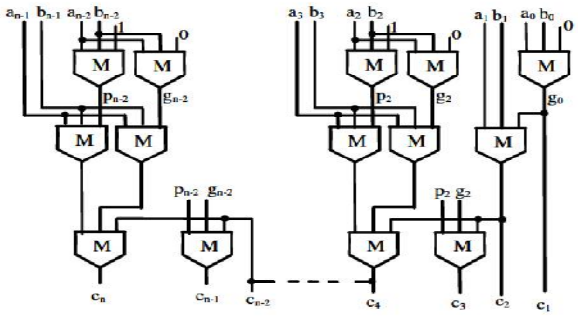



( a )



( b )

Fig 5:QCA cell layout and its simulation result of five-input majority gate




(a)

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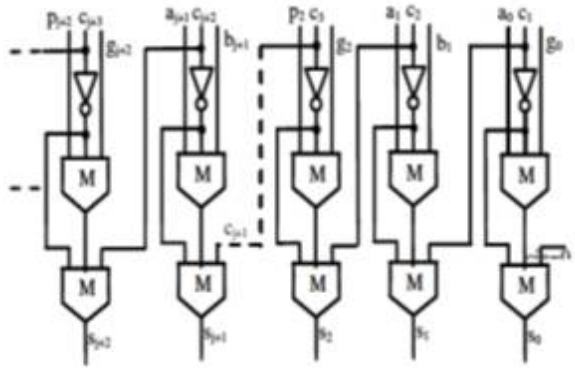

(b)

Fig 6: Novel *n*-bit adder (a) carry chain and(b) sum block.

We have assumed that the carry-in of the adder is cin=0 , the signal p0 is not required and the 2-bit module used at the least significant bit position is simplified.

It must be noted that the addition is performed when a carry is generated at the least significant bit position (i.e., g0=1) and then it is propagated through the subsequence bit positions to the most significant bit.

To introduce the novel architecture proposed for implementing ripple adders in QCA, let consider two *n*-bit addends $A = an-1, \ldots, a0$ and $B = bn-1, \ldots, b0$ and suppose that for the *i* th bit position (with $i = n - 1, \ldots, 0$) the auxiliary propagate and generate signals, namely $pi = ai + bi$ and This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.$gi = ai \cdot bi$ , are computed. *ci* being the carry produced at the generic $(i-1)$th bit position, the carry signal $ci+2$,furnished at the $(i+1)$the bit position.

## IV. SIMULATION RESULTS

Below figures represent the simulation result of Quantum-dot Cellular Automata (QCA) based Full Adder Circuit RTL and Technical Schematic Diagram and result analysis performance based on different logical input.

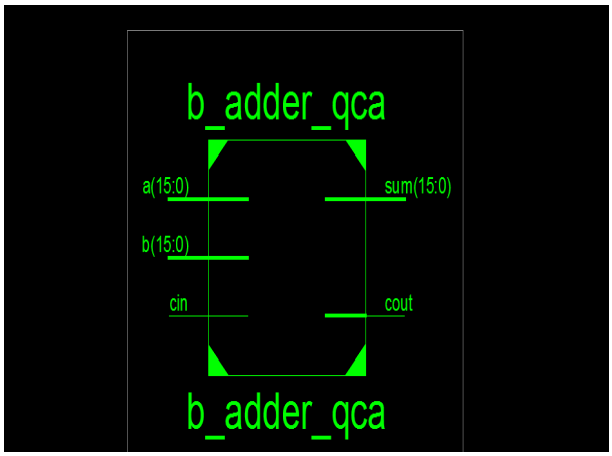


Fig 7: Basic RTL diagram of binary adder

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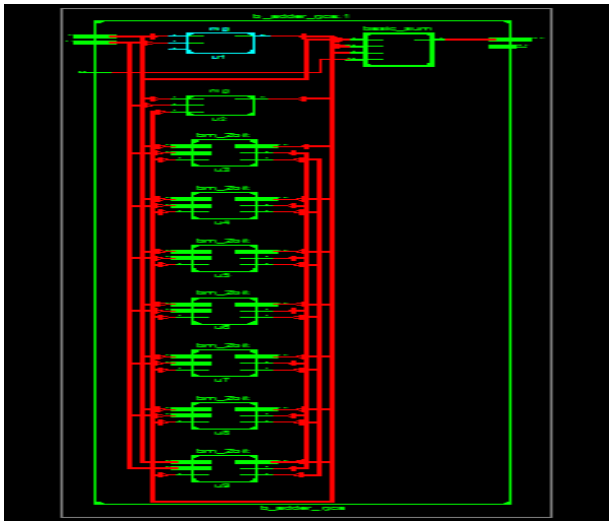

Fig 8: RTL schematic of binary adder

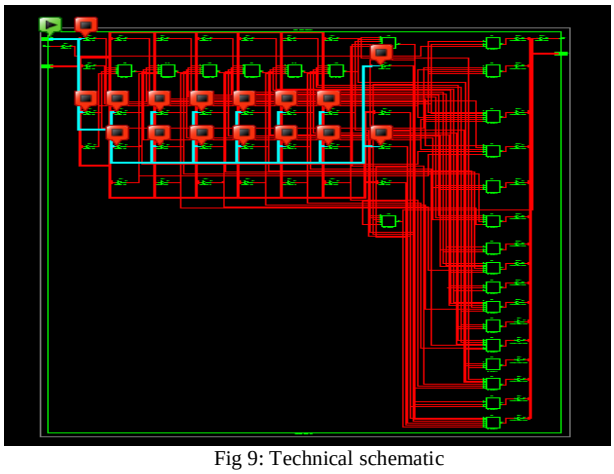

Fig 9: Technical schematic

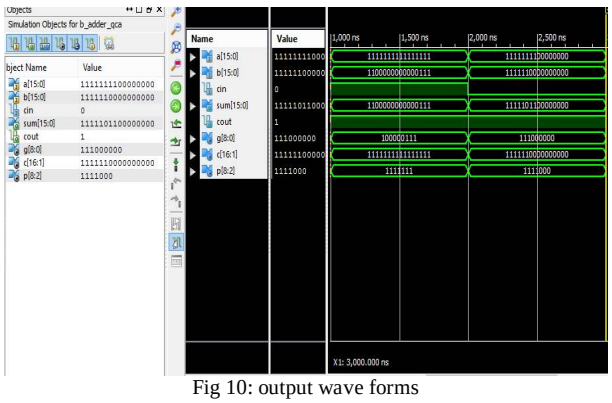

Fig 10: output wave forms

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## V. CONCLUSION

In this paper presents schematic approach to design and implement binary adder. In QCA to achieve high speed, low power, and low area. We also constructing an optimize n-bit adder circuit.

## VI. FUTURE SCOPE

We generated 16-bit binary adder in QCA. Future scope is that to generate 32-bit binary adder and 128-bit binary adder in QCA by using Xilinx software.

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## BIOGRAPHY

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