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Design and Implementation of Low Power FFT Processor for OFDM Wireless Communication

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ABSTRACT: Recently digital signal processing has received high attention due to the advancement in multimedia and wireless communication, The FFT processor is the most speed critical part in the multi-carrier orthogonal frequency division multiplexing (OFDM) communication system. The FFT (fast Fourier transform) processor is the most speed and power consumption critical part in the orthogonal frequency division multiplexing (OFDM) communication system , In these systems, low power is usually one of the major concerns. Accordingly Orthogonal Frequency Division Multiple Access (OFDM) technique based on Time Division Duplex (TDD) is an attractive technology for high data rate wireless access in multi channel communication, The modulation and demodulation of OFDM are done by Fast Fourier Transform (FFT) and Inverse Fast Fourier Transform (IFFT) respectively. The FFT (fast Fourier transform) processor is the most speed and power consumption critical part in the orthogonal frequency division multiplexing (OFDM) communication system we also propose a design new FFT algorithm for the implementation of multiplier that is to be used in radix 2^5 512-point

I. INTRODUCTION

The Fast Fourier Transform (FFT) is one of the most used algorithms in digital signal processing. The FFT, which facilitates the efficient transformation between the time domain and the frequency domain for a sampled signal, is used in many applications, e.g., radar, communication, sonar, speech signal processing.

UWB has became a hot research topic and plenty of research results have been published. Multiband-OFDM standard is one solution for UWB technology. A proposal for Multi-band OFDM UWB standard is published by IEEE 802.15 3a study group [12]. After IEEE 802.15 3a was withdrawn in the Spring of 2006, Multiband-OFDM has been controlled by ECMA International. In December 2007, the second revised version Standard ECMA-368: High Rate Ultra Wideband PHY and MAC Standard' was released, which specified physical layer (PHY) and medium access control layer (MAC) of the UWB technology based on Multiband-OFDM [5]

II. FFT ALGORITHM AND ITS APPLICATION IN OFDM

OFDM principle

There are many books and articles which describe how the orthogonal frequency-division multiplexing (OFDM) system works, such as [20] [3]. Here the FFT and IFFT modulation of OFDM is focused on, which is closely related to our FFT processor design.

2.2 OFDM signal

The fundamental principle of the OFDM concept is to split one high rate data symbol into a set of independent smaller symbols [2]. Each subsymbol is modulated on a separate subcarrier. Meanwhile, these subsymbols are transmitted simultaneously in time domain.

Signal Form Here the OFDM signal formula is directly introduced by Equation

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2.3 Multiband-OFDM for UWB system

Multiband-OFDM is an OFDM specification for UWB [4]. Multiband-OFDM was first proposed by Texas Instruments and was sponsored by Texas Instruments as a member of the Multiband OFDM Alliance, which is now part of WiMedia [22]. In December 2002, IEEE 802.15 3a was set up to develop a high data rate UWB PHY amendment for the IEEE 802.15 3WPAN standard. However, there are two different proposals to operate the wireless UWB, Multiband-OFDM UWB proposed by WiMedia, and Direct Sequence-UWB (DS-UWB), supported by UWB Forum. Because of the disagreements between the two groups, IEEE 802.15 3a was withdrawn. Nevertheless, a proposal for Multi-band OFDM UWB standard is published [12].

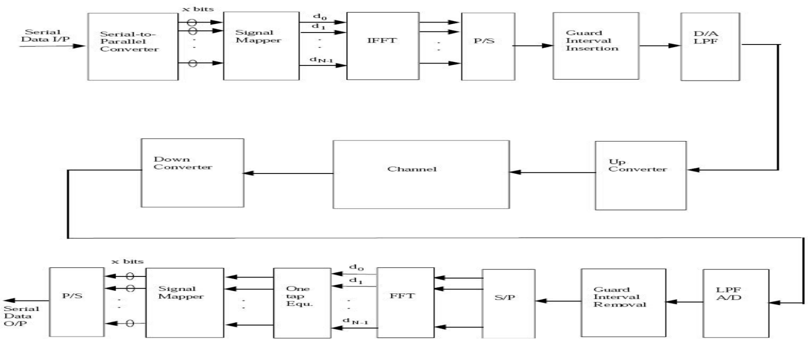

Fig:1.1 The general OFDM System

Fast Fourier Transform with Its Different Algorithms

As shown in the preceding chapter, in MB-OFDM UWB scheme, FFT plays an important role in the total base-band system. Based on the system necessity, 128 point FFT need to be processed by using the proper algorithm and it should be optimal for ASIC application. This chapter emphases on the various algorithms used to realize Fast Fourier Transform. The advantages and disadvantages of these algorithms are also analyzed.

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Improvement and Implementation

From the analysis of that R2[2]SDF needed 528 MHz clock frequency to process the data. As explained in Section 4.2, it is unrealizable for the baseband UWB processor. A novel parallel-pipeline FFT processor structure is suggested based on R2[2]SDF architecture. Clock frequency of proposed structure can be minimized to 157MHz, without any much demand for the chip area. By doing this way, power consumption is dramatically reduced.

To minimize the clock frequency while keeping throughput, most appropriate way is to parallelize butterflies. Parallelism will increase area and the power consumption. Hence, a balance is needed between level of parallelism and area and power consumption concern. By doing the analysis, for the pipeline structure, first stage is most clock-cycle-consuming stage that takes half of the total latency. Hence, only for the first stage, the first try is to parallel the butterflies. Nonetheless, by this, the data will overstock at beginning of second stage.

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The Algorithm Level

By analyzing the radix 2^2 algorithm, it is originate that the input can also be divided into the odd and even parts. These parts are not mixed until last stage. Here, 8 point FFT data flow is used to explain the proposal, as shown in Figure

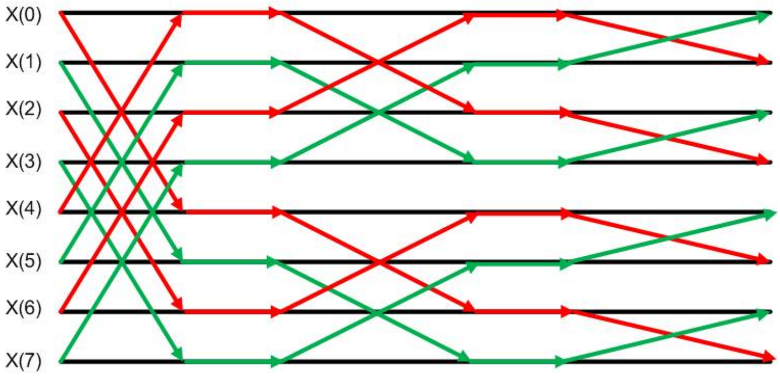

Figure 2.1: Radix 2^2 based parallel FFT algorithm data flow

The red line indicate the even input data flow whereas green line indicate the odd input data flow. In the first and second stage, no cross between red lines and green lines, that means even and odd input data can be independently processed in first and second stages. However, in the last stage, red lines and green lines are crossed that means the even and odd data must be mixed to process. It is clear that twiddle factors are not modified by this parallel algorithm as compared with the Radix 2^2 algorithm. Hence, the same number of multiplication is required. However, because of the parallelism, the position and order of twiddle factor required to be changed. Algorithm data flow based on 128 point parallel Radix 2^2 with the twiddle factor position

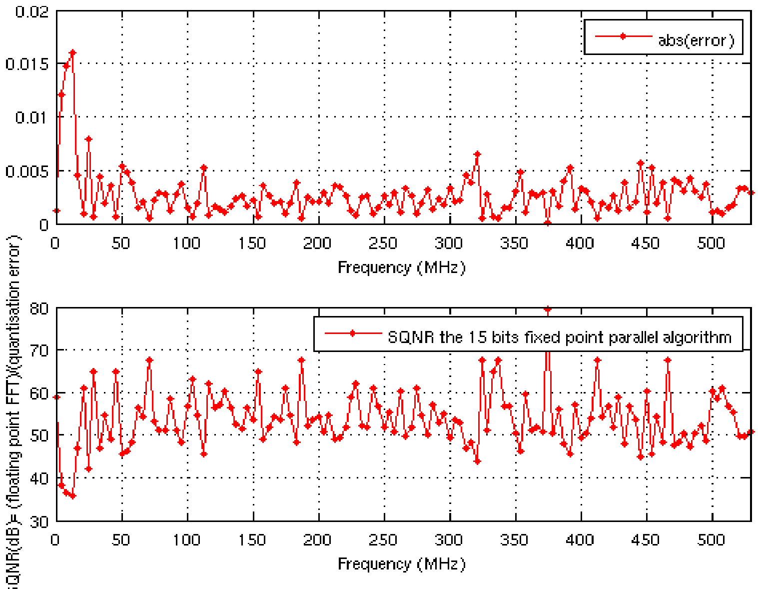

Figure 1.3: Error of 15 bits parallel radix 2^2 algorithm

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III. SIMULATION RESULTS

The errors between modelsim outcomes and Matlab simulation results is shown in Figure 1.4 It shows no error for the proposed FFT processor with Matlab fixed point Radix2^2Parallel simulation that means proposed FFT processor gained the expected accuracy.

The errors between proposed processor and Matlab builtin FFT is sown in figure 1.5 . It shows that SQNR of proposed FFT is above the 40 dB, which is approximately same as fixed point simulation in the Section 2.4. This result obtains the numerical precision requirement.

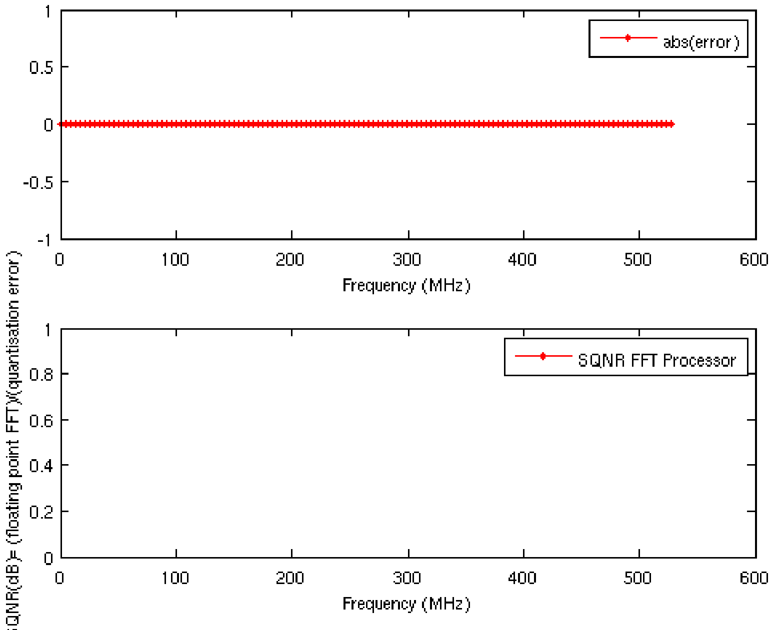

Figure 1.4: Result comparison between processor and the Matlab simulation

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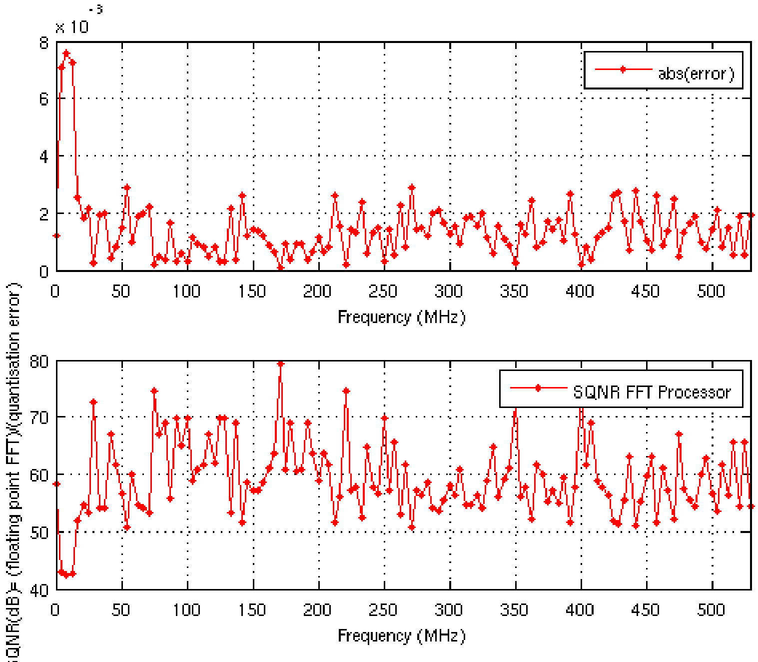

Figure 1. 5 Result comparison between processor and the Matlab built in FFT

IV. CONCLUSION

- Firstly, OFDM and UWB systems are analyzed. The specifications of FFT processor are defined combined with the literature research and the system simulation.
- FFT algorithms are reviewed and analyzed fully based on multiplicative complexity. The purpose is to find most suitable one for the UWB system requirements and the ASIC implementation. It shows that the Radix 2^X algorithms are best ones for the ASIC implementation.

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