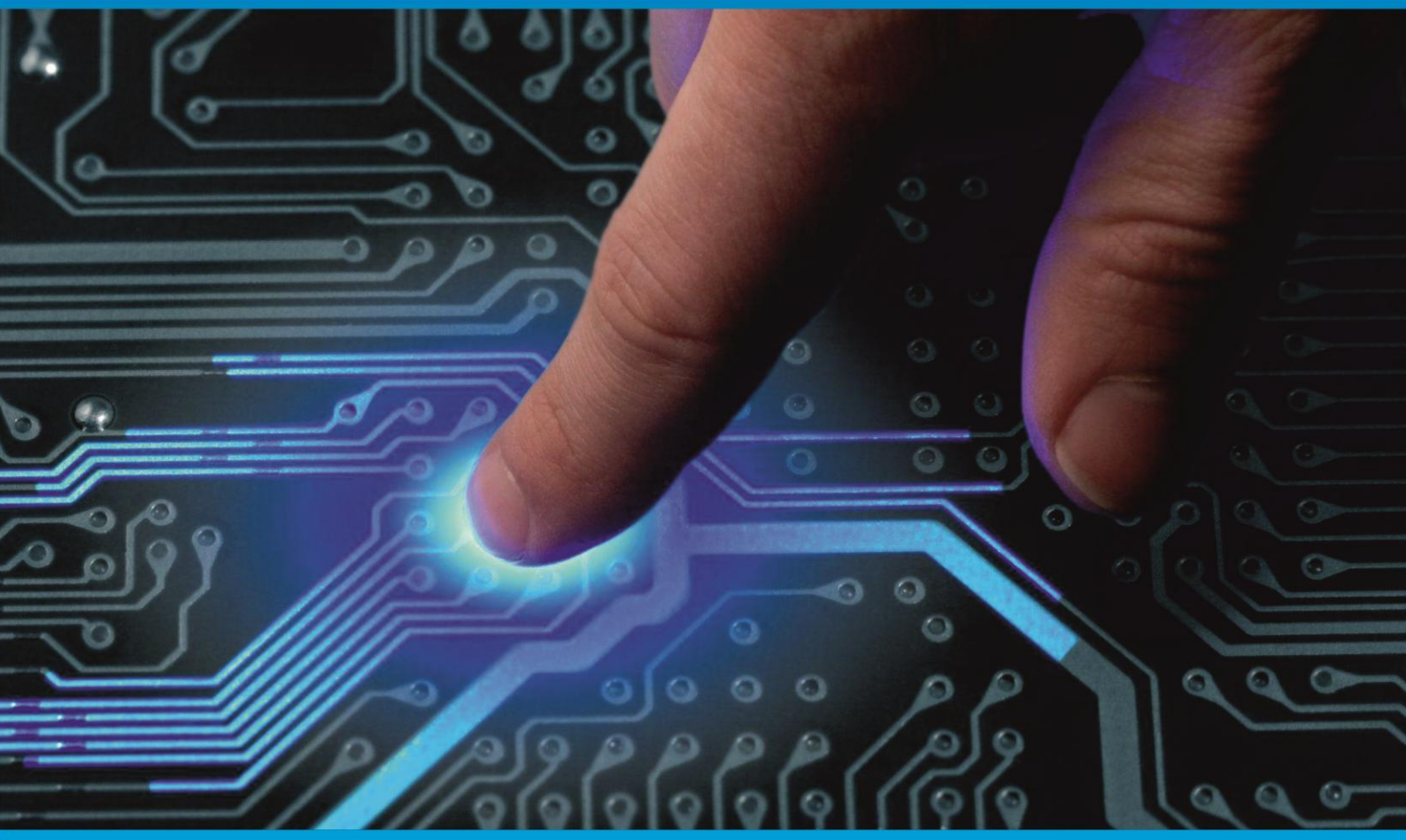
IJIRCCE

e-ISSN: 2320-9801 | p-ISSN: 2320-9798



INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN COMPUTER & COMMUNICATION ENGINEERING

Volume 8, Issue 12, December 2020

INTERNATIONAL STANDARD SERIAL NUMBER INDIA

Impact Factor: 7.488

International Journal of Innovative Research in Computer and Communication Engineering

| e-ISSN: 2320-9801, p-ISSN: 2320-9798| www.ijircce.com | |Impact Factor: 7.488 |

|| Volume 8, Issue 12, December 2020 ||

| DOI: 10.15680/IJIRCCE.2020.0812015 |

SRAM Emulated TCAM Comparator for Minimizing the Area and Working with Optimized Power

Amulothu Devi Vijaya Prasanthi, K Babu Rao

PG Student, Dept. of ECE., Universal College of Engineering & Technology, Dokiparru, Guntur, India

Assistant Professor, Dept. of ECE., Universal College of Engineering & Technology, Dokiparru, Guntur, India

ABSTRACT: Ternary Content Addressable Memories (TCAMs) are widely used in network devices to implement packet classification. They are used, for example, for packet forwarding, for security, and to implement software-defined networks (SDNs). TCAMs are commonly implemented as standalone devices or as an intellectual property block that is integrated on networking application-specific integrated circuits. For very high speed searching applications a technique TCAM (Ternary Content Addressable Memory) is introduced. Associative memory, associative storage and associative array are the synonyms of TCAM. For programming in data structures the name associative array is used most. If the input data is compared with sorted data and result is the matching data address then match hit arises. The objective of the project is to design a lossless data compression system which operates in high-speed to achieve high compression rate, by using architecture of compressor, the data compression rates are significantly improved. Also inherent scalability of architecture is possible. A 32-bit system with memory architecture is based on having data compression engines working on given data.

KEYWORDS: Ternary Content Addressable Memory (TCAMs), Software Defined Networks (SDNs).

I. INTRODUCTION

Nowadays, single event upsets (SEUs) altering digital circuits are becoming a bigger concern for memory applications. Previously there are more an error-detection methods for difference-set cyclic codes with majority logic decoding. Majority logic decodable codes are suitable for memory applications due to their capability to correct a large number of errors. However, they require a large decoding time that impacts memory performance. The proposed fault-detection method significantly reduces memory access time when there is no error in the data read. The technique uses the ternary content addressable memory, which makes the area overhead minimal and keeps the extra power consumption low. Dictionary based schemes copy repetitive or redundant data into a lookup table (such as TCAM) and output the dictionary address as a code to replace the data. The compression architecture is based around a block of TCAM to realize the dictionary. This is necessary since the search operation must be done in parallel in all the entries in the dictionary to allow high and data- independent throughput. There are many applications that could benefit from economical large-capacity TCAM's. Uses for large-capacity associative memories include "smart" databases, memory for Prolog computers, and artificial neural networks. Megabit look-up tables could make hardware dictionary processors commercially feasible, or they could increase resolution and system throughput for motion detection and image compression.

Lossless compression and decompression is the technique, which is used to perform the loss less data compression and decompression operations, which indeed used in the communication systems, to perform the low power data transmitting and receiving. First the clock is given which is used for transmitting and receiving the data within a single clock of positive edge. Input data is driven as a size of 32 bits, and the same output will appear as input using a dictionary technique.

This approach mainly consist of 3 main blocks

1) Compressor 2) De compressor 3) Control

| e-ISSN: 2320-9801, p-ISSN: 2320-9798| www.ijircce.com | |Impact Factor: 7.488 |

|| Volume 8, Issue 12, December 2020 ||

| DOI: 10.15680/IJIRCCE.2020.0812015 |

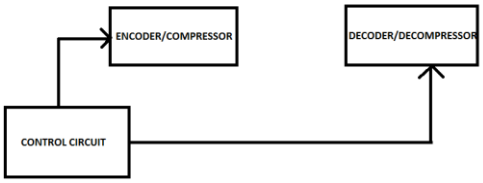


fig 1.1 : Model Diagram

II. INTRODUCTION TO VLSI

Very-large-scale integration (VLSI) is the process of creating integrated circuits by combining thousands of transistor-based circuits into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. The microprocessor is a VLSI device. The term is no longer as common as it once was, as chips have increased in complexity into the hundreds of millions of transistors.

2.1 Overview

The first semiconductor chips held one transistor each. Subsequent advances added more and more transistors, and, as a consequence, more individual functions or systems were integrated over time. The first integrated circuits held only a few devices, perhaps as many as ten diodes, transistors, resistors and capacitors, making it possible to fabricate one or more logic gates on a single device. Now known retrospectively as "small-scale integration" (SSI), improvements in technique led to devices with hundreds of logic gates, known as large-scale integration (LSI), i.e. systems with at least a thousand logic gates. Current technology has moved far past this mark and today's microprocessors have many millions of gates and hundreds of millions of individual transistors.

2.2 VLSI and systems

These advantages of integrated circuits translate into advantages at the system level:

- Smaller physical size. Smallness is often an advantage in itself-consider portable televisions or handheld cellular telephones.

- Lower power consumption. Replacing a handful of standard parts with a single chip reduces total power consumption. Reducing power consumption has a ripple effect on the rest of the system: a smaller, cheaper power supply can be used; since less power consumption means less heat, a fan may no longer be necessary; a simpler cabinet with less shielding for electromagnetic shielding may be feasible, too.

- Reduced cost. Reducing the number of components, the power supply requirements, cabinet costs, and so on, will inevitably reduce system cost. The ripple effect of integration is such that the cost of a system built from custom ICs can be less, even though the individual ICs cost more than the standard parts they replace.

2.3 Applications

- Electronic system in cars.
- Digital electronics control VCRs
- Transaction processing system, ATM
- Personal computers and Workstations
- Medical electronic systems.

International Journal of Innovative Research in Computer and Communication Engineering

| e-ISSN: 2320-9801, p-ISSN: 2320-9798| www.ijircce.com | |Impact Factor: 7.488 |

|| Volume 8, Issue 12, December 2020 ||

| DOI: 10.15680/IJIRCCE.2020.0812015 |

III. COMPRESSOR AND DECOMPRESSOR (32 BITS) BLOCKS EXPLANATION

This approach mainly consist of 3 main blocks.
1.Compressor 2. De-compressor 3. Control

The compressor has the following components.
1.Dram 2.Comparator 3.TCAM

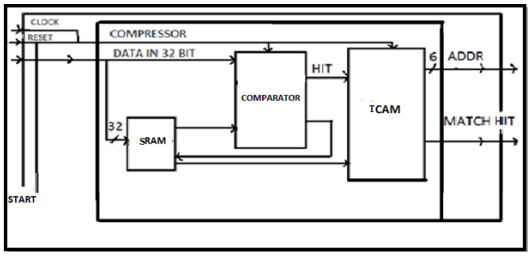


Figure 3.1 : Compressor for 32 bits

3.1 Memory :
Memory circuits can largely be separated into two major groups: dynamic memories that store data for use in a computer system (such as the RAM in a PC); and static memories that store information that defines the operating state of a digital system. Dynamic memory circuits for computer systems have become very specialized, and they will be covered in a later lab. This exercise will present memory circuits that are used to store information about the operating state of a digital system. Many electronic devices contain digital systems that use memory circuits to define their operating state. In fact, any electronic device that can create or respond to a sequence of events must contain memory. Examples of such devices include watches and timers, appliance controllers, gaming devices, and computing devices. If a digital system contains *N* memory devices, and each memory device stores a '1' or a '0', then the system's operating state can be defined by an *N*-bit binary number. Further, a digital system with *N* memory devices must be in one of 2*N* states, where each state is uniquely identified by a binary number created from the collective ternary contents of all memory devices in the system. At any point in time, the binary number stored in its internal memory devices defines the current state of a digital system. Inputs that arrive at the digital system may cause the ternary contents of one or more memory devices to change state (from a '1' to a '0' or vice-versa), thereby causing the digital system to change states. Thus, a digital system state change or state transition occurs whenever the binary number stored in internal memory changes.

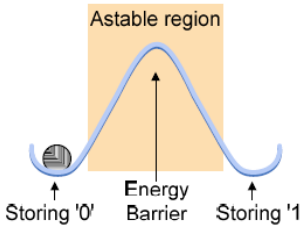


Figure 3.2 Memory States

SRAM: Static Random Access Memory (SRAM).The stored data can be retained indefinitely, without any need for a periodic refresh operation.

- SRAM (static RAM) is random access memory (RAM) that retains data bits in its memory as long as power is being supplied.
- Unlike dynamic RAM (DRAM), which stores bits in cells consisting of a capacitor and a transistor, SRAM does not have to be periodically refreshed. Static RAM provides faster access to data and is more expensive than DRAM.
- SRAM is used for a computer's cache memory and as part of the random access memory digital-to-analog converter on a video card.

| e-ISSN: 2320-9801, p-ISSN: 2320-9798| www.ijircce.com | |Impact Factor: 7.488 |

|| Volume 8, Issue 12, December 2020 ||

| DOI: 10.15680/IJIRCCE.2020.0812015 |

3.2 Comparator:

A comparator is a precision instrument employed to compare the dimension of a given component with a working standard (usually slip gauges).It thus does not measure the actual dimension but indicate how much it differs from the basic dimension. Compares the instantaneous values of two Analog signals and provides logical output to indicate their relative magnitudes (Logic '1'Logic '0' Thus the comparator responds to analog inputs and provides a digital output .

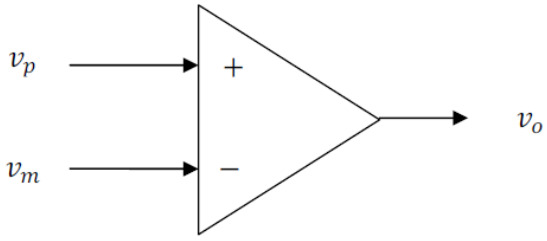


Figure 3.3 Block Diagram of Comparator

Comparator classification by major parameters:

- Propagation delay
- Current consumption
- Output stage type (open collector/drain or push-pull)
- Input offset voltage, hysteresis

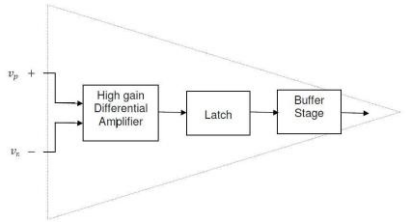


FIGURE 3.4 SCHEMATIC OF COMPARATOR

Ternary TCAMs:

Binary TCAM is the simplest type of TCAM which uses data search words consisting entirely of 1s and 0s. Ternary TCAM (TTCAM) allows a third matching state of "X" or "don't care" for one or more bits in the stored data word, thus adding flexibility to the search. For example, a ternary TCAM might have a stored word of "10XX0" which will match any of the four search words "10000", "10010", "10100", or "10110". The added search flexibility comes at an additional cost over binary TCAM as the internal memory cell must now encode three possible states instead of the two of binary TCAM. This additional state is typically implemented by adding a mask bit ("care" or "don't care" bit) to every memory cell.

A major interface definition for TCAMs and other network search engines (NSEs) was specified in an interoperability agreement called the Look-Aside Interface (LA-1 and LA-1B) developed by the Network Processing Forum, which later merged with the Optical Internetworking Forum (OIF). Numerous devices have been produced by Integrated Device Technology, Cypress Semiconductor, IBM, Broadcom and others to the LA interface agreement. On December 11, 2007, the OIF published the serial look aside (SLA) interface agreement.

| e-ISSN: 2320-9801, p-ISSN: 2320-9798| www.ijircce.com | |Impact Factor: 7.488 |

|| Volume 8, Issue 12, December 2020 ||

| DOI: 10.15680/IJIRCCE.2020.0812015 |

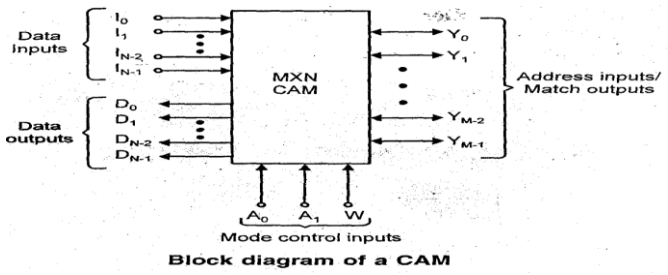


Figure 3.5 :Block diagram of TCAM

TCAM Advantages:

- They associate the input (comparand) with their memory ternary contents in one clock cycle.
- They are configurable in multiple formats of width and depth of search data that allows searches to be conducted in parallel.
- TCAM can be cascaded to increase the size of lookup tables that they can store.
- We can add new entries into their table to learn what they don't know before.
- They are one of the appropriate solutions for higher speeds.

IV. SOFTWARE USED

Xilinx

Xilinx software is used by the VHDL/VERILOG designers for performing Synthesis operation. Any simulated code can be synthesized and configured on FPGA. Synthesis is the transformation of VHDL code into gate level net list. It is an integral part of current design flows

V. RESULTS

5.1 EXISTED DESIGN RESULTS :

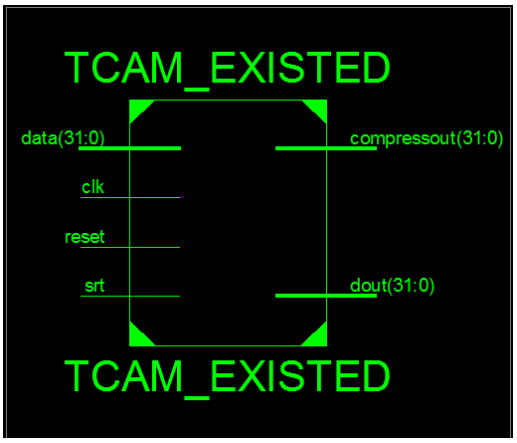


Figure 5.1: RTL schematic

| e-ISSN: 2320-9801, p-ISSN: 2320-9798| www.ijircce.com | |Impact Factor: 7.488 |

|| Volume 8, Issue 12, December 2020 ||

| DOI: 10.15680/IJIRCCE.2020.0812015 |

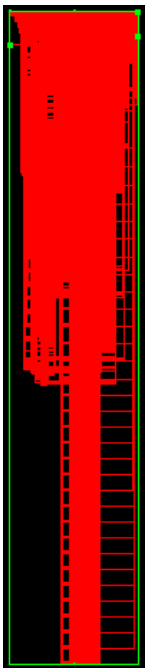


Figure 5.2: View Technology Schematic

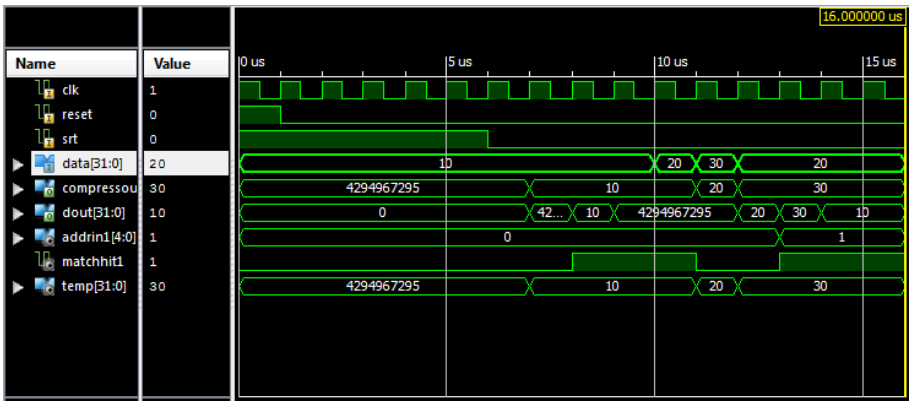


Figure 5.3 : simulated wave forms

5.2 PROPOSED DESIGN RESULTS:

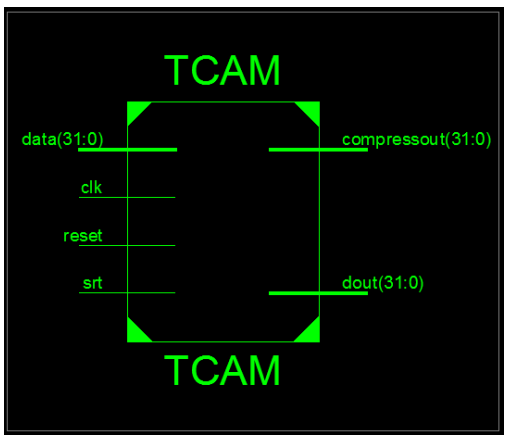


Figure 5.4 : RTL Schematic

| e-ISSN: 2320-9801, p-ISSN: 2320-9798| www.ijircce.com | |Impact Factor: 7.488 |

|| Volume 8, Issue 12, December 2020 ||

| DOI: 10.15680/IJIRCCE.2020.0812015 |

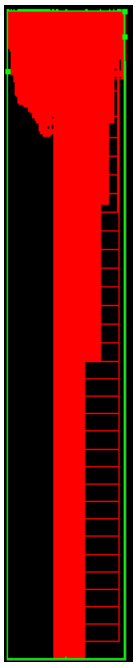


Figure 5.5: View Technology Schematic

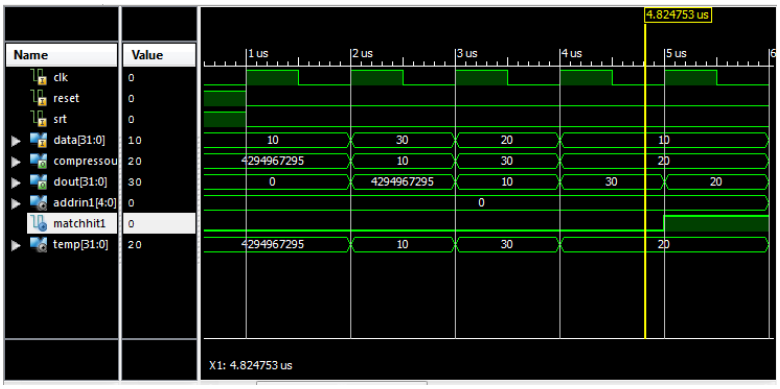


Figure 5.6 : simulated wave forms

Parameter	TCAM with Magnitude comparator	TCAM with Digital Comparator
No of LUTs	1691	1287
Power(mW)	13.801	10.503

Table 5.1 : Parameter Comparison Table

| e-ISSN: 2320-9801, p-ISSN: 2320-9798| www.ijircce.com | |Impact Factor: 7.488 |

|| Volume 8, Issue 12, December 2020 ||

| DOI: 10.15680/IJIRCCE.2020.0812015 |

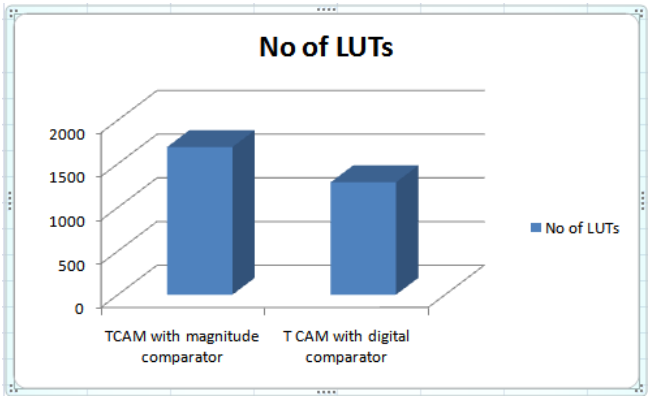


Figure 5.7:LUTs comparison bar graph

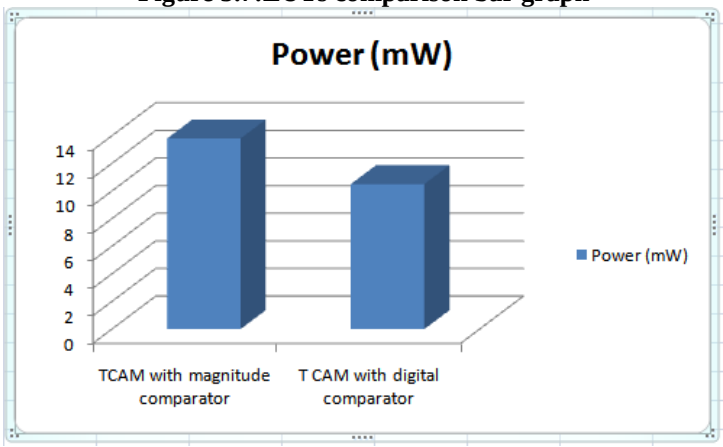


Figure 5.8:Power Comparison Bar Graph

VI. CONCLUSION

In this project, the proposed TCAM using digital comparator and SRAM is better than the existing TCAM using magnitude comparator. From the table 2 the proposed design which is nothing but TCAM with digital comparator uses less LUTs 1287 when compared with the existing design TCAM with magnitude comparator with an LUTs count of 1691.At the same time the power consumed for the proposed design is 10.503mW which is far better than the existing design power consumption with a value of 13.801mW, those are shown in table2. TCAM is a application specific design in which the input data is stored in SRAM memory sequentially from the entered first and fore inputs from the reset. Every input data is sent to comparator in which comparison is done with present and previous inputs (in memory).if any repetition of input data, match hit(when TCAM comparator output is 1) arises. Where the creating of new sorting data is replaced by the previously stored data address by which area is minimized and design is working with optimized power. Based on this functionality, design has verified. The functionality is simulated using Xilinx tool.

REFERENCES

[1] N. Kanekawa, E. H. Ibe, T. Suga, and Y. Uematsu, *Dependability in Electronic Systems: Mitigation of Hardware Failures, Soft Errors, and Electro-Magnetic Disturbances*. New York, NY, USA: Springer-Verlag, 2010.
[2] J. L. Autran *et al.*, "Soft-errors induced by terrestrial neutrons and natural alpha-particle emitters in advanced memory circuits at ground level," *Microelectron. Rel.*, vol. 50, no. 9, pp. 1822–1831, Sep. 2010.
[3] A. L. Silburt, A. Evans, I. Perryman, S. J. Wen, and D. Alexandrescu, "Design for soft error resiliency in Internet core routers," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 6, pp. 3551– 3555, Dec. 2009.
[4] A. Evans, S.-J. Wen, and M. Nicolaidis, "Case study of SEU effects in a network processor," in *Proc. IEEE Workshop Silicon Errors Logic-Syst. Effects (SELSE)*, Mar. 2012, pp. 1–7.

| e-ISSN: 2320-9801, p-ISSN: 2320-9798| www.ijircce.com | |Impact Factor: 7.488 |

|| Volume 8, Issue 12, December 2020 ||

| DOI: 10.15680/IJIRCCE.2020.0812015 |

[5] C. L. Chen and M. Y. Hsiao, "Error-correcting codes for semiconductor memory applications: A state-of-the-art review," *IBM J. Res. Develop.*,vol. 28, no. 2, pp. 124–134, Mar.1984.
[6] K. Pagiamtzis and A. Sheikholeslami, "Ternary content-addressable memory (TCAM) circuits and architectures: A tutorial and survey," *IEEE J.Solid-State Circuits*, vol. 41, no. 3, pp. 712–727, Mar. 2006.
[7] F. Yu, R. H. Katz, and T. V. Lakshman, "Efficient multimatch packet classification and lookup with TTCAM," *IEEE Micro*, vol. 25, no. 1, pp. 50–59, Jan./Feb. 2005.
[8] P. Bosshart *et al.*, "Forwarding metamorphosis: Fast programmable match-action processing in hardware for SDN," in *Proc. ACM SIGCOMM*, 2013, pp. 99–110.
[9] I. Syafalni, T. Sasao, and X. Wen, "A method to detect bit flips in a soft-error resilient TCAM," *IEEE Trans. Comput.-Aided Design Integr.Circuits Syst.*, vol. 37, no. 6, pp. 1185– 1196, Jun. 2018.
[10] S. Pontarelli, M. Ottavi, A. Evans, and S. Wen, "Error detection in ternary TCAMs using Bloom filters," in *Proc. Design, Automat. Test Eur. Conf. Exhib. (DATE)*, Mar. 2013, pp. 1474–1479.
[11] N. Zilberman, Y. Audzevich, G. A. Covington, and A. W. Moore, "NetFPGA SUME: Toward 100 Gbps as research commodity," *IEEEMicro*, vol. 34, no. 5, pp. 32–41, Sep./Oct. 2014.

INNO SPACE

SJIF Scientific Journal Impact Factor

Impact Factor:
7.488

ISSN INTERNATIONAL STANDARD SERIAL NUMBER INDIA

निस्केयर NISCAIR

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN COMPUTER & COMMUNICATION ENGINEERING

9940 572 462 6381 907 438 ijircce@gmail.com

www.ijircce.com

Scan to save the contact details