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Design and Analysis of D Flip Flop Using Different Technologies

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ABSTRACT : The field of digital electronics has been directly towards to the low power digital system. The use of very large scale integration technology in high performance computing, wireless communication, consumer electronics has been rising at a very fast rate. The challenge for VLSI technology is growing in leakage power consumption. Wide utilizations of memory storage systems in modern electronics triggers a demand for high performance and low area implementation of basic memory component and one of the most state holding element is D Flip Flop. In this paper analysis of power, delay, area and power delay product is done for D flip flop using different technologies like static CMOS, C^2MOS, POWER PC, GDI MUX, TSPC, etc. Low power Flip flops are useful for the design of low power digital system. The analysis and the comparison is done using TANNER EDA Tool at 130nm Technology.

KEYWORDS: Low power, CMOS, C^2MOS, ,GDI MUX,TSPC, D Flip Flop, POWER PC

I. INTRODUCTION

In the past, the major concerns of vlsi designers were area, cost, performance and reliability. Low power dissipation became a highly design concern and become more important as we move to all mobile computing and communications. The latest advancement in computing technology has set up a goal for high performance with low power consumption for vlsi designers. Flip flops are important state holding and timing elements in digital circuits. The performance of D flip flop is much important to conclude the performance of the whole circuit. With increasing use of mobile devices, consumer electronics market demands a stringent constraint on reducing power consumption. Designers are striving for small area, low power and higher speed due to increasing demand of portable devices. Several researchers have worked on flip flops but they focus on one or few types of flip flops and applications. The need for comparing different design is the main motive of this paper. In this D flip flop is designed by using different techniques like Static CMOS, C^2mos(clocked cmos).GDI MUX,DSTC,POWER PC and TSPC etc by using130nm and simulations is done using Tanner EDA.

II.REGIONS OF FLIP FLOP OPERATION

There are three regions of flip flop operation and in which one is acceptable for functioning correctly. The regions are as follows:-

- Stable Region-In this region the set up and hold time of a flip flop are met and in this the clock to Q delay is not dependent to D to clock delay.
- Metastable region- in this region as D to clock delay is decreases at a certain point the clock to Q delay rising and ends to failure, which are difficult to debug in real circuits.
- Failure Region-In this region the changes in data are unable to be transferred to the output of the flip flop.

In this the stable region is the required region for the operation of flip flop. Figure 1 shows the regions of the flip flop.

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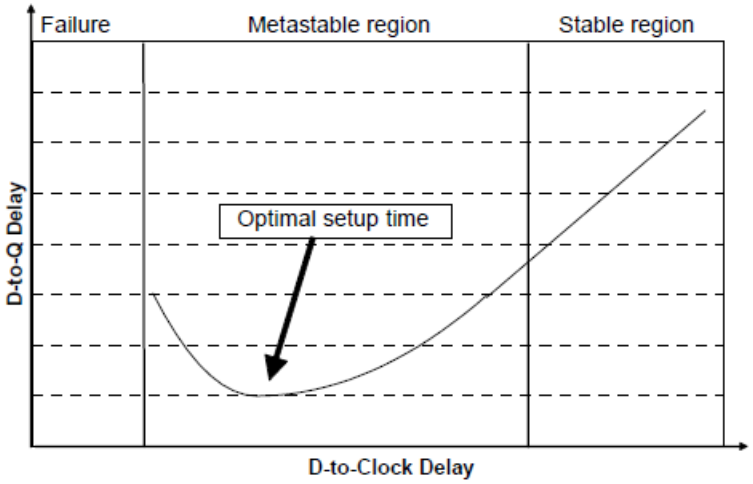

Fig.1-Operation regions of DFF

II. IMPLEMENTATION OF D FLIP FLOP USING DIFFERENT TECHOLOGIES

A. **Static CMOS (complementary metal oxide semiconductor)-**It consist of nMOS pull down and pMOS pull up transistors together in a complementary way. The circuit diagram of Static CMOS based DFF as follows in figure 2.

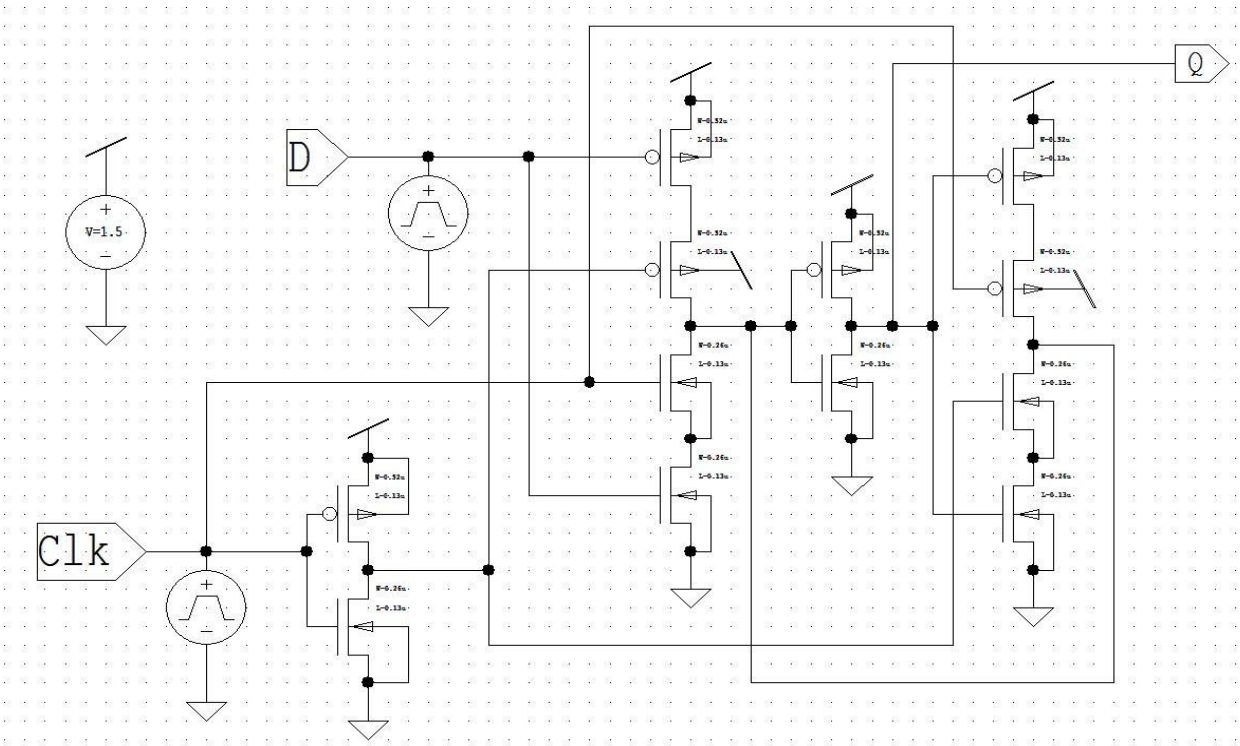

Fig.2- DFF implementation circuit using Static CMOS

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In this circuit 1.5 v voltage is used and simulated using Tanner EDA at 130nm Technology. The output waveform of Static CMOS Based DFF is shown Figure 3.

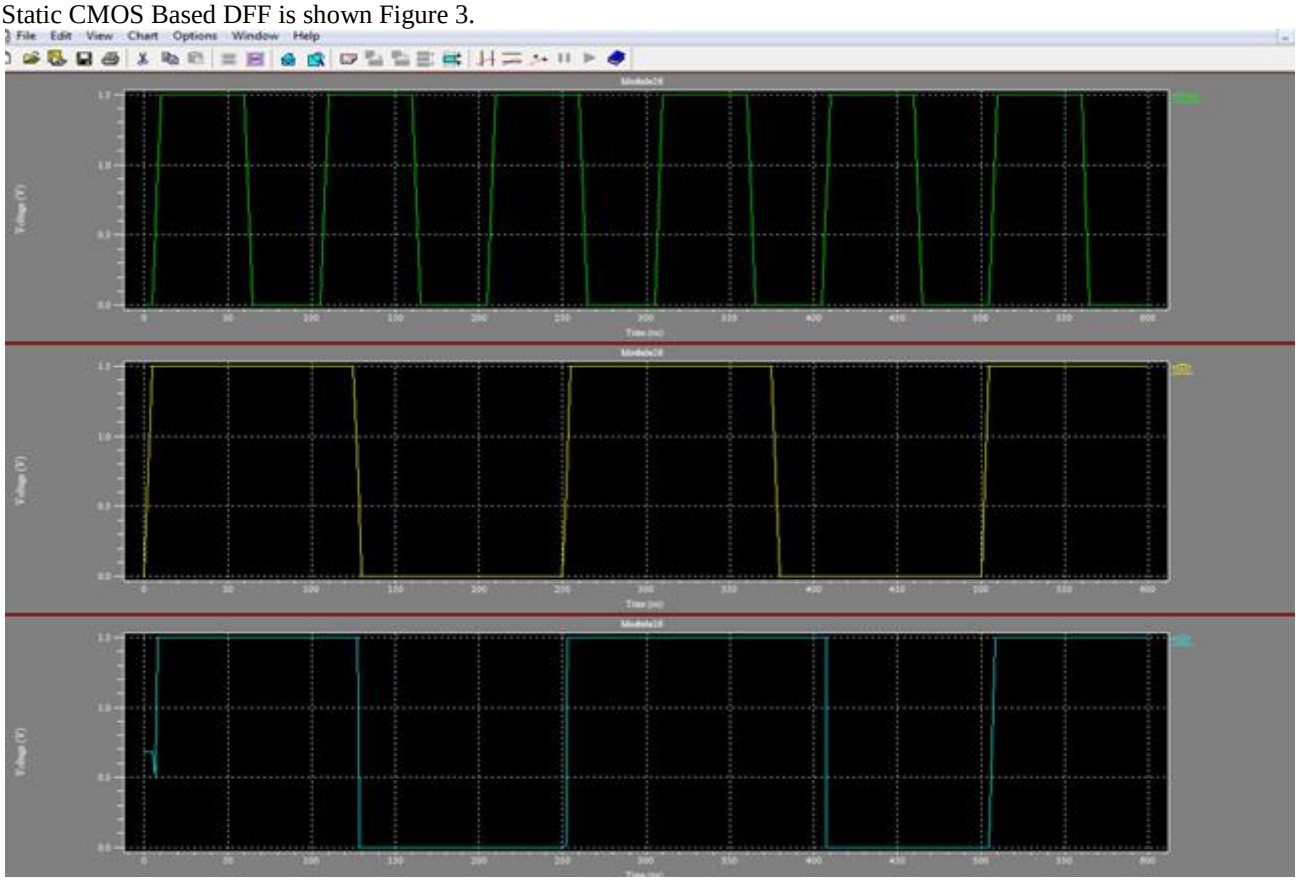

Fig.3-Output waveform of Static CMOS based DFF

B.C^{2}MOS(Clocked CMOS) Based D Flip flop- clocked cmos is composed of a static logic circuit with tristate output network (made up of FET's M1 and M2) that is controlled by Ø and Ø bar. When Ø=0 both M1 and M2 are active and become a standard static logic state. And when Ø=1 both M1 and M2 are cut off as shown in figure 4.

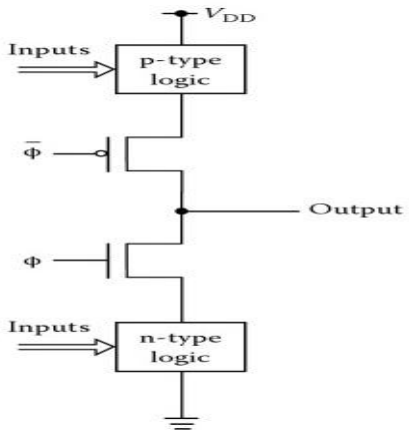

Fig.4-Clocked CMOS logic

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The schematic diagram of implementation of D flip flop using clocked CMOS is shown in figure 5 .

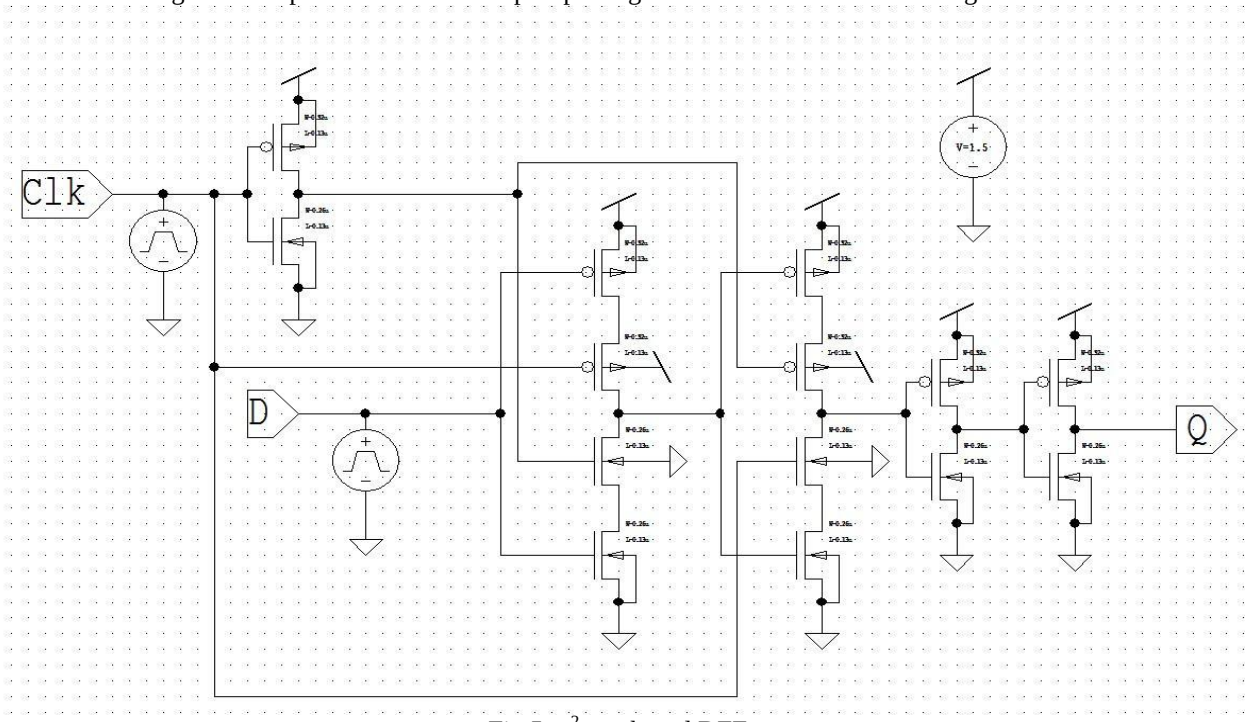

Fig.5- c^{2}mos based DFF

The output waveform of Clocked CMOS based D flip flop is shown in Figure.6

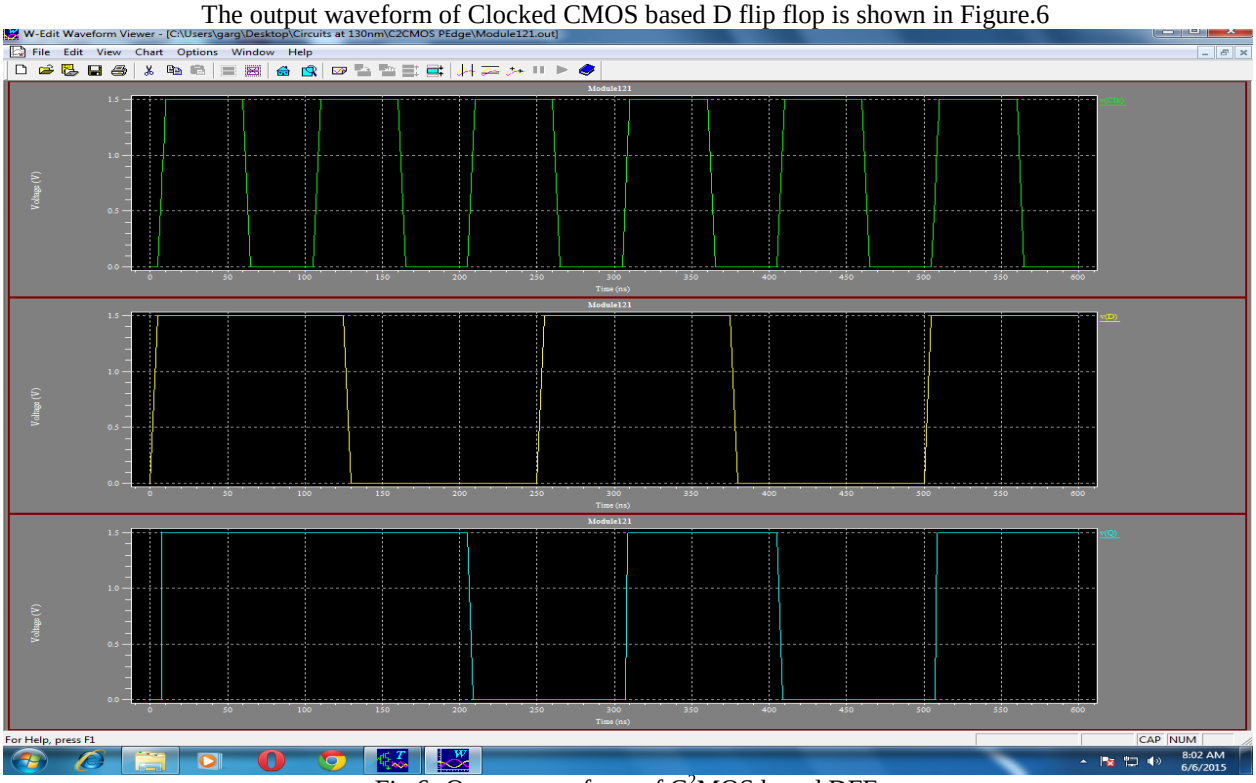

Fig.6.-Output waveform of C^{2}MOS based DFF

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C.GDI MUX (Gate Diffusion Input Multiplexer)- GDI multiplexers are composed of single pair of transistors and cross coupled pair of Invertors. First multiplexer is connected to the system clock and its inputs are connected to D input and feed back loop. The schematic diagram of GDI MUX based D Flip Flop is shown in figure 7.

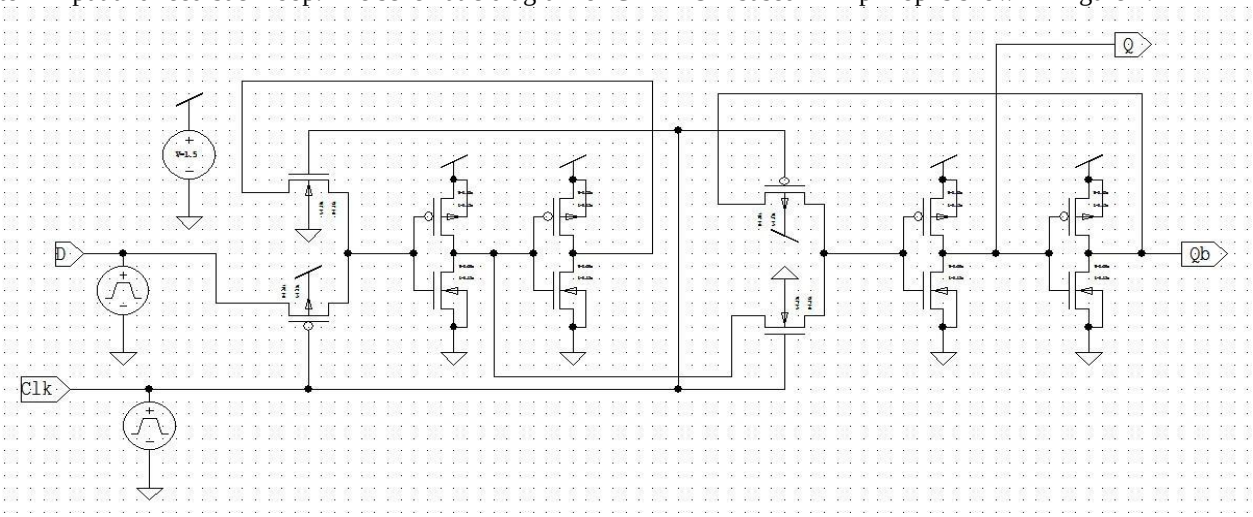

Fig.7-GDI MUX based DFF

This topology creates a Positive edge triggered flip flop with reduced propagation delay. The output waveform of GDI MUX based DFF is shown in figure 8.

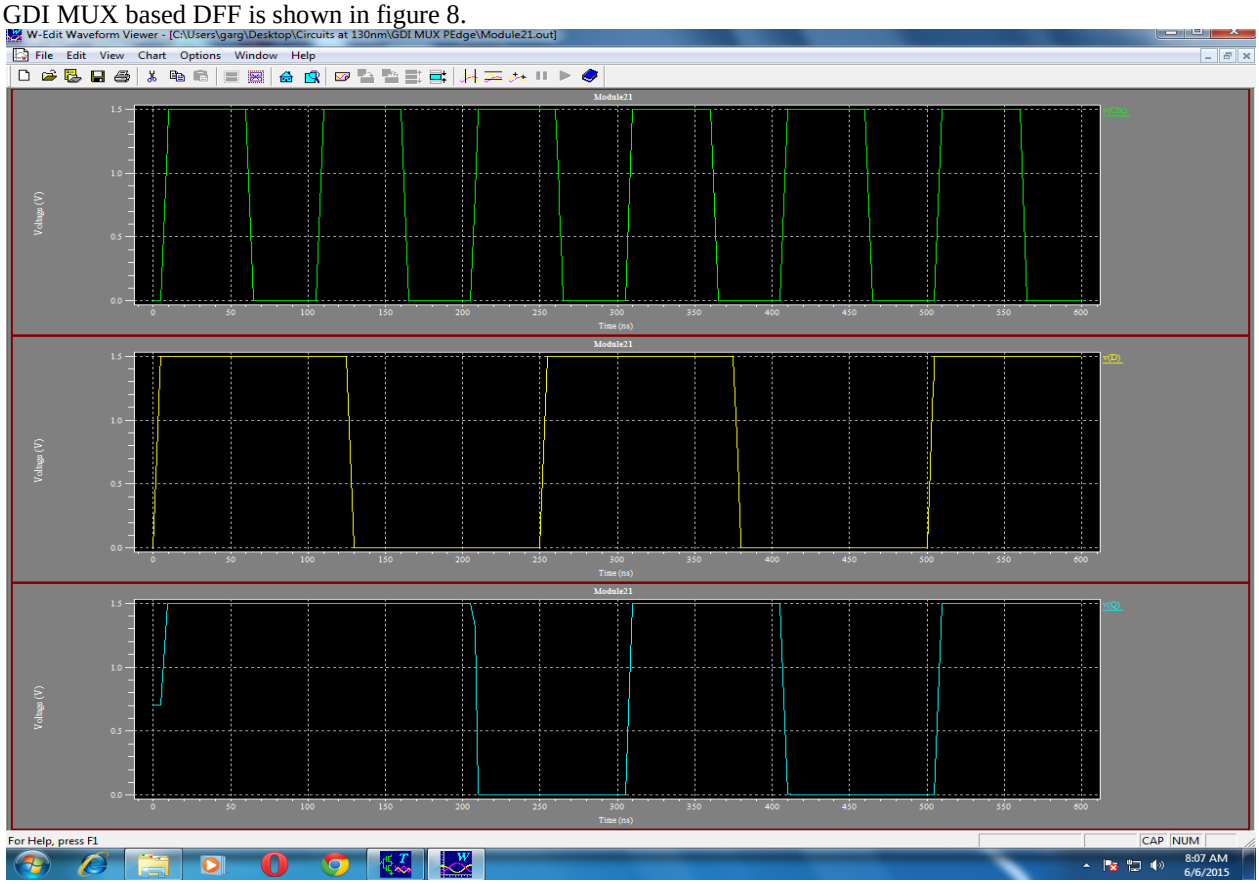

Fig.8-Output waveform of GDI MUX based DFF

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D. POWER PC-The main advantage of POWER PC D flip flop is short circuit path and low power feedback.The circuit diagram of D Flip flop using POWER PC is shown in figure 9.

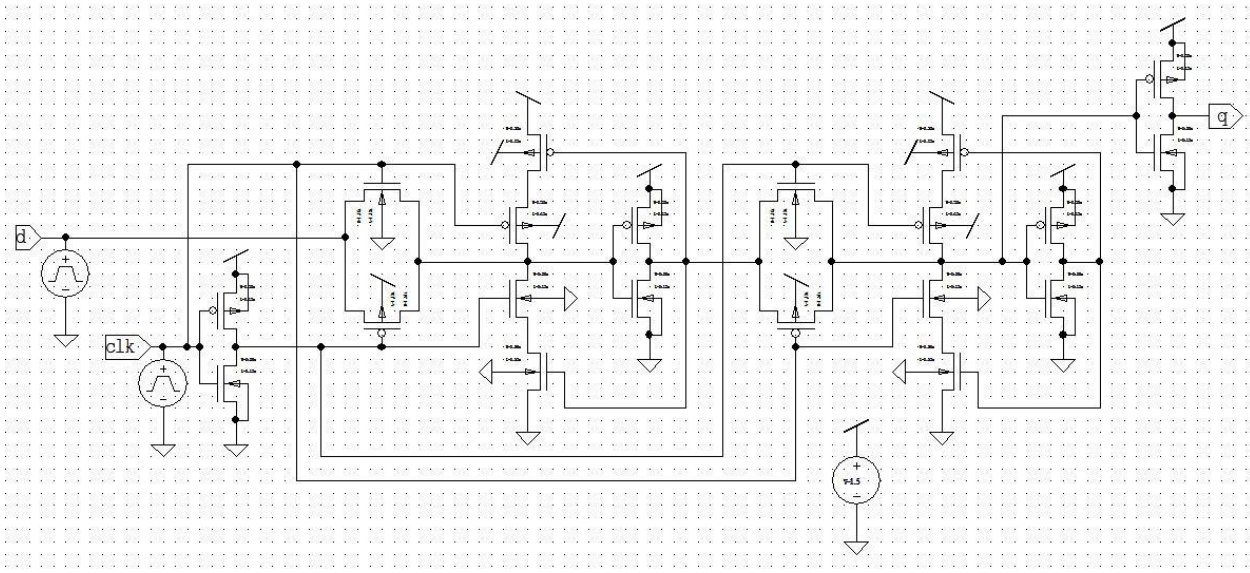

Fig.9- POWER PC based DFF

The output waveform of POWER PC based DFF is shown below in figure 10.

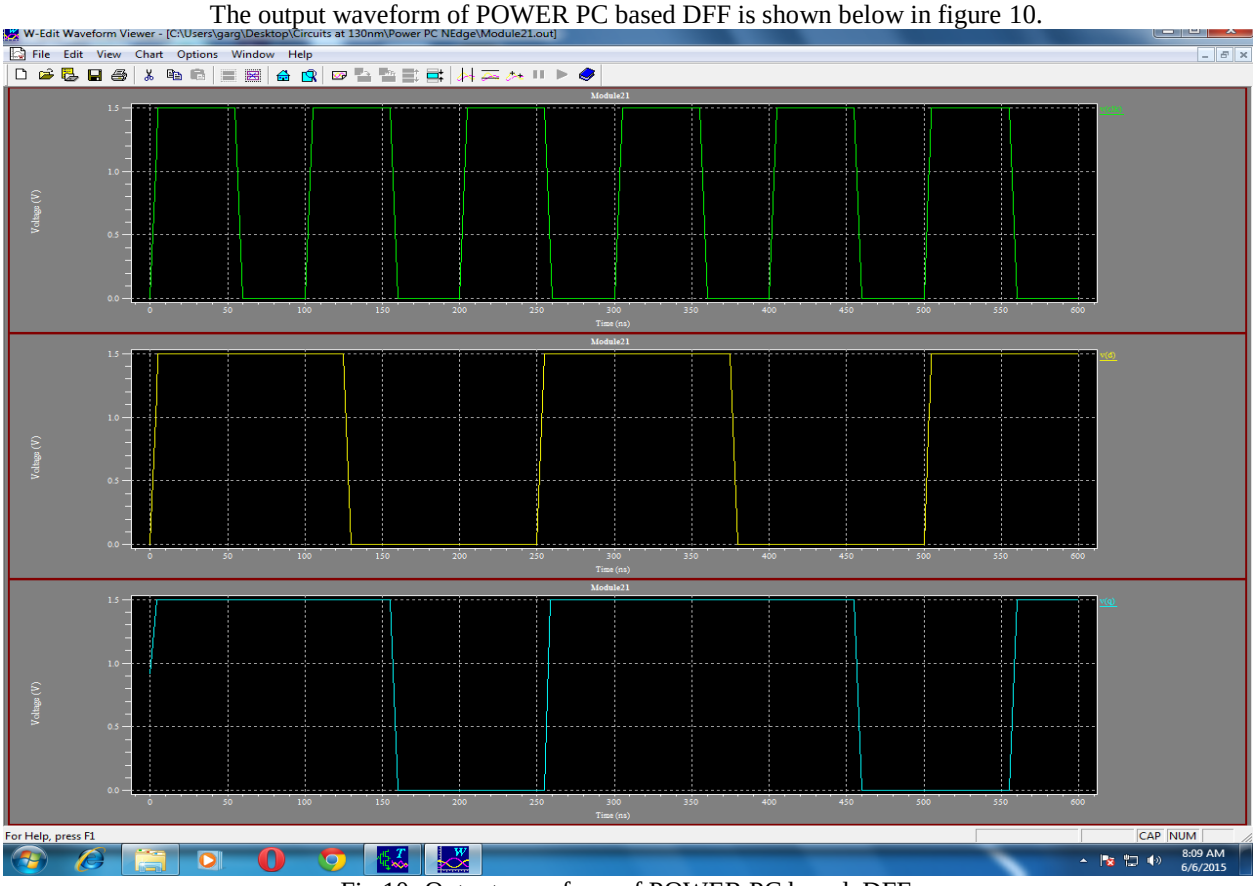

Fig.10- Output waveform of POWER PC based DFF

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E. TSPC (True single phase clocked)- In TSPC logic we have only clock and do not need an inverted clock. These techniques eliminate skew problems due to different clock phases. The circuit diagram of TSPC based D flip flop is shown in figure 11.

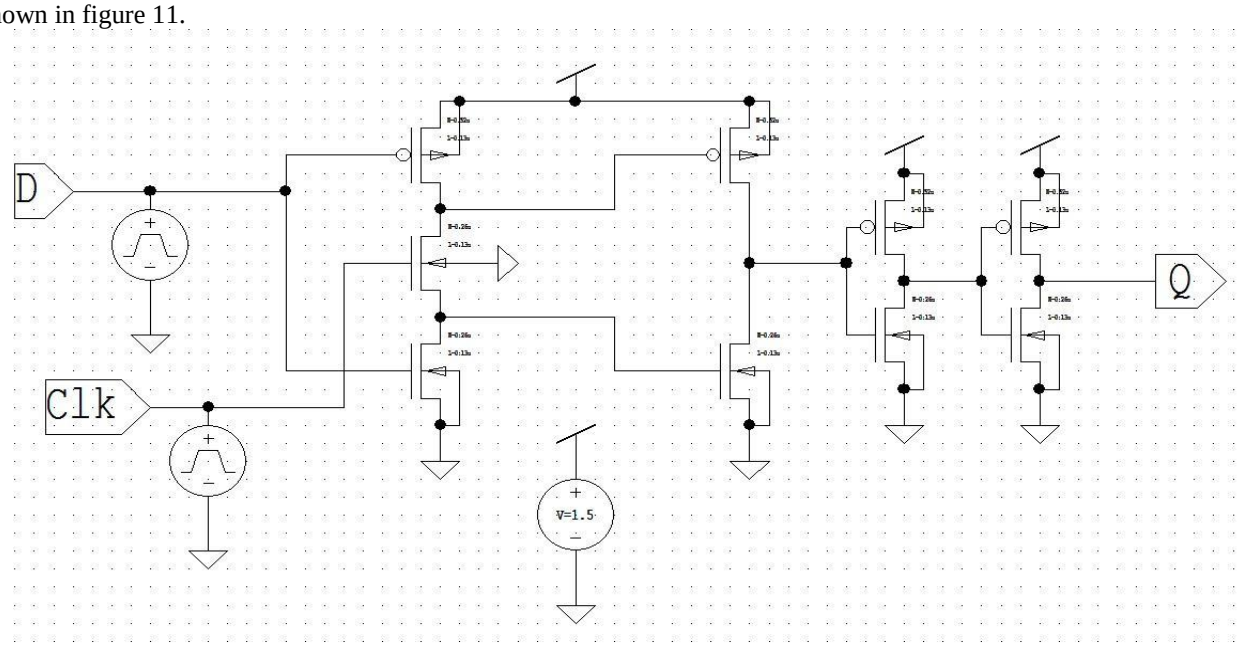

Fig.11- TSPC based DFF

The output waveform of TSPC based D flip flop is shown in figure 12.

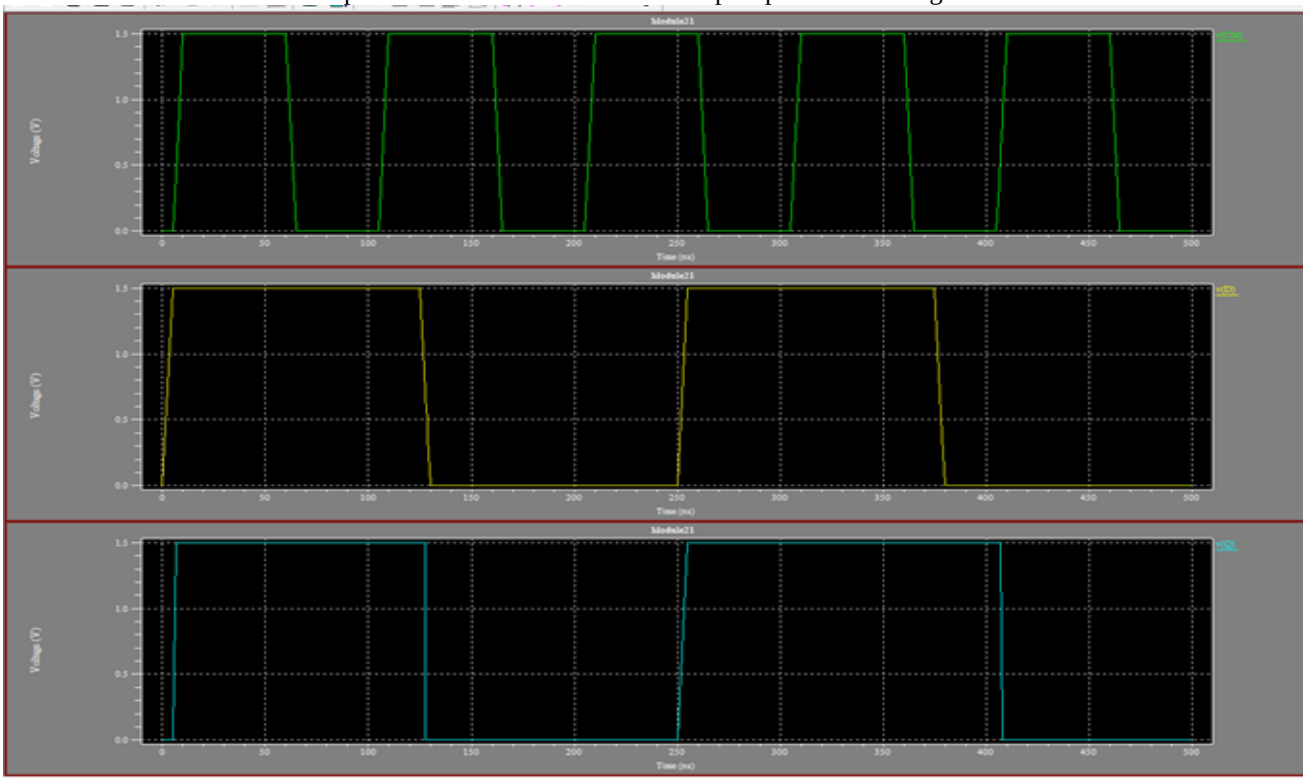

Fig.12- Output waveform of TSPC based DFF

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The comparison of D flip flop using these different technologies is shown in Table 1.

S.No.	DESIGN STYLE	POWER DISSIPATION (µW)	PROPAGATION DELAY (nsec)	FIGURE OF MERIT (µ-nJ)	NO. OF TRANSISTORS
1	CMOS	2	4.94	9.88	18
2	CCMOS	0.52	4.71	2.4492	14
3	GDI MUX	2.43	2.78	6.7554	12
4	POWER PC	0.09	30	2.7	20
5	TSPC	0.53	0.29	0.1537	9

Table.1-Comparison table of DFF using different techniques at 130nm

All these designs and simulations are done using TANNER EDA at 130nm Technology.

IV. CONCLUSION

It is concluded from power dissipation comparison that power pc has lowest power dissipation at 130nm.and in propagation delay comparison TSPC has least propagation delay and also concluded from transistor count comparison TSPC has less transistor count..So it is better to use TSPC logic style to design a system where fast speed is required. The electronic circuit designed with TSPC logic style will occupy less space on chip. TSPC has best performance in terms of power, speed at lower supply voltages.

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