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Design and Implementation of MCM based Block FIR Filter for the Application ECG Noise Filtering

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ABSTRACT: Modifying any type digital based hardware architecture and reducing the hardware system power, it's speed and the complexity level where VLSI technology is used . The process of filtering is mainly used in DSP and DIP real world applications as well and its work is to remove the noise in original signal or image. The filter architecture with an optimized process is used for reducing its processing time and to increase the performance of the system. In several digital signal processing (DSP) area adaptive digital filters find wide applications.Here a low-complexity filter design using the MCM scheme is presented with block implementation of fixed FIR filtersthe proposed structure involves significantly less energy per sample (EPS) and less area delay product (ADP) than the existing block implementation of direct-form structure for medium or large filter lengths, while for the short-length filters, the block implementation of direct-form FIR structure has less ADP and less EPS than the proposed structure. From the simulation results, we find that the proposed design offers large efficient output when compared to the existing outputs. Here the digital architecture based VLSI technology is used to modify the FIR filter architecture and this architecture uses a novel partial product generator which is generally used to alter the efficient architecture inorder to implement a delayed least mean square adaptive filter by using three co-efficient input.This algorithm is used to reduce the path delay and also to improve the speed when compare to proposed methodology.

KEYWORDS: block processing,FIR,reconfigurable architecture,VLSI.

I. INTRODUCTION

FIR digital filters are the ones find extensive applications in mobile communication systems in various specilizations such as channelization,channel equalization, matched filtering, and pulse shaping, because of their absolute stability and linear phase properties. But the problem is the filters employed in mobile systems must be realizedto consume less power and must operate at high speed.Thus we can conclude that the complexity of FIR filters is mainly dominated by coefficient multiplication operation. The number of LOs and the LD two are being two key metrics that determine the complexity of coefficient multiplications in FIR filters. LOs symbolize the adders required in calculating the sum of partial products in the multiplier,that determine the filter circuit's area and power requirements. LDs denote the number of adder steps in a maximal path of decomposed multiplications, that determine the speed of filtering operations. Thus, the low-complexity FIR filter implementation algorithms focuses on reducing the number of LOs and LD in coefficient multipliers.

Numerous design methodologies have been recommended by various researchersfor the efficient realization of FIR filters that are having fixed coefficients by using both distributed arithmetic (DA) and multipleconstant multiplication (MCM) approaches.Here DA-based designs use a special method called lookup tables (LUTs) to storeprecomputed results to reduce the computational complexity.

A method called MCM (Multiple Constant Multiplication) reduces the number of additions required for the realization of multiplicationsusing common subexpression sharing technique, when a given input ismultiplied with a set of constants. Here this MCM scheme is moreactive, when a common operand is multiplied with many number of constants. Hence, this MCM scheme is fitfor the implementation of large order FIR filters with fixedcoefficients. But the thing is, MCM blocks can be formed only in thetranspose form configuration of FIR filters. Popularly used method is Block-processing method which is used to derivehigh-throughput hardware structures. The beauty of this technique

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is that it not only providesthroughput-scalable design but also improves the area-delayefficiency. Eventhough block-based FIR structure' derivation isstraightforward when direct-form configuration is used while the transpose form configuration does notsupport block processing, FIR filter is required to be realizedby transpose form configuration. Because only with that, the advantages of MCM technique can be taken into account. Other than that, transposeform structures are inherently pipelined and they are supposed to offerhigher operating frequency to support higher sampling rate.

This block-processing method is popularly used to originate high-throughput hardware structures and it not only provides throughput-scalable design but also improves the area-delay efficiency. In this paper, we discover the possibility of realization ofblock FIR filter in transpose form structure in orderto take advantage of the MCM schemes and also for both fixed and reconfigurable applications, it explores the inherentpipelining for area-delay efficient realization of large orderFIR filters. There are threemain contributions that are explained in this paper as follows.

1. Block preparation for the transpose form FIR filter.
2. Analysis of transpose form FIRfiltrer and flow graph derivation with reduced registercomplexity.
3. Designing a transpose form block filter for reconfigurableapplications.
4. Block implementation of fixed FIR filters with a low-complexity design method using MCM scheme.
5.

II. EXISTING METHOD

For both fixed and reconfigurable applications, Basant Kumar Mohanty et al proposed a FIR filter in transpose form configuration for the advantages of efficient area and delay realization of large order FIR filters. In that, they have derived a flow graph for transpose form block FIR filter with optimized register complexity based on a detailed analysis of FIR filter in transpose form configuration. For the transpose form FIR filtera generalized block formulation is given and also they have derived a general multiplier based architecture for the transpose form of block filter which is used mainly for reconfigurable applications. Here the implementation of direct-form structure has less area delay product (ADP) and less energy per sample (EPS) for the short-length filters and for medium or large length filters, it offers high ADP and high EPS.

To add the partial inner productsin the FIR filter structure, the ripple carry adders are the one mainly used., Ripple Carry Adder which is the well known adder architecture is composed of cascaded full adders for an*n*-bit adder which is built by cascading of full adder blocks in series. Then the carry-out of onestage is fed directly to the carry-in of the next stage. There are *n* number of full adders needed for an *n*-bit parallel adder. Popularly used method is Block-processing method which is used to derive high-throughput hardware structures. The beauty of this technique is that it not only provides throughput-scalable design but also improves the area-delay efficiency.

III. PROPOSED METHOD

A. TRANSPOSE FORM BLOCK FIR FILTER FOR RECONFIGURABLE APPLICATIONS

The proposed structure for block FIR filter is [based on the recurrence relation] shown in Fig. 4.5 for the block size $L = 4$. It consists of one coefficient selection unit (CSU), one register unit (RU), M number of innerproductunits (IPUs), and one pipeline adder unit (PAU).

The CSU stores coefficients of all the filters to be used for the reconfigurable application. It is implemented using N ROM LUTs, such that filter coefficients of any particular channel filter are obtained in one clock cycle, where N is the filter length. The RU receives $\mathbf{x}k$ during the kth cycle and produces L rows of $\mathbf{S}0k$ in parallel. L rows of $\mathbf{S}0k$ are transmitted to M IPUs of the proposed structure. The M IPUs also receive M short-weight vectors from the CSU. such that during the kth cycle, the $(m + 1)$th IPU receives the weight vector $\mathbf{c}M-m-1$ from the CSU and L rows of $\mathbf{S}0k$ form the RU. Each IPU performs matrix-vector product of $\mathbf{S}0k$ with the short-weight vector $\mathbf{c}m$, and computes a block of L partial filter outputs $(\mathbf{r}mk)$. Therefore, each IPU performs L inner-product

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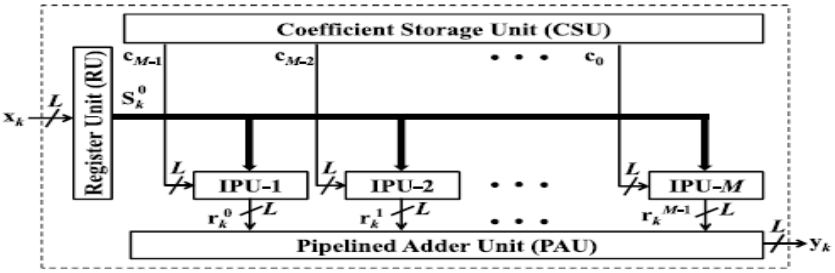

Figure 4.1 block fir filter

computations of L rows of $\mathbf{S}0k$ with a common weight vector $\mathbf{c}m$. The structure of the $(m+1)$th IPU . It consists of L number of L-point inner-product cells (IPCs). The $(l+1)$th IPC receives the $(l+1)$th row of $\mathbf{S}0k$ and the coefficient vector $\mathbf{c}m$, and computes a partial result of inner product $r\,(kL-l)$, for $0 \le l \le L-1$. Internal structure of $(l+1)$th IPC for $L = 4$ is shown in Fig. 8(a). All the M IPUs work in parallel and produce M blocks of result $(\mathbf{r}mk)$.These partial inner products are added in the PAU to obtain a block of L filter outputs. In eachcycle, the proposed structure receives a block of L inputs andproduces a block of L filter outputs, where the duration of eachcycle is $T = TM + TA + T\text{FA} \log 2 L$, TM is one multiplier delay, TA is one adder delay, and TFA is one full-adder delay.

B. MCM-BASED IMPLEMENTATION OF FIXED-COEFFICIENT FIR FILTER

The proposed MCM-based structure for FIR filters for block size $L = 4$ is shown in Fig. 4 for the purpose of illustration. The MCM-based structure (shown in Fig. 9) involves six MCM blocks corresponding to six input samples. The proposed MCM-based structure for FIR filters for block size $L = 4$ is shown in Figure 4.5. For the purpose of illustration. The MCM-based structure involves six MCM blocks corresponding to six input samples. Each MCM block produces the necessary product terms as listed in Table 4.1. The subexpressions of the MCM blocks are shift added in the adder network to produce the inner-product values (rl,m), for $0 \le l \le L-1$ and $0 \le m \le (N/L)-1$ corresponding to the matrix product of (14). The inner-product values are finally added in the PAU to obtain a block offilter output. The Canonical Signed Digit (CSD) representation of filter coefficients will increase the common subexpressions which reduces the design complexity. The design examples show that the average reduction of LO achieved using the optimized method is better than the other subexpression techniques.

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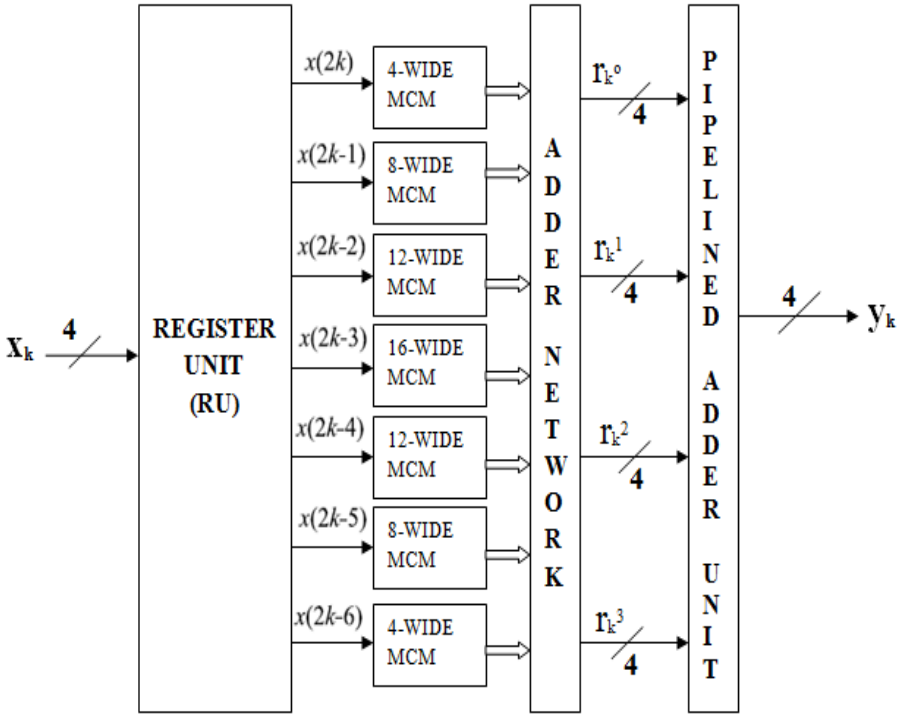

Figure 4.2 MCM based structure for fixed fir filter of block size L=4 filter length N=16

C. FILTERING NOISE FROM ELECTROCARDIOGRAM USING FIR FILTER

Filtering of ECG signal is very important because noisy ECG signal can mask some important features of the Electrocardiogram (ECG). Hence the filters are necessary to remove this noise for proper analysis of the ECG signal. This paper presents the study of FIR filter using common subexpression elimination techniques for ECG signal Processing. The common subexpression elimination techniques minimize the logic operators (LO) in realizing finite impulse response (FIR) filters. The Canonical Signed Digit (CSD) representation of filter coefficients will increase the common subexpressions which reduces the design complexity. The design examples show that the average reduction of LO achieved using the optimized method is better than the other subexpression techniques.
The ECG signal gets corrupted due to different types of artifacts and interferences such as Electrode contact noise, Power line interference, Motion artifacts, contraction, Base line drift, Instrumentation noise generated by electronic devices and Electrosurgical noise

IV. IMPLEMENTATION

A SIMULATION

The ECG signal samples are used to revise the different cases of the patient and these signals are taken from MIT-BIH database . These ECG signals are easy to be examined in MODELSIM and XILINX.The number of samples are not enough for a complete study the effects of several parameters such as age, gender, weight, etc. The purpose of this study focuses only on the pre-processing of ECG signal without concerning such factors for sampling.This Pre-processing of ECG signal is made for the removal of noise associated with the ECG signal. While acquisition of ECG, it gets corrupted due to different types of artifacts and interferences such as Power line interference, Electrode contact noise, Motion artifacts, Muscle contraction, Base line drift, Instrumentation noise generated by electronic devices and Electrosurgical noise. For the meaningful and accurate detection, steps have to be taken to filter out all these noise sources.

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B. RESULT OF THE TRANSPOSE FORM BLOCK FIR FILTER FOR APPLYING A DIGITAL INPUT

The simulation result of transpose form block FIR filter using recurrence relation is shown in the figure5.1thus for the block size=4 and filter length 16. The impulse response is "finite" because there is no feedback in the filter; if you put in an impulse (that is, a single "1" sample followed by many "0" samples), zeroes will eventually come out after the "1" sample has made its way in the delay line past all the coefficients. The Canonical Signed Digit (CSD) representation of filter coefficients will increase the common subexpressions which reduces the design complexity. The design examples show that the average reduction of LO achieved using the optimized method is better than the other subexpression techniques.

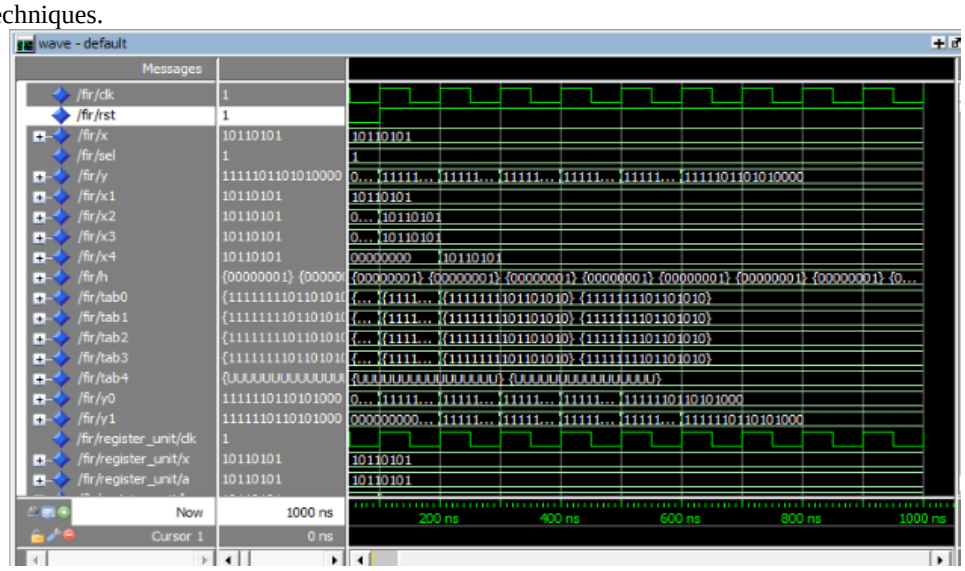
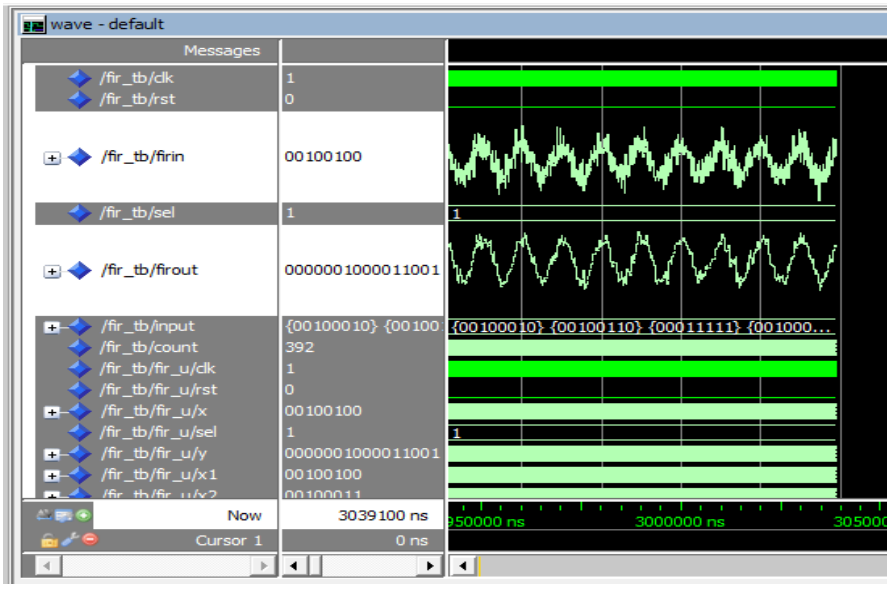


Figure 5.1 simulation result of of block fir filter

C. FILTERING NOISE FROM ELECTROCARDIOGRAM USING FIR FILTER

The simulation result of filtering noise from electrocardiogram using fir filter Is shown the figure 4.7. Figure shows an ECG Waveform which consist of P wave, QRS complex, T wave And various intervals. Importantly, the R-R interval represents one heartbeat.



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D. PERMANCE ANALYSIS

The performance of MCM based FIR filter architecture for fixed and reconfigurable block FIR filter was stimulated by MODELSIM 6.3. The various parameters such as area, power, delay are found out and compared with the other MCM algorithm.

TABLE 4.2 COMPARISON TABLE:

PARAMETER	EXISTING SYSTEM	PROPOSED SYSTEM
TYPE	DA	MCM
AREA(SLICES COUNT)	460	147
DELAY TIME (ns)	59.745	30.747
FREQUENCY (MHz)	16.737	32.523

V. CONCLUSION AND SUGGESTION FOR FUTURE WORK

FIR with DUC multistandard channel filter architecture is designed to reduce the circuit complexity level when compared to the existing channel filter architecture. For area-delay efficient realization of both fixed and reconfigurable applications, realization of block FIR filters in transpose form configuration is carried out. Here a generalized block formulation is presented for transpose form block FIR filter based on that transpose form block filter is derived for reconfigurable applications. In order to reduce the computational complexity, a new novel method is presented to recognize the MCM blocks for both horizontal and vertical subexpression elimination in the proposed block FIR filter for fixed coefficients. Simulation results show that the proposedMCM based FIR filter architecture for fixed and reconfigurable application involves significantly less ADP and less EPS than the existing block direct-form structure for medium or large filter lengths whereas for the short-length filters, the existing block direct-form structure has less ADP and less EPS than the proposed structure.

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