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Design and Analysis of Energy Efficient Adders Using Low Power Techniques

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ABSTRACT: As leakage power (static power) dissipation is playing a major role in the total power dissipation of a circuit. Hence, Different techniques were proposed and implemented over the time .So we proposed a technique called Power gate, which is an advanced version of sleepy keeper. In order to maintain the proper output and area, we decreased the number of transistors in the circuit. A full adder adds binary numbers and accounts for values carried in as well as out. A one-bit full adder adds three one-bit numbers, often written as A, B, and Cin; A and B are the operands, and Cin is a bit carried in from the previous less significant stage. The full adder is usually a component in a cascade of adders, which add 8, 16, 32, etc. bit binary numbers.

Full adder circuit is an essential component for designing of various digital systems. It is used for different applications such as Digital signal processor, microcontroller and microprocessor and data processing units. Due to scaling trends and portability of electronic devices there is a high demand and need for low power and high speed digital circuits with small silicon area. Full adder circuits are used comprehensively in Application Specific Integrated Circuits (ASICs). So, design and analysis of low power and high performance adders are of great interest .This method aims on power gate technique .power gate is a novel technique for low power digital circuits design in a VLSI design this techniques allows reduction in power consumption, propagation delay, and transistor count of the digital circuit compared to static, sleepy transistor and sleepy keeper techniques.

KEYWORDS: Full Adder, Sleep Keeper, Power Gating

I.INTRODUCTION

Low power has become main constrain for portable systems. These systems require more feature and high battery life time. The total power of the electronic circuit is the sum of static power, dynamic power and short circuit power. The dynamic power consumption becomes significant contributor to overall power consumption. Hence, the reduction of power consumption is compulsory.

A 1-bit full adder adds three single-bit numbers, often written as A, B, and Cin. The A and B used as operands and Cin bit are carried in from the succeeding least significant stage. Adder circuits produce double-bit output, carry-out and sum typically represented by the signals Cout and Sum, where

Sum = A xor (B xor Cin)
Cout = A.B + A.Cin + B.Cin

This paper presented two different technique based on the reduce the leakage power.

A. Sleep Keeper

The new leakage reduction technique which is called as the sleepy keeper. The basic problem with traditional CMOS is, the transistors are used only in their most efficient and natural inverting way i.e. PMOS transistor is connected to VDD and NMOS transistor is connected to GND. It is well known that PMOS transistors are not efficient at passing GND i.e. weak zero output we are going to get. Similarly it is well known that NMOS transistors are not efficient at passing VDD i.e. weak one is the output form. However to maintain the value of '1' in sleep mode, given that the '1' value has already been calculated, the sleepy keeper approach uses this output value of '1' and an NMOS transistor is connected to VDD to maintain output value equal to '1' when in sleep mode.

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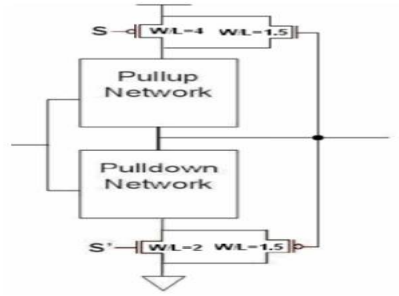

Fig 1: Sleepy keeper structure

B. Power Gating

Power Gating is a technique used in integrated circuit designs. The main aim of this circuitry is to reduce power consumption, by switching off the power flow in the unused blocks in the circuit. In addition, it is also used in reducing stand-by or leakage power. Power gating technique is used to save the leakage power when, the system is not in operation. This can be accomplished by adding a switch, either to VDD or VSS supply. If the design is power gated, then it is said to be in OFF state, where the power is switched off. Hence it is more beneficial technique of all the low power techniques as we can dissipate near zero power. The control to the power gating switching circuit is generated by the Power gating control block

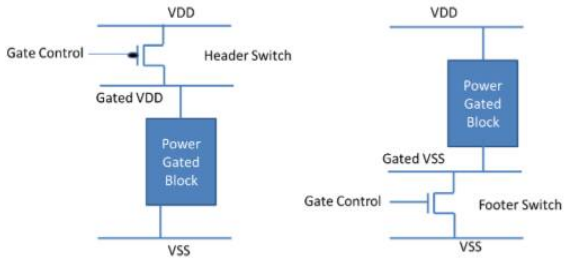

Fig 2: Power Gating Technique

II.LITERATURE SURVEY

A. Complementary Cmos Logic style:

A static CMOS gate is a combination of two networks, called the pull-up network (PUN) and the pull-down network (PDN) as shown as Figure.2.1. The figure shows a generic N input logic gate where all inputs are distributed to both the pull-up and pull-down networks. The function of the PUN is to provide a connection between the output and VDD anytime the output of the logic gate is meant to be 1 (based on the inputs). Similarly, the function of the PDN is to connect the output to VSS when the output of the logic gate is meant to be 0. The PUN and PDN networks are constructed in a mutually exclusive fashion such that one and only one of the networks are conducting in steady state. In this way, once the transients have settled, a path always exists between *Vdd*and the output F, realizing a high output (“one”), or, alternatively, between *VSS* and F for a low output(“zero”). This is equivalent to stating that the output node is always a low-impedance node in steady state.

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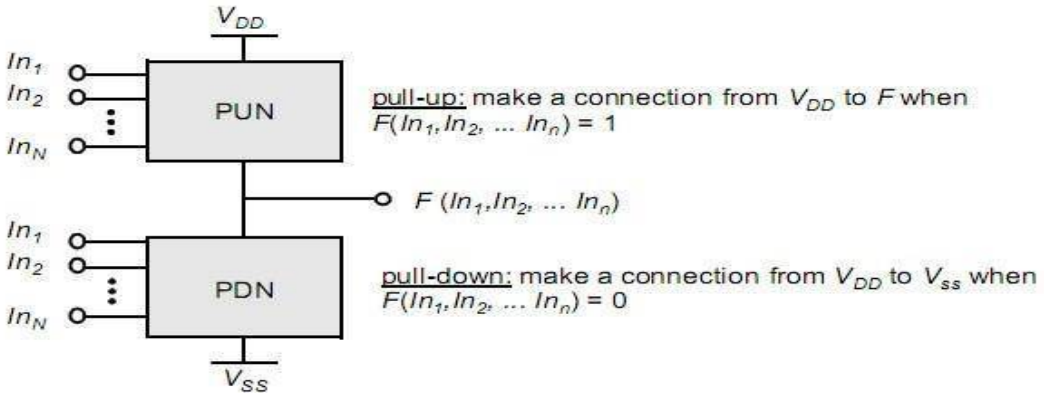

Figure.3: Complementary logic gate as a combination of a PUN (pull-up network) and a PDN(pull-down network)

B. Sleep Approach

The most well-known traditional approach is the sleep approach. In the sleep approach, both(i) an additional "sleep" PMOS transistor is placed between Vdd and the pull-up network of a circuit and (ii) an additional "sleep" NMOS transistor is placed between the pull-down network and Gnd.In case of sleep approach in fig.2, transistors gating VDD and GND are added to the base case. The added transistors cut off supply of power when in sleep mode. Each added transistor is referred to as “sleep transistor” and takes the width of the largest transistor in the base case. A PMOS transistor is placed between VDD and the pull up network, and NMOS sleep transistor is placed between GND and pull down network

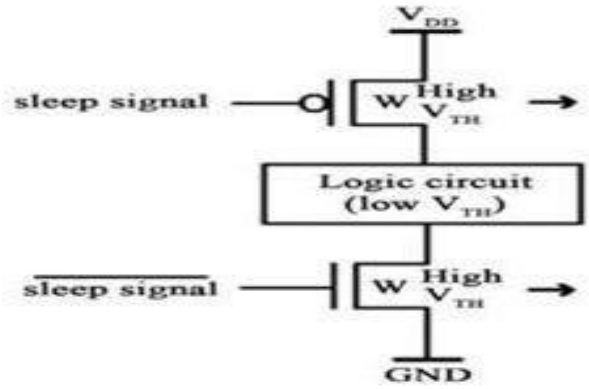

Figure.4: Sleep Transistor technique

III. DESIGN AND IMPLEMENTATION

A. Conventional CMOS:

The full adder operation can be stated as follows

Given the three 1-bit inputs A, B, and Cin, it is desired to calculate the two 1-bit outputs Sum and Carry, where

Sum = A xor (B xor Cin)

Cout = A.B + A.Cin + B.Cin

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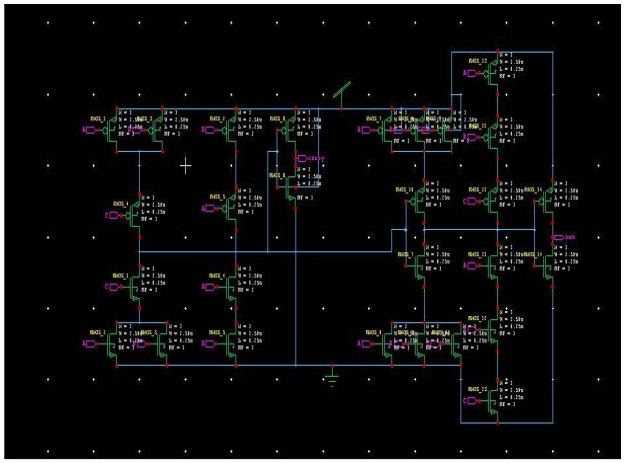

Figure 3: Conventional 28-T 1 bit full adder

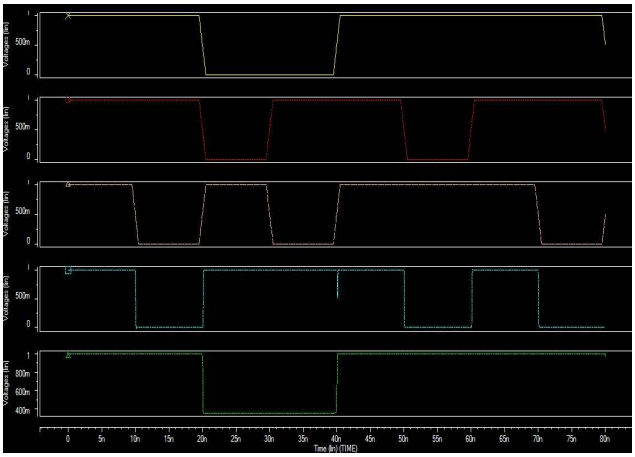

Figure 4: Full adder output wave form

B.Sleepy Keeper Technique:

This technique is used for static power dissipation reduction and maintaining the proper state of output. Two extra transistors one is P-type and N-type transistor are connected parallel to footer transistor with one terminal connected to ground and to header transistor with one terminal at VDD respectively.

This avoids the floating output, which was the major disadvantage of previously used sleep approach. The following output of main logical circuit is given as the input to keeper transistor. We considered that sleepy keeper technique having less static power consumption and delay.

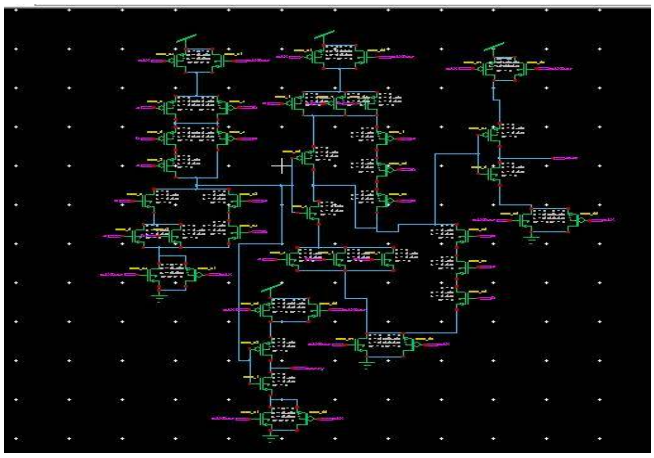

Figure 5:Sleepy keeper Technique 1 bit full adder

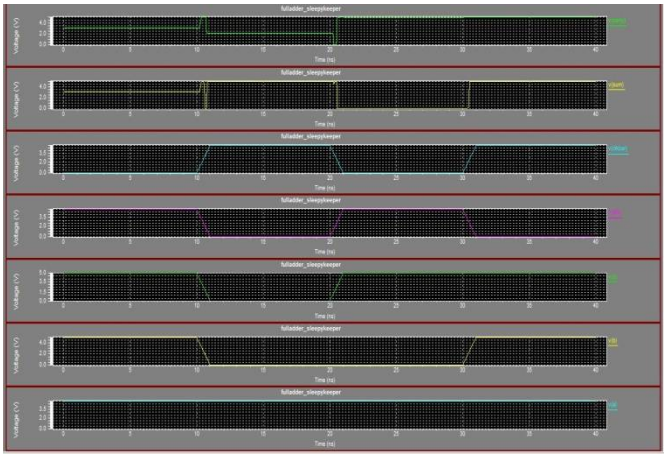

Figure 6: Sleepy Keeper Technique output wave form

C. Power Gate Technique:

Power gating is a technique used in integrated circuit design to reduce power consumption, by shutting off the current to blocks of the circuit that are not in use.In addition to reducing stand-by or leakage power, power gating has the benefit of enabling Iddq testing.

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Power gating uses low-leakage PMOS transistors as header switches to shut off power supplies to parts of a design in standby or sleep mode.

NMOS footer switches can also be used as sleep transistors. Inserting the sleep transistors splits the chip's power network into a permanent power network connected to the power supply and a virtual power network that drives the cells and can be turned off.

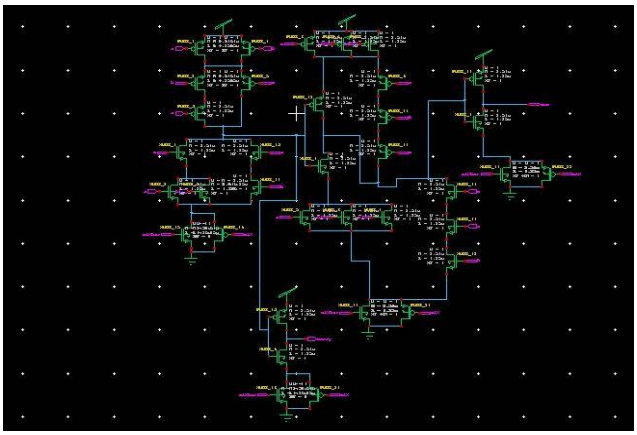

Figure 7: Power gating technique 1 bit full adder

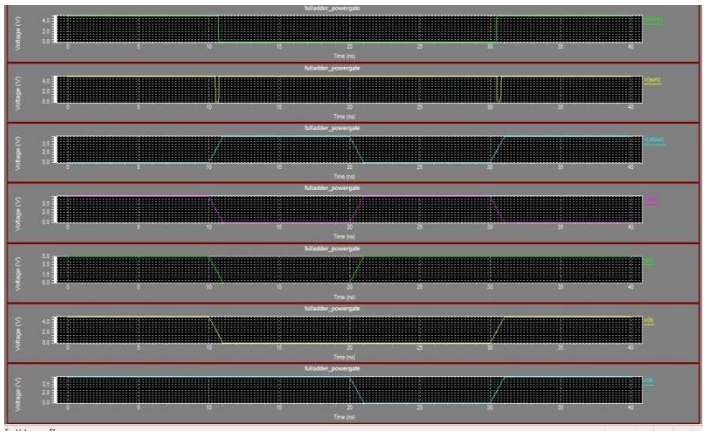

Figure 8: Power gating technique output waveform

III. SIMULATION RESULTS

In the nanoscale CMOS technology, leakage loss is major concern. The focus of this dissertation is the problem of increasing leakage in modern VLSI designs. In this dissertation we have studied various power gating techniques for low power VLSI design. Power gating techniques are commonly used in today's high performance microprocessors for obtaining high performance that are not possible using static CMOS circuits. Power gating logic provides high speed, high fan-in and compact gates with flexibility in design and logic output.

Here we designed a new method for implementing a low power full adder by Sleepy keeper and Power gating using 22nm and 16nm technology. The explored technique of realization achieves a low power high speed design for a widely used subcomponent full adder. Simulated outcome using state-of-art simulation tool shows power and speed comparison between conventional and proposed full adders also presented. All simulations have been performed on 90nm and 45nm standard models on Tanner EDA tool.

The schematic of the circuits was captured in S-EDIT and Simulation was carried out in T-SPICE from TANNER EDA and H-Spice Schematics and simulation waveforms of design are shown in figures below.

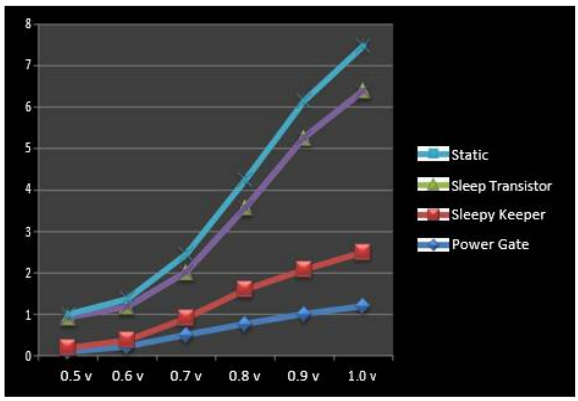

Figure 9: 16nm vdd varies from 0.5v to 1.0 v

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Table 1: 16nm Vdd varies from 0.5v to 1.0 v

Voltage	Power Gate	Sleepy Keeper
0.5 v	0.095355	0.094601
0.6 v	0.21728	0.15531
0.7 v	0.49857	0.41212
0.8 v	0.76546	0.82699
0.9 v	1.0089	1.0669
1.0 v	1.2001	1.2954

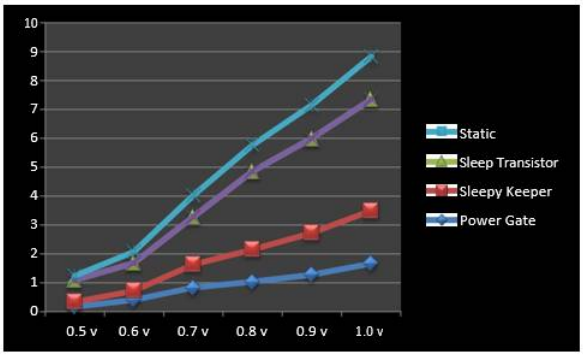

Figure 10: 22nm vdd varies from 0.5v to 1.0 v

Table 2: 22nm vdd varies from 0.5v to 1.0 v

Voltage	Power Gate	Sleepy Keeper
0.5 v	0.17679	0.15456
0.6 v	0.41216	0.31192
0.7 v	0.82763	0.80767
0.8 v	1.0364	1.1168
0.9 v	1.2818	1.4495
1.0 v	1.6736	1.8223

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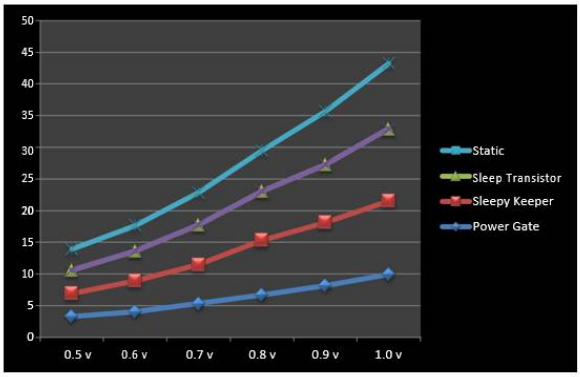

Figure 11: 90nm vdd varies from 0.5v to 1.0 v

Table 3: 90nm vdd varies from 0.5v to 1.0 v

Voltage	Power Gate	Sleepy Keeper
0.5 v	3.3158	3.5955
0.6 v	4.077	4.8163
0.7 v	5.3453	6.1081
0.8 v	6.748	8.582
0.9 v	8.1906	9.9074
1.0 v	9.9499	11.607

IV. CONCLUSION

In order to test the performance of proposed adder cells, all schematic have performed on Tanner EDA tool version 13.0v and Simulations have carried out using HSPICE to measure the power consumption, propagation delay and power delay product of the full adders using 90nm and 45nm technology with same input conditions of 1.0 V and 0.7V supply Simulation results are shown in figures.

The primary goal of this thesis work is not only to provide an efficient result in low power VLSI design but also shows a successful try in terms of reduction of power dissipation. With the continuous technology scaling devices, the leakage power is of great concern for designs in nanometer technologies and is becoming a major contributor to the total power consumption; leakage power has become more dominant as compared to Dynamic power. The gate leakage has become dominant sources of leakage and is expected to increase with the technology scaling. The solutions for leakage power dissipation or reduction of leakage power dissipation have to be sought both at the process technology and circuit levels. Here we thoroughly reviewed the some of the techniques efficiently used in reducing leakage power consumption in all digital as well as analog designs.

V. FUTURE WORK

The advent of a mobile computing era has become a major motivation for low power design because the operation time of a mobile device is heavily restricted by its battery life. The growing complexity of mobile devices, such as a cell phone with a digital camera or a personal digital assistant (PDA) with global positioning system (GPS), makes the power problem more challenging. The proposed technique can be implemented in low power VLSI circuit and save the

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power consumption of the chip which leads to increase battery life. Next we will research on Finfet and Tunnel fet technologies.

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BIOGRAPHY

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