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Eye Diagram Analysis of ICS using Digital Phosphor Oscilloscope

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ABSTRACT: Numerous kinds of interconnection rise for those rapid correspondences of electrical advanced signs, for instance, bundles for incorporated circuits, non coaxial connectors , for loads up (inner) or items (external).Eye outline is an estimation strategy for assessing the transmission quality through either a gadget or a framework in a measurable way. In this paper, eye diagram analysis is performed for a semiconductor IC using digital phosphor oscilloscope to test if it meets the high speed and full speed compliance limits set by USB-Implementers forum. By rehashing this development over numerous examples of the waveform, the resultant diagram will speak to the normal insights of the sign and will take after an eye. The enlightening compares to the slightest bit time frame and is commonly called the Unit Interval (UI) width of the eye chart. The results in this work are eye diagram analysis of high speed and full speed USB and the compliance tests are passed.

.**KEYWORDS:** Universal Serial Bus-Implementers Forum (USB-IF), Integrated Circuit (IC) ,Digital Phosphor Oscilloscope(DPO),HighSpeed Electrical Test Tool (HSET)

I. INTRODUCTION

Information eye graph is a technique for speaking to and investigating fast computerized signal. The eye chart permits perception and assurance of key parameters of the sign's electrical quality rapidly. Information eye outline Folding the pieces of the waveform comparing to every individual piece from the computerized waveform into a solitary diagram, with the sign adequacy on the vertical hub and the time on the even hub. By rehashing this develop more than a few models of waveform, the subsequent diagram speaks to the normal insights of the sign and is like the eye. The enlightening compares to a piece period and is typically called the unit stretch (UI) width of the eye graph. The perfect advanced waveform with sharp ascent and fall times and steady adequacy is the eye outline as appeared in Fig.1.

The analysis is carried out for an Integrated circuit (IC) with both typical devices and corner lots. The corner lots are worst case scenario devices with different mobilities for PMOS and NMOS of the device. The corner lot devices are manufactured and eye diagram analysis is carried out on them in every IC manufacturing cycle. The passing of eye diagram analysis for both typical and corner lots ensures that the IC or device meets the standars set by USB-IF. Approval from USB-IF results in increased reliability of the device and every semiconductor IC manufacturer strives to achieve this standard.

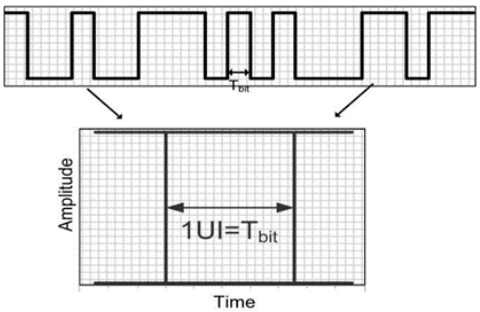

Fig.1. Ideal High Speed Digital Signal with Eye Diagram

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II. RELATED WORKS

As referenced in the theoretical, early testing of configuration is important to improve quality.
In [1], Presents a 12.5-Gb/s on-chip oscilloscope (OCO) circuit to gauge eye outlines and Jitter histograms of highspeed computerized signals.In [2], Proposes eye chart estimation strategies for direct input move register (LFSR)-based piece streams in pseudo irregular double grouping (PRBS) test and scrambling.In [3], creator talks about demonstrating strategy of proportionate lumped circuit for fast interconnections, an inventive technique is proposed to anticipate the physical inborn eye graph. As referenced in [3], examine multiplexer offering ascend to sequential output punishments can be comprehended from [4], [5]. In [4] The plan and usage of eye graph development and investigation is done in DPO. In [5] Author Proposes a quick approach that utilizes just two antipolarity the slightest bit information designs rather than the pseudo-irregular piece arrangement as info sources to recreate the most pessimistic scenario eye chart.

III. PROPOSED METHOD

Decide whether the gadget under test has a hostage link, or whether it has a standard Series B or Mini-B repository. Hostage link structures require signal quality estimation at the end (hsfe). Separable link structures require estimation at the close to end (hsne). Turn on the oscilloscope and permit it to get ready for 20 minutes. Empower the TDSUSB programming application on oscilloscopes. Press the Default Setup button on the Oscilloscope Front Panel, select File → Recall Default in the Applications menu bar, select the High Speed tab in the Measuring Option menu of the USB 2.0 consistence test application, select High Speed Signal Quality Tests, Eye Diagram, Timeline, Rate And EOP in Signal Quality Area ofApplication, Up Click Configure on the Licensing screen. Select the upstream and most end for devices with captive cables or near end for devices that do not have captive cable. Press the icon. Verify that the oscilloscope display does not report "clipping". If it is, adjust the vertical spread until the "clipping" message does not appear. Press OK on the screen until it displays the correct waveform. Attach the USB cable to the designated power supply port of the Compliance Test Fixture. Verify that the red power LED and red init LED are lit. Connect the upstream facing port of the device under test to the USB connector of the device's SQ segment of the test fixture. Connect the initial port of the test fixture to the high-speed capable port of the test bed computer. Apply power to the device. Attach the differential probe of the test fixture. Make sure the + polarity in the probe is with D + on the fixture. High-speed electrical test bed Launch high-speed electrical test tool software on a computer. The main menu appears and shows the USB2.0 Host Controller. Select the device and click TEST to enter the HS Electrical Test Tool Application → Device Test menu. The device under test must be counted together with the root port connected to the device's VID. Place the test switch (S6) in the test position. Verify that the red test LED is lit. Using the oscilloscope, verify that the test packets are being transmitted from the test port. Adjust the trigger level as necessary. If you cannot get a steady trigger by adjusting the trigger level, try a slight change in the trigger. Once the test packet is displayed correctly, click OK in the Application dialog box.
The Tektronix USB application usually triggers and displays the correct test packet without the need to place cursors. Cursors can be started from the application by selecting them if needed, and if the cursor measurement is enabled on the oscilloscope, place two vertical cursors around a test packet. After the EOP (END OF PACKET) place the cursor before the sync field (a bit time) and another cursor (a bit time). Click OK on the USB2 application, the dialog box to enable acquisition and analysis of the test packet.

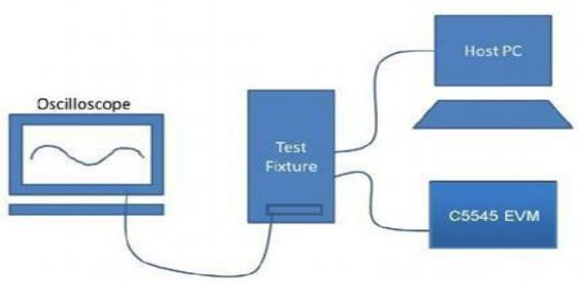

Fig.2. Test Setup

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IV. RESULTS

Rapid and max throttle USB tests were led for both commonplace gadgets and procedure corners (all corners are passing). The particulars of the considerable number of parameters set by USB-IF are passing.

Procedure Lots (or corner parcels) are exceptional changed wafers that help confirming chip structure strength to suit process varieties that measurably happen in wafer creation throughout the years. The red mask region is the compliance limit of the devices and none of the eye diagrams are within the red region ensuring the compliance test is passed.

There are 5 exemplary corners:

- FF (quick)
- SF (slow quick)
- SS(slow moderate)
- FS (quick moderate)
- TT(typical run of the mill)

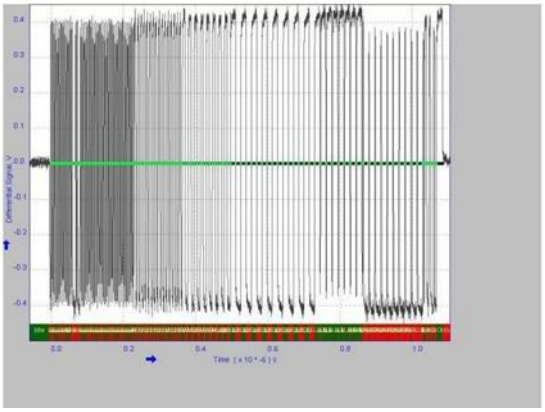

Fig.3. High speed Waveform Plot

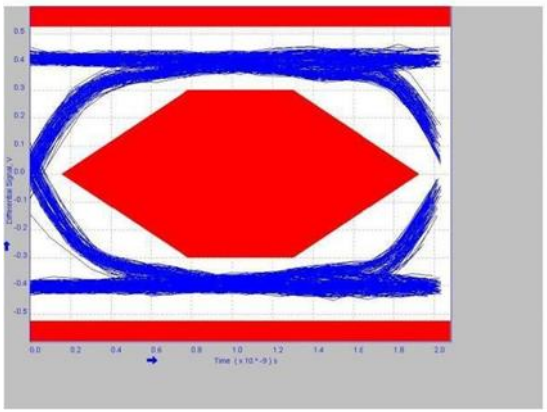

Fig.4. High speed Eye Diagram

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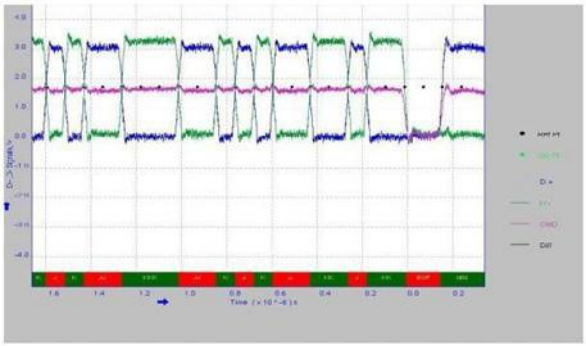

Fig.5. Full speed Waveform Plot

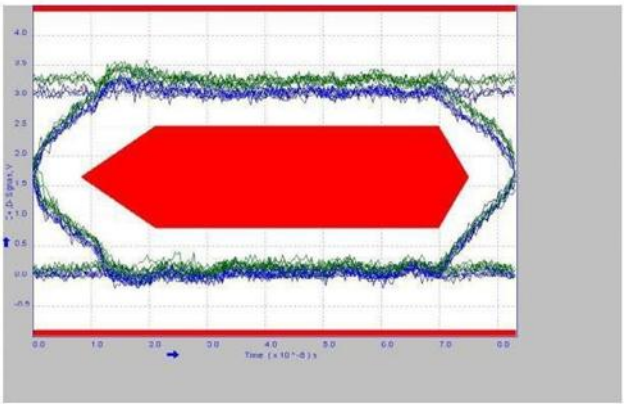

Fig.6. Full speed Eye Diagram

V. CONCLUSION

AS High Speed advanced Signals surpass numerous gigabit every subsequent rates, eye charts give the way to rapidly and precisely measure signal quality and framework execution. In this work, high speed and full speed USB analysis is vital in any device manufacturing of a semiconductor IC manufacturing process. The compliance is met and passed for both typical IC devices along with corner lots. The passing of corner lots ensures high robustness of the device as they are worst case scenario devices.

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