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Computation of Silicon Neuron and Synapse: Neuromorphic Analog VLSI Systems

Dr.V.C.Kotak, Prof.Sushma Srivastava, Madhuri Gala, ShilpaPandhare

Vice Principal, Shah & Anchor Kutchhi Engineering College, Mumbai, India

Associate Professor, Dept. of Electronics Shah & Anchor Kutchhi Engineering College, Mumbai, India

M.E. Student, Dept. of Electronics, Shah & Anchor Kutchhi Engineering College, Mumbai, India

M.E. Student, Dept. of Electronics, Shah & Anchor Kutchhi Engineering College, Mumbai, India

ABSTRACT: The term "*neuromorphic*" was coined by *Carver Mead* to describe very large scale Integration (VLSI) systems containing electronic analog circuits that mimic neurobiological architectures present in the nervous system [1]. Neuromorphic computation is related to modelling and simulation of networks of neurons and systems using the same *organizing principles* found in real nervous system. We have implemented the synapse –neuron integration to understand the signal processing between the two. The Spice simulation software provide a highly flexible platform to test the computational properties of Analog VLSI Neuromorphic circuits described in this paper, and allow us to test the behavior of such circuits.

KEYWORDS: neuromorphic; neural networks; analog circuits; subthreshold; silicon neuron; silicon synapse; Integrate and fire; depression; facilitation.

I. INTRODUCTION

Neuromorphic engineering is a discipline characterized by two main goals. Firstly to understand the computational properties of biological neural systems using standard CMOS VLSI technology as a tool. And to make use of the known properties of biological systems to design and implement efficient devices for engineering applications [2]. It was first observed by *Carver Mead* that the CMOS circuits operating in the sub-threshold region have current–voltage characteristics similar to that of ion-channels present in neurons and synapse and also consume less power; hence can be used as analogues of neuron and synapse.

There are some direct analogies between biological neural systems and analog VLSI neuromorphic systems: conservation of charge, amplification, exponentiation, thresholding, compression, and integration. Neuromorphic Architectures are Computer architectures that are similar to biological brains; computer architectures that implement artificial neural networks in hardware. Functional units are composed of neurons, axons, synapses, and dendrites. Synapses are connections between two neurons. Remembers previous state, updates to a new state, holds the weight of the connection. Axons and dendrites connect to many neurons/synapses, like long range bus.

II. RELATED WORK

The applicability of neuromorphic devices to engineering challenges is widespread, and includes biomedical, displays, hearing, imaging, language, locomotion, neural interface, power, processing, robotic, security and vision. Neuromorphic engineering proposes to fill the gap between, on the one hand, computational neuroscience, and, on the other hand, traditional engineering. A common purpose is establishing prosthesis, circumventing areas in the brain, which became dysfunctional after a stroke or head injury. Some brain implants involve creating interfaces between neural systems and computers, these are part of a wider research field called brain computer interfaces. *Brain implants (neural implants)*, are devices that connect directly to a biological subject's brain or nervous system. They are usually placed on the surface of the brain, attached to the brain's cortex or fired into the brain.Neural Prosthesesis used in conjunction with a planned training program to replace or improve function of an impaired nervous system or to provide a better, more controllable prosthesis following loss of a limb.

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The first widely used neural prosthetic was the cochlear hearing implant in the early 1980s, which provides a sense of sound to people with severe hearing impairment. Since the late 1990s, implants for the brain and spinal cord have been developed with varying degrees of success. Brain-machine interfaces (BMIs) have been defined as devices that detect intent—typically intended movement—from brain activity, and translate it into an output action, such as control of a cursor on a screen or a robotic arm, acquiring a neural signal that can be consciously controlled; analyzing that signal to identify an intended motor output; and executing the intended action. A visual prosthesis, often referred to as a bionic eye, is an experimental visual device intended to restore functional vision in those suffering from partial or total blindness. Many devices have been developed, usually modelled on the cochlear implant or bionic ear devices, a type of neural prosthesis in use since the mid-1980s [3].

III. ANALOG NEUROMORPHIC CIRCUITS

An important reason of using analog computation is that it provides 10-100 times greater computational density than digital computation.Analog circuits deliver much lower power than digital circuits. Also these analog circuits can perform many computations faster and more efficiently than digital [4]. It is easy to develop analog circuits as they follow the same physical laws as biological systems. The advantage of analog circuits is their Accuracy and Reconfigurability. Silicon Simulation of analog circuit is easy than digital circuit. Analog computation yields tremendous power savings equal to a >20 year leap in technology.

A. Sili*con Neuron:*

From the functional point of view, silicon neurons can all be described as circuits that have one or more *synapse* blocks, responsible for receiving spikes from other neurons, integrating them over time and converting them into currents, as well as a *soma* block, responsible for the spatial-temporal integration of the input signals and generation of the output analog action potentials and/or digital spike events. In addition both synapse and soma blocks can be interfaced to circuits that model the neuron's spatial structure and implement the signal processing that takes place in dendritic trees and axons respectively.

The circuits we use to implement the neuron are based on those pro-posed by Mead, Liu S.-C, and Van Schaik and have been described in detail by Indiveri. The integrate-and-fire neuron model (also known as threshold fire model) is one of the most widely used models. In I&F neuron circuits like Axon-hillock circuit when potential V reaches a threshold value, then an action potential is generated and V is reset to a sub-threshold value. The membrane capacitor is charged until it reaches a certain threshold, at which time it discharges, producing an action potential (spike) and the potential is reset. Thus the traditional form of an integrate-and-fire model has sub-threshold integration domain where the neuron integrates the inputs and a threshold voltage for the generation of action potential.

The Axon-Hillock circuit is very compact and allows for implementations of dense arrays of silicon neurons. It has a major drawback: it dissipates non-negligible amounts of power.An alternative design that has both the possibility to set an explicit threshold voltage and that implements spike-frequency adaptation is proposed in Linear Threshold Integrate & Fire neuron circuit.

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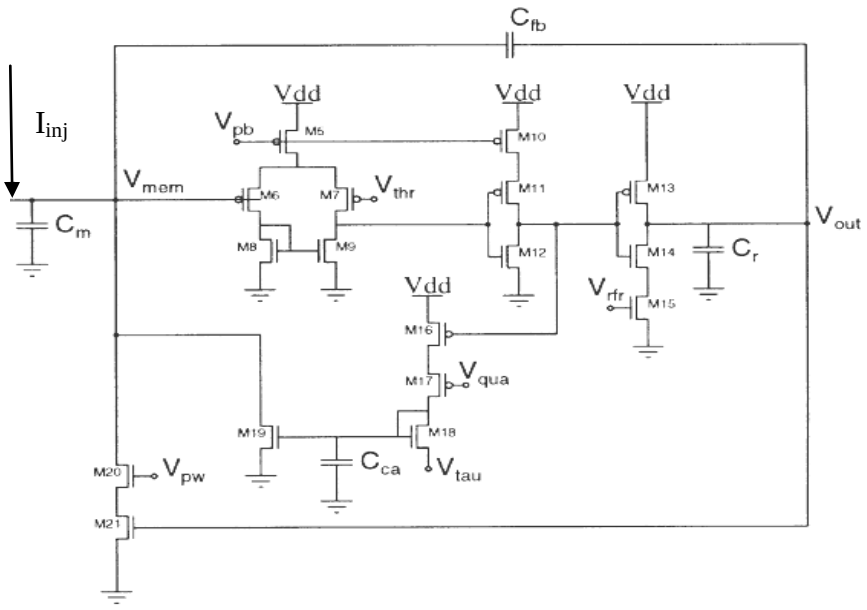

Fig. 1. Circuit diagram of Linear Threshold Integrate and Fire Neuron

The circuit in the Fig1 implements a linear threshold integrate-and-fire neuron with an adjustable voltage threshold V_{thr}, spike pulse width V_{pw} and refractory period V_{rfr}. If a DC current I_{inj} is sourced into the neuron's membrane capacitance C_m, its membrane voltage V_{mem} increases accordingly. The transconductance amplifier M5-M9 compares V_{mem} to threshold Voltage V_{thr}. As soon as V_{mem} exceeds V_{thr}, the amplifier's output voltage switches to V_{dd}. The two inverters M10-M12 and M13-M15 implement a non- inverting high-gain amplifier; hence V_{out} also switches to V_{dd}. The capacitor C_{fb}, together with C_m implements a capacitor divider that provides a positive feedback to the node, V_{mem}. This feedback speeds up the circuit's response [5].

When V_{out} switches to V_{dd}, the transistor M21 is switched on. This discharges membrane capacitor C_{mem} to flow to ground through transistors M20 and M21 at a rate controlled by V_{pw}. This bias voltage can be used to control the spike's pulse width. As C_{mem} is discharged, V_{mem} decreases. Once V_{mem} decreases below the threshold V_{thr}, the transconductance amplifier switches to ground. The first inverter then switches to V_{dd}, but the output of second inverter V_{out} does not immediately goes to zero; it decreases linearly at a rate set by V_{rfr}. In this way, transistor M21 is kept on even after the V_{mem} has decreased below the neuron's threshold voltage. As long as the gate voltage of M21 is sufficiently high, the neuron is said to be in its refractory period, Spike pulse cannot be generated because the current injected in the membrane capacitance Cm is discharged directly to ground. Once the transistor M21 is turned off, a new spike pulse can be generated.

B. S*ilicon Synapse:*

Synapses are highly specialized structures that, by means of complex chemical reactions, allow neurons to transmit signals to other neurons. When an action potential generated by a neuron reaches a presynaptic terminal, a cascade of events leads to the release of neurotransmitters that give rise to a flow of ionic currents into or out of the post synaptic neuron's membrane. An integrator circuit implements a simplified model of a real biological synapse: as input pulses arrive at the synapse, they are integrated such that the circuit's output current encodes the frequency of the input spike train. Synapses can be excitatory or inhibitory. These excitatory or inhibitory post synaptic currents (EPSC or IPSC, respectively) have temporal dynamics with a characteristic time course that can last up to several hundreds of milliseconds [6].

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Dynamical synapses can be depressing, facilitating, or a combination of both. In a depressing synapse, the synaptic strength decreases after each spike and recovers towards to its maximal value with a time constant, T_d . In facilitating synapses, the strength increases after each spike and recovers towards to its minimum value with a time constant, T_j [7].

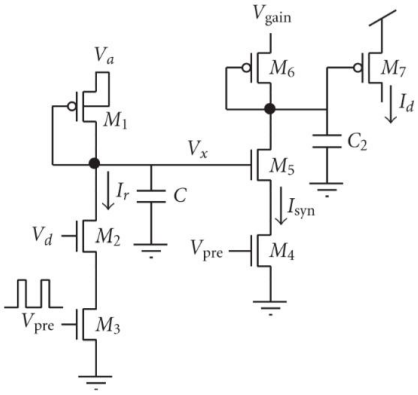

Fig. 3. Depressing Synapse [7]

In the depressing synapse the voltage V_a determines the maximum synaptic strength while I_{syn} is exponential in the voltage, V_x. The sub circuit consisting of transistors, M1, M2, M3, control the dynamics of I_{syn}. The presynaptic input goes to the gate terminal of M3 which acts like a switch. During a presynaptic spike, a quantity of charge (determined by V_d) is removed from the node V_x, In between spikes, V_x recovers towards V_a through the diode-connected transistor M1. Also during the presynaptic spike, transistor M4 turns on and the synaptic current I_{syn} into the membrane potential of the neuron. We can convert the Isyn current source into an equivalent current I_d with some gain and a "time constant" through the current-mirror circuit consisting of M6, M7, and the capacitor C2, and by adjusting the voltage V_{gain}.

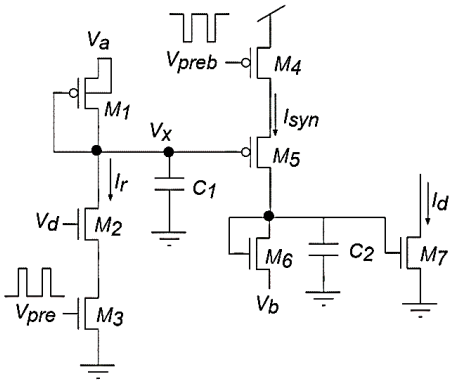

Fig. 4. Facilitating Synapse [7]

The circuit in fig.4 on the left is the same as part of the circuit in Fig.3. The voltage Vx determines the synaptic strength and the current Id goes to the neuron. The diff erence in this circuit from the depressing synaptic circuit is that the node Vx goes to the gate of a pFET instead of an nFET. This circuit would be have to be inverted so that it can be combined with the neuron circuit. The facilitating synapse acts like a low-pass filter to changes in spike rates. A step increase in presynaptic firing rate leads to an increase in the synaptic strength. Both types of synapses can be treated as time-invariant fading memory filters.

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C. Communication in Artificial Neural System

To demonstrate the communication between a synapse and a neuron we implemented the integration of Linear Threshold Integrate & Fire Neuron and the depressing synapse mentioned in section III A & III B respectively. The synaptic current I_s injected into the neuron part is a depressing type current. Output pulses V_{out} were fired at fixed intervals with membrane voltage V_{mem}. The firing rate of the neuron decreases over time and eventually the signal is suppressed due to the decrease in the post synaptic input as the neuron is fired by a depressing synapse.

IV. SIMULATION RESULTS

Simulations were performed on this circuit using Spice CMOS 2micron technology. By adjusting parameters like the synaptic weight, capacitor values and threshold values the output waveforms were observed as shown in fig.6.

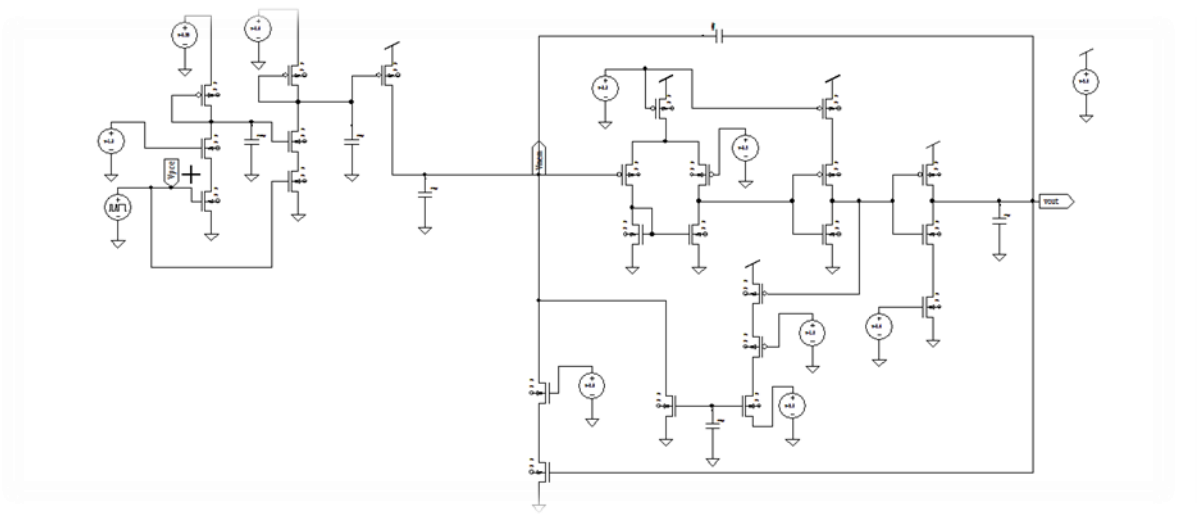

Fig. 5: Spice Simulation of Neuron Synapse Integration

The input to the synapse is a spike train with a frequency of 100Hz (V_{pre}). The synaptic current Id injected into the neuron part is a depressing type current as shown in fig. 5. Output pulses V_{out} were fired at fixed intervals with membrane voltage V_{mem}.

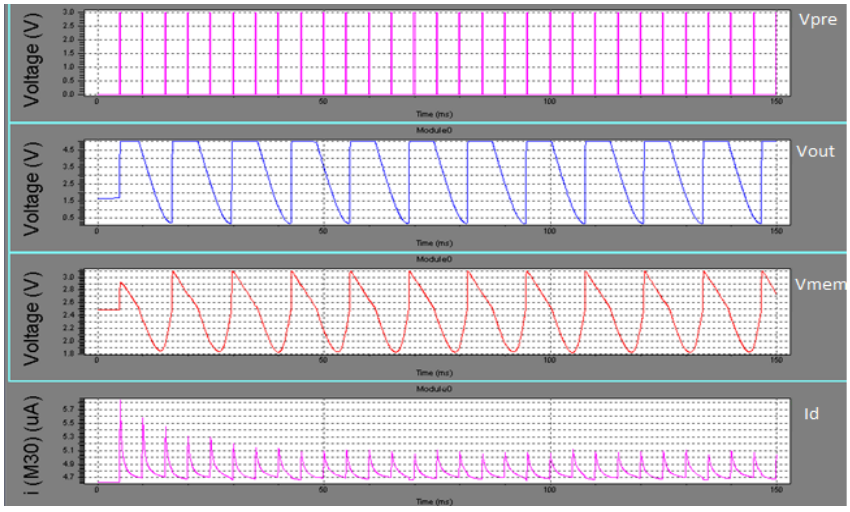

Fig. 6: Output of synapse and neuron integration.

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The firing rate of the neuron decreases over time due to the decrease in the post synaptic input as the neuron is fired by a depressing synapse. The synaptic current (Id) obtained at the output of the synapse decreases after every spike input and the current comes to a steady state. The time taken by the current to come to the steady state is dependent on the synaptic weight. This synaptic current is injected into the neuron. V_{mem} was generated at regular intervals depending on the value of the synaptic current. As V_{mem} crosses the threshold voltage V_{thr} output spike pulses V_{out} were generated as shown in the fig.6.

III. CONCLUSION AND FUTURE WORK

The simulation results showed that output pulses Vout were fired at fixed intervals with membrane voltage V_{mem}. Communication between neurons and synapses can be shown using various Neural Network Algorithms like Address Event Representation (AER), Back propagation algorithm, Winner-Take-All (WTA), etc. In our work we have implemented synapse circuits with constant weight but in case of long term plasticity, the weight is determined by both the presynaptic and post synaptic activity. The VLSI circuits that implement such learning rules range from Hebbian rules to spike-timing dependent plasticity.

With the advancements in CMOS technology there are various other technologies in which neural networks are being implemented such as the Floating-gate synapse, Optically Gated Carbon Nanotube FET (OG-CNTFET) Synaptic Device, The Carbon Nanotube Synaptic Circuit and the memristor based synaptic devices.

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BIOGRAPHY

Dr. V.C.Kotak obtained his Ph.D. from VJTI, Mumbai. He has competed his M.E. from VJTI, Mumbai. He is Senior Member of IEEE, Life Member of ISTE, CSI and Fellow Member if IETE. He is the Membership Development Chair at IEEE Bombay Section, Region 10 and in the past he has been Chair of Student Activities Committee as well. He is currently Vice Principal at Shah and Anchor Kutchhi Engineering College, Mumbai, India and also acting Principal. He is Dean of Resource Mobilisation and Planning as well as Head of Training and Placement Dept. He has more than 27 years of Teaching Experience. His research interests are Coding Theory, Data Communication and Networking, RFID and its applications.

Prof. Sushma Srivastava obtained her M.E. in Microelectronics in 1991 from BITS Pilani. Her research interests are VLSI, Nanotechnology and Neuromorphic Engineering.

Madhuri Gala is pursuing M.E. in Electronics Engineering, Shah and Anchor Kutchhi Engineering College, Mumbai University She received Bachelors of Engineering (B.E.) degree in 2011 from Shah and Anchor Kutchhi Engineering College, Mumbai University. Her research interests are VLSI and Neuromorphic Engineering.

Shilpa Pandhare is pursuing M.E. in Electronics Engineering, Shah and Anchor Kutchhi Engineering College, Mumbai University She received Bachelors of Engineering (B.E.) degree in 2009 from Shah and Anchor Kutchhi Engineering College, Mumbai University. Her research interests are VLSI and Neuromorphic Engineering.