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Low Power Enhanced Speed Dual Edge Pulse Triggered Flip-Flop Based On Signal Feedthrough Scheme

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ABSTRACT: Flip-flops and latches are the critical elements contributing in performance of the VLSI circuits. Pulse triggered flip-flop are not complicated in circuitry as they have a single latch design. Explicit pulse triggered flip-flop provides high speed operation due to higher toggle rate.This paper presents an efficient dual edge pulse triggered Flip-flop (P-FF) design in terms of power consumption and speed. The Proposed design features pulse generator based on NAND-logic that can be shared among flip-flops to reduce power dissipation and a unique modified true single phase clock latch (TSPC) based on a signal feed-through scheme. The design successfully reduces the transistor sizes in discharging path. Adoption of Conditional discharging technique causes reduction in internal switching activity. The simulations are carried out in tanner tool software using 180nm CMOS Technology. The proposed design provides solution to the long discharging path problem resulting in improved speed and power performance.

KEYWORDS: flip-flop (FF), pulse triggered, dual edge, low power, signal feedthrough.

I. INTRODUCTION

In VLSI circuits Flip-Flops are used to design counter, shift register and Integrated Circuits etc. Flip-Flops are basic storage and timing elements in VLSI circuits having a great impact on circuit power consumption as well as speed. The Power delay product of a Flip-flop can affect the system's overall performance. Hence the design in the Flip-flop with low power dissipation and low propagation delay improves the modern digital design to greater extent. Clock system consists of clock generator, storage element and clock distribution network. Thus Power consumed by the clock system is up to 30% to 60 % of the total power consumed by system. To overcome this problem a triggered based Flip-Flop is implemented.

Pulse-triggered flip-flops (P-FF) are characterized by an uncomplicated structure, negative setup time; soft edge and higher toggle rate giving improved performance over traditional master slave flip flop. P-FF has less number of clocked transistors. Pulse triggered flip-flops can be static, semi-static, dynamic or semi-dynamic. P-FF made up of a pulse generator for producing strobe signals and a latch part for storing data and are classified into two types, Implicit-pulsed in which pulse generation is incorporated in latch part and explicit-pulsed in which pulse generator and latch are separate[1].Implicit type P-FF is more power economical but suffers from inferior timing characteristics. In explicit type flip-flop, logic separation from latch design gives a unique speed advantage. Also circuit complexity and power consumption can be reduced when one pulse generator is shared among the group of flip-flop.

Flip-flops are used to store the data so that this stored data can be applied to other sequential or combinational circuits. In single edge triggering we are able to store the data either at rising edge(0 to 1 transition) or falling edge (1 to 0 transition).Thus the output will change only at the triggered edge otherwise it will remain unaffected in spite of change in input. In dual edge triggering, output will change at both the rising as well as falling edge resulting in lower clock frequency.

In this paper we present a low power and high performance Dual edge explicit pulse triggered flip-flop design which is based on a signal feedthrough scheme. Here the internal node of the latch design is feed directly with input

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signal to fasten the data transition. A simple pass transistor is introduced to implement the mechanism which provides extra signal driving .when it is combined with pulse generation circuitry, gives enhanced speed and PDP performances. Use of dual edge triggering along with extra pull up NMOS transistor acts as a current limiter by passing the current only when clock is enabled resulting in lower power consumption in a circuit.

II. CONVENTIONAL EXPLICIT TYPE P-FF DESIGNS

Explicit Pulse triggered Flip-Flop made up of Pulse generator for generating the pulse explicitly and a Latch network. Pulse generator circuit generates a short pulse around the rising (or falling) edge of the clock. This short pulse is given as clock input to a latch. Thus in this short window, Sampling of latch is done. To provide a fine comparison there are few existing designs are discussed.

A. Explicit-Pulse Data-Close-to-Output (ep-DCO) Flip-flop

Due to its semi-dynamic true-single-phase clock (TSPC) structured latch, it is considered to be the fastest FF[1]. The pulse width is determined by delay of three inverters. Explicit Data Close to output Flip-Flop suffers from large switching power dissipation problem due to discharging of internal node on each rising edge of clock whenever it has static input 1 case. This flip-flop does not produce any useful operation at internal node resulting in more power consumption.

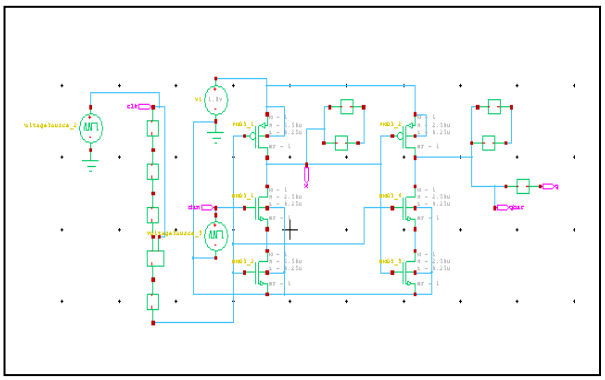

Fig.1. ep-DCO

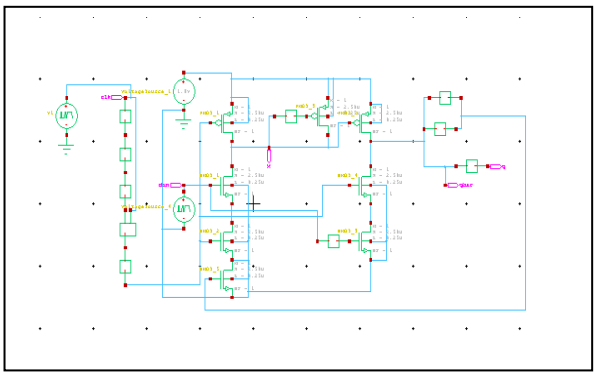

Fig.2 CDFF

B. Conditional Discharge Flip-flop (CDFF)

Conditional discharge mechanism is introduced to reduce power dissipation [3]. An extra NMOS_5 transistor is employed which is controlled by the output feedback signal Q_fdbk. Thus if the input data remains "1" no discharge occurs. But this design Suffers from worst case delay caused by longer discharging path. Keeper logic for internal node is simplified by having only inverter and a pull up pMOS transistor.

C. Static Conditional Discharge Flip-flop (S-CDFF)

S-CDFF which is shown in fig (3) uses static latch structure and thus differs from the CDFF. It doesn't consist of periodical precharges of internal node [4]. It is having a longer data-to-Q delay as compared to CDFF design. The three transistors NMOS_1- NMOS_2 - NMOS_5 constitutes a discharging path which results in worst case delay. A larger data-to-Q (D-to-Q) delay is exhibited by S-CDFF design as compared to the CDFF design.

A. Modified Hybrid latch Flip-flop (MHLFF)

To overcome worst case delay problem caused by discharging path consist of three stacked transistor MHLFF is introduced [8]**.** In this flip flop the keeper logic at internal node is removed. Though, this circuit is simple, it encounters two drawbacks. MHLFF drawback is that internal node x becomes floating in cases when output Q is '1'and input Data also equal to'1' resulting in extra dc power. A long 0 to 1 delay is expected since the node *X* is not predischarged.

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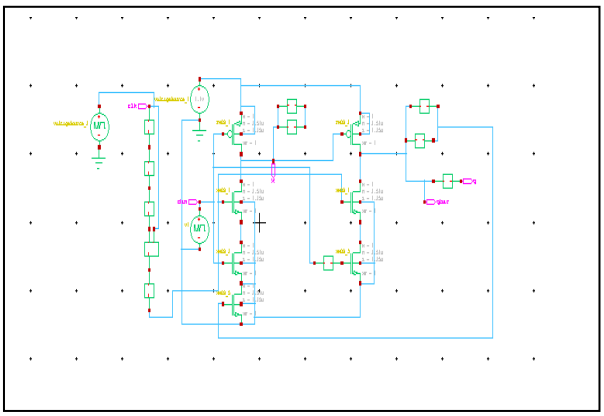

Fig.3 S-CDFF

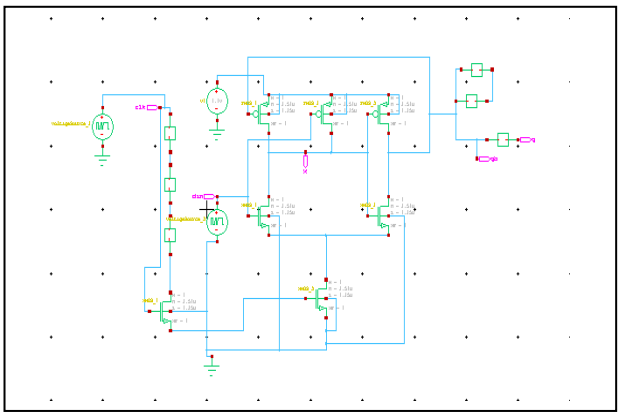

Fig.4 MHLFF

III. PROPOSED SIGNAL FEEDTHROUGH SCHEME FOR SINGLE EDGE TRIGGERED FLIP-FLOP

The four reviewed Conventional designs which use basic TSPC latch structure faced the worst case timing occurring at 0 to1 data transition. In proposed design signal feedthrough scheme is adopted for improving the delay.

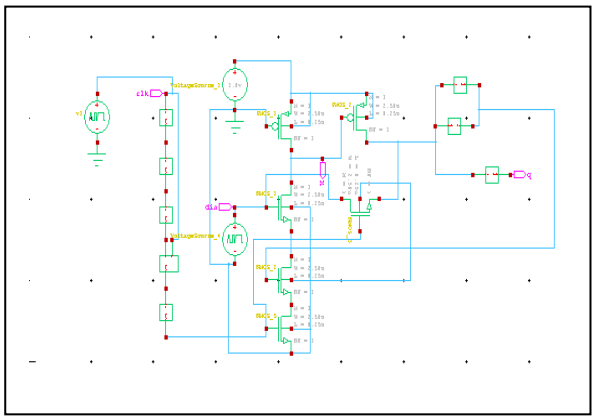

Fig.5 Proposed single edge triggered Flip-Flop

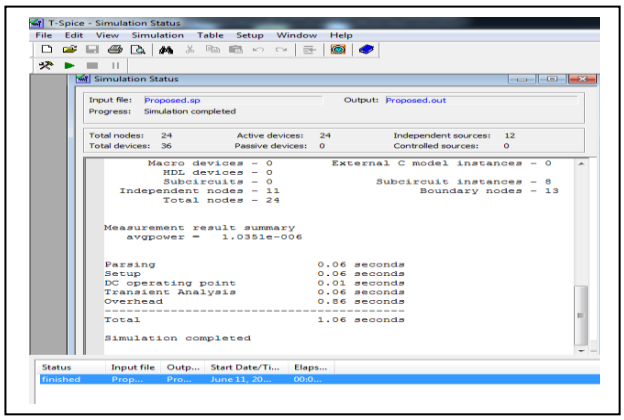

Fig.6 simulation output of proposed FF

This design avoids superfluous switching at an internal node by using a unique TSPC latch in terms of three aspects:
1. The pseudo-nMOS logic style design is obtained by using a weak pull up pMOS_1 transistor having gate connected to ground. Thus circuit saving of the proposed design includes charge keeper circuit which is required for the internal node in existing designs.
2. Pass transistor NMOS_3 which is controlled by pulse clock is included to provide the signal feedthrough so that input data can drive output node of latch directly.
3. The pass transistor provides extra driving to output node of latch during 0 to 1 transition and also provides the discharging path for the node during 1 to 0 data transition. Also the load capacitance of internal node is reduced.

Working:

1. No data transition: In this case, when a clock pulse arrives, level of the input data and output node of the latch (Q) is same. Thus there will be no driving effort in the input stage of the FF as only the on current is passed through Pass transistor NMOS_3. At the same time, in internal nodes, there is no signal switching because

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Complementary signal levels are assumed by input data and the output feedback and The pull-down path of internal node is off.

2. '0' to '1' data transition: The transistor PMOS_2 is turned on due to the discharge of internal node x hence the output node of the latch is pulled to logic '1'.During the pulse duration period, discharging path is conducted .This is the worst case timing in the operation of flip-flop .But a boost is provided via pass transistor NMOS_3 from input source (signal feedthrough) to shorten the delay.

3. '1' to '0' data transition : when a clock pulse arrives transistor NMOS_3 is turned on and output node of the latch is discharged through this transistor.

IV. PPROPOSED DUAL EDGE TRIGGERED FLIP-FLOP

The flip-flop consists of NAND logic based pulse generator and a unique modified TSPC latch based on a signal feed through scheme. By maintaining the same data throughput, dual edge-triggered flip-flops manages to reduce the clock frequency to half that of the single edge-triggered flip-flops. In this Flip-flop only the latch part is duplicated to provide the upper data path and lower data path .Here one path is used for positive triggering and another path is used for negative triggering A single pulse generator is used to feed the pulses to latch part. The proposed flip-flop consumes lower power as compared to conventional designs as an extra pull up nMOS transistor with one end connected to source and drain connected to ground acts as a current limiter by allowing the current to pass only when the Clock is '1' .The proposed flip-flop provides enhanced speed operation with lower power consumption.

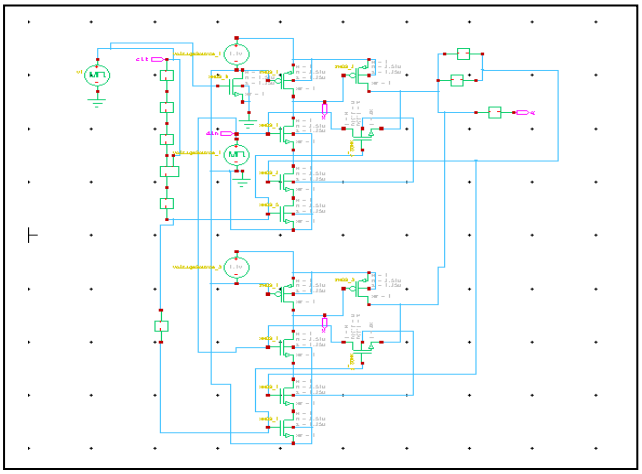

Fig.7 Proposed dual edge triggered FF (DETFF)

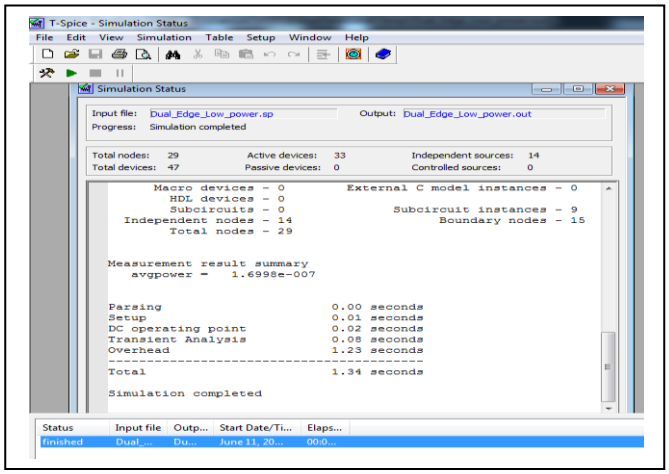

Fig.8 Simulation output of Proposed DETFF

V. SIMULATION RESULTS

In this paper different flip-flop structures are designed in s-edit of tanner tool and compared .we have used TSPICE simulation with 180nm CMOS technology files using operating condition with frequency 50MHz and supply voltage 1.8V. All the Pulsed Flip-flop Presented in paper uses NAND logic based pulse generator except MHLFF. Considering the simulation results it is observed that the proposed flip-flop have lower power consumption and low data to Q (D-Q) delay. In Table I the proposed single edge triggered design is compared with existing explicit P-FF designs. Average power consumption of the flip-flops is calculated for 100% switching activity by using test data pattern as10101010 and for 50% switching activity by using the test data pattern as 111000111000.It is observed that average power consumption of ep-DCO is highest due to discharging of internal node at every rising edge and the proposed design has a lower power consumption as compared to other designs in both 100% as well as 50% switching activity. Also the delay of the proposed design is greatly reduced. The design is having less no of transistor and lower PDP which is suitable for high speed application.

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Table.1.comparison of various P-ff Designs

sr. no	P-FF design	ep-DCO	CDFF	SCDFF	MHLFF	Proposed single edge triggered
1	Delay(ns)	1.36	1.36	1.70	1.53	1.19
2	P_{avg}(μW) (β=100%)	789.5	108.92	19.249	214.33	1.0344
3	P_{avg}(μW) (β=50%)	792	101.47	10.29	95.22	0.985
4	Transistor count	28	30	31	19	24
5	PDP(fJ)	1073.7	148.13	32.72	327.92	1.23

Table.2.comparison between Proposed Single Vs Dual edge Design

Sr.No	P-FF Designs	Delay (ns)	P_{avg}(μW) (β=100%)	Transistor count	PDP(fJ)
1	Proposed single edge triggered	1.19	1.0344	24	1.23
2	Proposed dual edge triggered	1.02	0.16998	33	0.1733

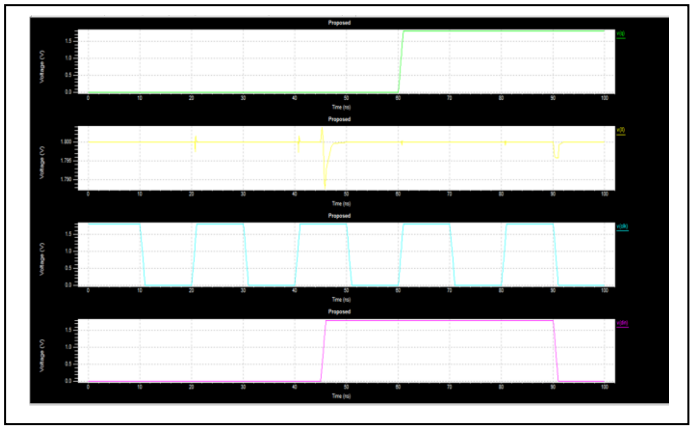

Fig.9 simulation of proposed single edge FF

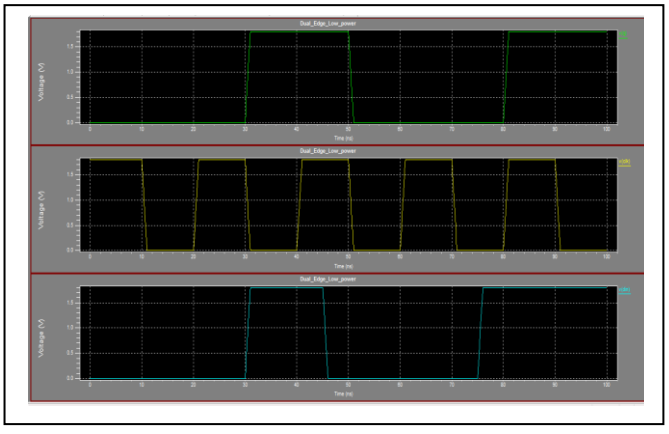

Fig.10 simulation of proposed DETFF

Table 1 shows that due to the use of signal feedthrough scheme, the proposed single edge triggered design is efficient in terms of power consumption and delay. Table II shows that the proposed dual edge triggered design is having more enhance speed and power consumption than single edge triggered design. Also the PDP of Proposed DETFF is very low .hence the flip-flop is suitable for faster applications. The simulation waveforms of the proposed single edge and dual edge flip-flops(Fig.9 and Fig 10) shows that dual edge can sample the data on both positive as well as negative edges hence, requires lower frequency as compared to the single edge Flip-flops.

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VI. CONCLUSION

In this paper various pulse triggered flip-flops are discussed and compared. We presented a single edge triggered and dual edge triggered flip-flop designs based on signal feedthrough. The main aim was to supply a signal feed through to the internal node of the latch from input source directly, which would make possible additional driving to cut down the transition time and improve both power and speed performance. Design of the dual edge triggered flip-flop was achieved by using a simple pass transistor to provide signal feedthrough and addition of extra pull-up nMOS transistor helps to lower the power of the design. From the comparison table I, II it is clear that proposed design has least delay, power switching activity and Power delay product (PDP) in comparison with all discussed flip-flops. Thus incorporating a signal feedthrough scheme along with a dual edge triggering and nmos transistor as a current limiter gives an efficient flip-flop design.

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