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Design and Implementation of Smart Error Detecting Network on Chip Based Router Architecture

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ABSTRACT: Recently Networks on Chip (NoC) is playing vital role in development in VLSI. Network on Chip (NoC) can be one of the solutions for faster on chip communication. For efficient communication between devices of NoC, routers are needed. In this paper, a low- area and power efficient NoC architecture is proposed by eliminating the input and output buffer. Buffers are replaced by elastic buffer. It is based on error detection mechanism suitable for dynamic NoC's. The advance reliable network consists of router with separate routing logic block and error correcting mechanism. In this paper the proposed router architecture replaces FIFO buffers with the elastic buffers in order to reduce area, and power consumption and also to have better performance. Here performance is evaluated on the basis of power and delay product.

KEYWORDS: Network on chip (NoC), reliable router, elastic buffer,VLSI.

I.INTRODUCTION

To solve the problem of the traditional bus in the area interconnect scaling and power consumption, etc., a new on-chip communication structure Network-on-Chip has been proposed[1]. Networks-on Chips (NoC) is a bridge concept from Systems on-Chip (SoCs) into Multiprocessor System-on-Chip (MPSoC). As the scalability of Chip Multiprocessors (CMPs) increases, the Network-on-Chips (NoCs) architectures must overcome the problems of global wire delay and power consumption. As a consequence, the main feature of NoC is the use of networking technology to establish data exchange within the chip. Clearly, energy-efficient and fault tolerant NoCs architectures are required to sustain the performance gains.

Router is the most important component for the design of communication back bone of a NoC system. In a packet switched network, the functionality of the router is to forward an incoming packet to the destination resource if it is directly connected to it, or to forward the packet to another router. It is very important that design of a NoC router should be as simple as possible because implementation cost increases with an increase in the design complexity of a router [2]. Three research areas to improve NoCs architectures include (a) buffering and switching to improve energy-efficiency, (b) topologies designed for high throughput, and (c) fault tolerance for robust or reliable performance.

One of the main challenges of NoC is that it has to face the dynamically placed reconfigurable devices into dynamic NoC [3]. Configurable network was designed to obtain dynamic reconfiguration of FPGAs. An NoC comprises routers and interconnections allowing communication between the PEs or IPs. The NoC relies on data packet exchange. The path between the source and the destination is defined through routing algorithms. The most suitable routing algorithm for mesh network is XY algorithm, but it cannot be used to avoid both dead lock and live lock. To overcome the above limitations, adaptive routing logic is used that updates the information about the neighbouring router. Adaptive XY

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routing algorithm includes the concept of Odd-Even algorithm [4] and XY algorithm well suited for a NoC which uses dynamically reconfigurable devices . Adaptive XY routing algorithm is used in this architecture.

Reliable router can detect faults in the data packet during transmission. These faults may affect due to data packet errors or permanent routing errors. Routing errors can be detected by Routing Logic block. To detect these faults, specific error detection blocks are required in this architecture. The data transmission with minimum error that can be achieved by the inclusion of error correcting techniques in the router. It is includes correcting of error occurng in the transmitted data using hamming codes. Error correcting codes (ECCs) are implemented inside the NoC components, to protect data packets against errors. Error detection and correction blocks present in the router architecture. Different types of error detection and correction techniques used in NoC are end to end, switch to switch and code disjoint techniques. Switch to switch error detection and correction technique is used in this paper. The switch-to switch detection is based on the implementation of an ECC in each input port of the NoC switches. For eample, four ECC blocks are implemented in a router of four communication directions (North, South, East, and West). Therefore, the ECC block analyzes its content to check the correctness of the data, when a router receives a data packet from a neighbor. This process detects and corrects data errors according to the effectiveness of the ECC being used.

Input and output buffers in router architectures are replaced by elastic buffers. The input and output buffers of router increase the power budget and chip area. Eliminating input and output buffers is a natural approach to design low-power NoCs or reducing the number of input and output buffers overhead degrades the network performance. In this paper, the proposed router architecture replaces FIFO buffers with the elastic buffers in order to reduce area, and power consumption and also to have better performance.
The rest of this paper is organized as follows: Section II describes related work. Section III presents Proposed Architecture. Section IV discuses routing error detetion . The experimental results and performance evaluation are presented in Section V. Section V present applicaton of NoC. Finally, conclusion is drawn in Section VII.

II. RELATED WORK

In order to meet the real time applications the trend of embedded system has been moving towards Multiprocessor System on Chip (MpSoC), where the number of SoC is more. Increasing the number is becoming a burden for connecting medium. Connecting the SoC's through NoC gives an effective connection between the peripherals. The peripherals were connected through a shared bus in the earlier period, which can be either single or multiple shared busses connected using bypass bridges and point-to-point connection between the peripherals [5]. This development of connection led to network on chip, where the peripherals are connected by splitting into certain sub circuits via NoC .One of the main challenges of NoC is that it has to face the dynamically placed reconfigurable devices which later emerged into dynamic NoC .Configurable network was designed to obtain dynamic reconfiguration of FPGAs. The NoC is further modified to improve the performance and manage the dynamically placed modules using the inclusion of certain switching techniques. Now the focus is towards the data transmission with minimum error that can be achieved by the inclusion of error correcting techniques in the router. In error correcting code is included only on any two ports of the router among the four, and it is further incorporated with all the four ports to improve the performance of NoC .The path between the source and the destination is defined through routing algorithms. The most suitable routing algorithm for mesh network is *XY* algorithm, but it cannot be used to avoid both dead lock and live lock. To overcome the above limitations, adaptive routing logic is used that updates the information about the neighbouring router .Adaptive *XY* routing algorithm includes the concept of Odd-Even algorithm and *XY* algorithm well suited for a NoC which uses dynamically reconfigurable devices.

III. PROPOSED ARCHITECTURE

The proposed architecture is modified RKT-NOC switch; it will overcome both dead and live locks. The figure of the modified RKT-switch is shown in fig 1. It is suitable for a 2-d mesh NoC, having four directions (north, south, east, and west) and the PES and IPS can be connected directly to any side of a router. So, there is no specific connection port for a PE or IP. Each port direction is composed of two unidirectional data buses (input and output ports).The proposed algorithm having no of blocks, they are loopback module, ECC, routing error detection, routing logic, elastic buffers, and control signals.

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The majority of current NoCs spend considerable area and power for router buffers. Here developed elastic buffer (EB) which adds simple control logic in the channels to use pipeline flip-flops (FFs) as EBs with two storage locations. This way, channels act as distributed FIFOs and input buffers are no longer required. Removing buffers which significantly simplifies router design. Area and power consumption can be reduced by using this elastic buffer. This has motivated to reduce or eliminate buffer cost.

The reliable switch operation s based on store and forward method. Store and forward is a technique in which, at each node the packets are stored in memory and the routing information examined to determine which output channel to direct the packet. This is why the technique is referred to as store-and-forward (SAF). This technique is suitable for dynamically reconfigurable NoCs.

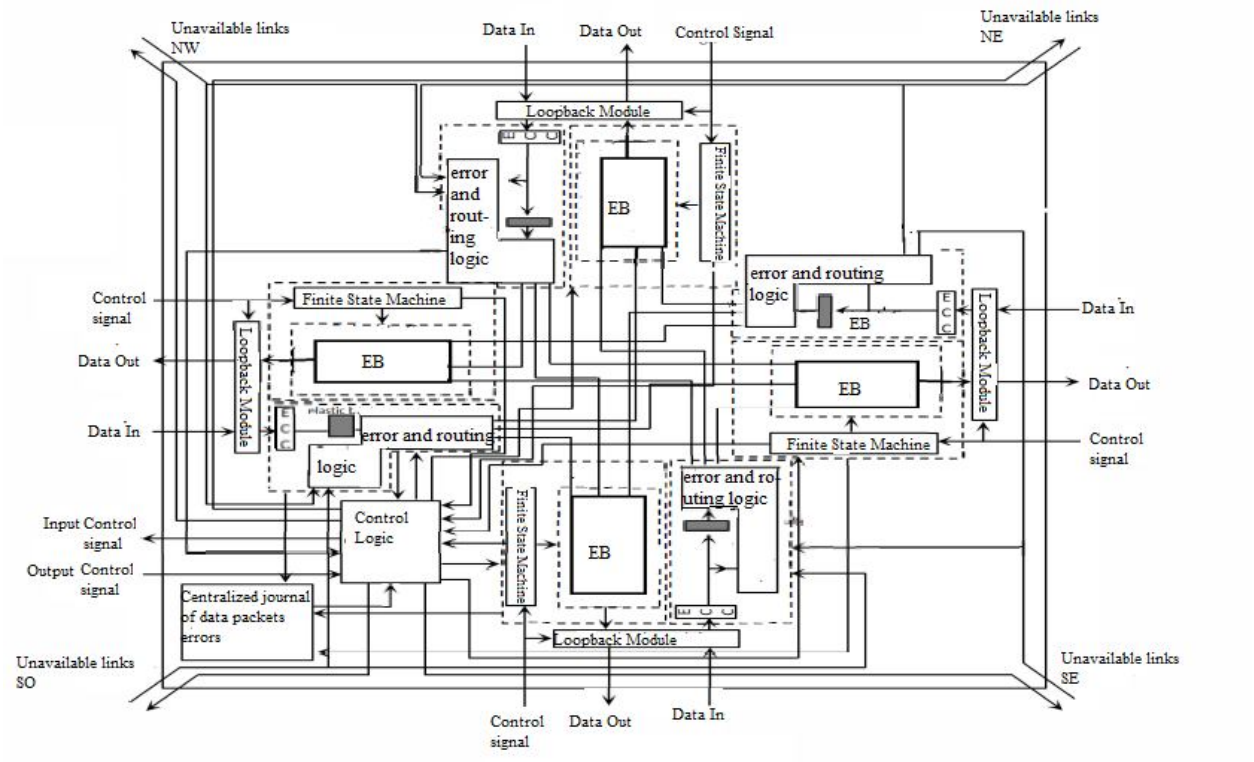

Fig. 1. Reliable router architecture

A.ELASTIC BUFFER

Elastic buffer (EB) was proposed to eliminate router buffers while preserving buffering in the network [5]. Figure 2(a) shows a D flip-flop (DFF) [6] that is implemented using master and slave latches. By adding control logic to drive the latch enable pins independently. Each latch can be used as an independent storage location. Thus, the FF becomes an EB, a FIFO with two storage locations. This is illustrated in Figure 2(b).

Sequene EB channels to act a distributed FIFO. FIFO storage can be increased by adding latches to EBs or by using repeater cells for storage. EBs use a ready-valid handshake to advance a flit (flow-control digit).An upstream *ready* (R) signal indicates that the downstream EB has at least one empty storage location and can store an additional flit. A downstream *valid* (V) signal indicates that the flit currently being driven is valid. A flit advances when both the ready and valid signals between two EBs are asserted at the rising clock edge.

EB is responsible to eliminate the associated area and energy cost. EB is used in this proposed reliable router architecture can be replaced with lightweight EB architecture – ElastiSore [7] to support multiple Virtual channels.

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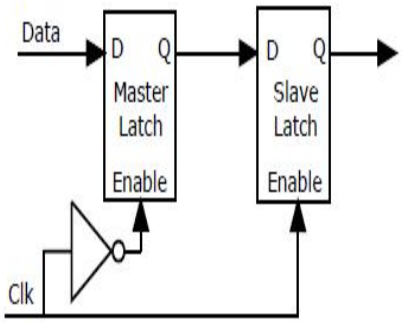

Fig 2(a). A DFF implemented with a master and a slave D latch.

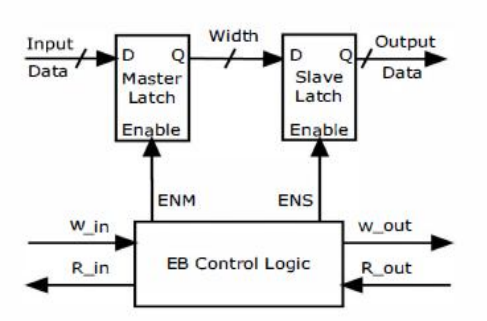

Fig 2(b). Elastic buffer

B.ROUTING LOGIC

Routing acts as the backbone to avoid deadlock and live lock. The routers have the address in the matrix format i.e., it is defined by its XY coordinated. There were two types of logic used namely Deterministic and adaptive or both the types can be combined to be used for dynamic reconfigurable network structure. A deterministic routing algorithm provides a unique path from a source to destination. Adaptive routing algorithm routes adaptively, if there is an obstacle or fault in switch. Adaptive XY routing algorithm is used for routing.
Adaptive XY routing algorithm has

1) XY-routing first routes packets along the X-axis.
2) Once it reaches the destination's column, the packet is then routed along the Y-axis until the destination's line.
3) Any packet moving in the Y direction can never return to the X-direction.

Error logic will identify the error in the routing path. This routing logic will follow a loopback module to avoid deadlock and live lock.

C.ERROR CORRECTION (ECC)

Transmission of data without any error in the NoC ensures integrity of data. To guarantee error free transmission of messages, the error correcting techniques is included in the switch to avoid both routing error and data error. This paper uses hamming code for data error checking, which has the tendency to check burst errors. If error occurs then it sends a Nack to the source requesting for retransmission. Each switch is identified by a unique address mentioned in matrix form. When a message is passed from one IP core to another IP core via switch, it checks the status of the flits received. Flits received through the loop back mechanism indicate that the router ahead is faulty. The flits routed by

XY algorithm states that the router ahead is not faulty. If adaptive XY algorithm is used then the flits are received to bypass the faulty router. The availability of the next router is determined by checking the status of the availability signal along the diagonal direction. Thus the routing error detection mechanism is highly suitable to avoid both dead

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lock and live lock, Deadlock is a situation that occurs when a packet is waiting for an event that can never happen because of circular dependence on resources**.** Livelock, on the other hand, is a configuration of the network in which packets continue to move, but never reach their destination.

D.LOOPBACK MODULE

The RKT switch consists of a loopback module block which is used to make a new path for the packets by looping back through another port. It is done if and only if the current router found any fault in the neighbour router to which the packet has to be sent.
In a dynamic reconfigurable NoC, position and number of components in the network can change during the reconfiguration time. During reconfiguration, reconfigurable area is deactivated as well as faulty routers are also isolated. If reconfigurable region or faulty region is present in the routing path, data packet may get lost. Therefore the data packet cannot reach the destination. To overcome this drawback the router architecture contain output buffer associated with this module. The role of loopback module is to empty the buffers of loopback module for each output port by looping back the data packet in to the input port of the router. Then looped back packets are rerouted towards another output port of the router. The loopback module [8] avoids data packet getting trapped or data packet loss.

A loopback module is implemented in each of the four ports of the router. The architecture of the loopback module is depicted in Fig. 3. In the operation of loopback module it initially checks the data request in signal from the router it has to send the packet if it is high and the unavailability link is low then the control logic block checks the availability of nearest router to transmit data packets. Data packet is loop backed, if nearest router is unavailable or if there is fault in a nearest router. If no loopback is needed, a semi-crossbar switch connects the buffer to the data out signal in order to send data packet towards the nearest router and sets the data _request_out signal. Then mux connects the input data bus in to data in bus. When a loopback is required the logic control block configures the semi-crossbar block to send the considered data packet on the data_loopback bus. Therefore, the data packet is looped back inside the router and will be considered as a new packet. At the time of looping back the signal there is a chance for making a delay in receiving the data through that port to avoid this at the time of looping back the data the occ_out is activated to stop sending data to that particular port from the neighbour.

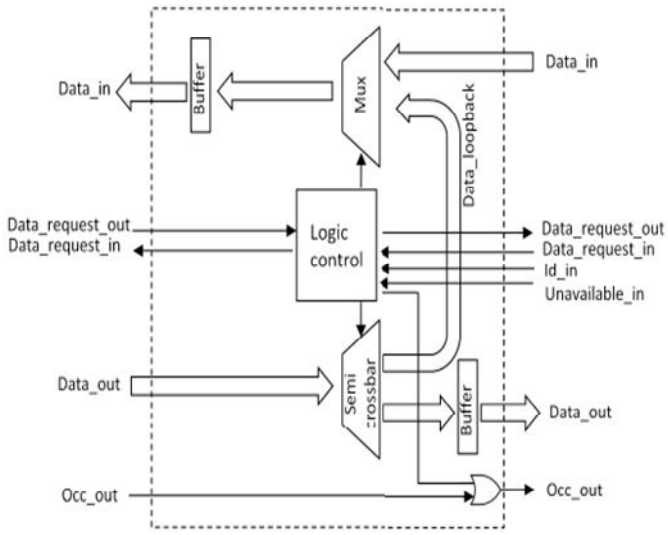

Fig 3. Architecture of loopback module

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IV. ROUTING ERROR DETECTION

The occurrence of error is not only due to the change in the value of the message being sent it also occur due to the wrong routing path.
Adaptive XY routing algorithm is used.The main difficulty in routing error detection is to distinguish a bypass of an unavailable component in the NoC from routing error. Non detection of routing errors is the possible loss of data packets being sent. This routing error detection is performed in parallel after the Hamming ECC. Routing error detection is achieved by using three components. These are diagonal availiability indication, journal of routing error, and informations on data packets. Component required for routing error is given below:

A.Diagonal availiability indication

Reliable router uses information links to indicate the availability status of the neighbour. if a router input port is permanently faulty, it is disabled while maintaining the other input ports as active. if all input ports are faulty, the router is considered as unavailable. Unavailable means the router that cannot receive data packets due to permanent faults. The reliable router indicates its availiability status to the eight direct neighbouring routers through the diagonal availiability indication (DAI). It checks the correctness of the routing algorithm.

B. Journal of routing error

The journals are related to the routing logic blocks of the neighboring router connected to the considered input port. Each routing error detection block has three journals to keep the routing error detection results. These journals differentiate the permanent and transient errors.Some conditions are:

a) If all the bits are in set state, it indicates permanent error.
b) If all the bits are in zero state, it indicates no error in the routing.
c) If any bit is in one state, it indicates there is a error in the routing.

C. Informationfield in the data packet

Information field includes flit type, source address, destination address and unique path identification bit. Flit type bit indicates whether it is data or header. Header includes the information about the routing. Flit type is one bit. Source and destination address are 4 bit for 4x4 mesh network. If there is only single path is availible for routing, then unique path identification bit will be set and it does not show routing error.

V. RESULTS AND PERFORMANCE EVALUATION

A.Simulation Results and Performance Evaluations

The designed NoC architectures are simulated and the required parameters are calculated using the tool ModelSim, which is used as a simulation and debugging tool for verilog.

In this designed reliable NoC the message takes an alternative path to reach the destination if there is any fault in the path through which it has to transmit the message, thus the message reach the destination even the router in the transmitting path is faulty.

The main advantage in this designed router is that the message can reach the destination even there is fault in the path through which the message travels .

TABLE I shows the area and power analysis of reliable router architecture with elastic buffer and reliable router architecture with FIFO buffers. Area and power of reliable router architecture with elastic buffer and FIFO buffer is compared.

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TABLE I. AREA AND POWER ANALYSIS

Reliable Router	Area	Power
With elastic buffers	52.75418μm^2	841.256uW
With FIFO buffers	130.56842μm^2	1673.46uW

B.Synthesis Results And Performance Evaluations

In this paper the performance of reliable network architecture is analyzed based on packet throughput and packet latency.

l)Packet throughput

The packet throughput is the rate at which the packet traffic can be sent across the network. For packet passing system, the packet throughput TP is defined as the ratio of (Total packets completed x packet length)/(Number of IP blocks x Total time)

$$TP = \frac{\text{(Total packet completed) * (Packet Length)}}{\text{(Number of IP blocks) * (Total Time)}}$$

Where Total pa y arrive at their destination processing cores, packet length is measured in flit, number of processing cores is the number of functional processing cores involved in the communication, and total time is the time that elapses between the occurrence of the first packet generation and last packet reception. Thus, throughput is measured as the fraction of maximum load that the network is capable of physically handling. Throughput signifies the maximum value of the accepted traffic and it is related to the peak data rate sustainable by system. Comparison of packet throughput with elastic buffer and FIFO buffer is given in TABLE II.

2)Packet latency

Transport latency is defined as the time (in clock cycles) that elapsed from between the occurrence of head flit injection into the network at the source node and the occurrence of the tail flit reception at the destination node. In order to reach the destination node from some starting source node, flit must travel through a path consisting of a set of routers and inter connects. Each packet may have a different latency. Therefore for a given packet P and latency L is defined as

L= received time -sending time.

TABLE II. PACKET THROUHPUT AND LATECY ANALYSIS

4X4 Mesh network	Packet throughput	Packet latency
With elastic buffer	1.68x 10^6 bit/s	1180ns
With FIFO	1.29x 10^6 bit/s	1565ns

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VI. APPLICATIONS

- The most important application is it uses hamming code for error detection and correction .So,it helps in online detection of faulty nodes in NoC.
- It is used in Network Hub for fast error free data communication.

VII. CONCLUTION

Reliable router architecture with elastic buffer is simulated using Modelsim. Elastic buffers are used instead of FIFO buffers. In this paper we evaluate the performance of reliable router design using elastic buffer .Compared the power and area of the elastic buffer and FIFO buffer. Reliable router architecture with elastic buffer has less area and power consumption and also has better performance.

REFERENCES

[1] L. Benini and G. De Micheli, "Networks on chips: A new SoC paradigm,"Computer, 2002 vol. 35, no. 1, pp.70– 78 .
[2] A.S. Kale, Prof. M. A. Gaikwad, "Design and analysis of on chip router for network on chip", International Journal of Computer Trends and Technology- July to Aug Issue 2011.
[3.] C. Bobda, A. Ahmadinia, M. Majer, J. Teich, S. Fekete, and J. van der Veen, ―DyNoC: A dynamic infrastructure for communication in dynamically reconfigurable devices,‖ in Proc. Int. Conf. Field Program. Logic Appl., Aug. 2005, pp. 153–158..
[4.]G.-M. Chiu, ―The odd-even turn model for adaptive routing,‖ IEEE Trans. Parallel Distrib. Syst., vol. 11, no. 7, pp. 729–738, Jul. 2000.
[5] G. Michelogiannakis, J. Balfour, and W.J. Dally, "Elastic Buffer Flow Control for On-Chip Networks," HPCA ' 09: Proc. 15th Int'l Symp. High-Performance Computer Architecture, pp. 151-162, 2009.
[6] Vladimir Stojanovic and Vojin G. Oklobdzija. Comparative analysis of master-slave latches and flip-flops for high performance and low-power systems. *IEEE Journal of Solid- State Circuits*, 34(4):536–548, Apr 1999.
[7] I. Seitanidis, A. Psarras, G. Dimitrakopoulos and C. Nicopoulos," ElastiStore: An Elastic Buffer Architecture for Network-on-Chjp Routers ",in the proceedings of Design, automation and test in Europe conference and exhibition, 2014.
[8] Cedric Killian,Camel Tanougast, Fabrice Monteiro, andAbbas Dandache, "Smart Reliable Network on chip", in IEEE transactions on VLSI Systems, Vol.22, No.2, Feb. 2013.

BIOGRAPHY

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