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Analytical Large Signal Model for Graphene Based Transistor

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ABSTRACT: We propose a semi-empirical graphene field-effect transistor (G-FET) model for analysis and design of G-FET-based circuits. This model describes the current–voltage characteristic for a G-FET over a wide range of operating conditions. The gate bias dependence of the output power spectrum is studied and compared with the simulated values. Good agreement between the simulated and the experimental power spectrums up to the third harmonic is demonstrated, which confirms the model validity. Moreover, S-parameter measurements essentially coincide with the results obtained from the simulation. The model contains a small set of fitting parameters, which can be straightforwardly extracted from S-parameters and dc measurements. The developed extraction method gives a more accurate estimation of the drain and source contact resistances compared with other approaches. As a design example, we use a harmonic balance load-pull approach to extract optimum embedding impedance values for a sub harmonic G-FET mixer.

KEYWORDS: Gate leakage, insulated gate, PHEMT, InAlAs/InGaAs, Si_3N_4.

I.INTRODUCTION

A heterojunction is the interface that occurs between two layers or regions of dissimilar crystallinesemiconductors. These semiconducting materials have unequal band gaps as opposed to a homojunction. It is often advantageous to engineer the electronic energy bands in many solid state device applications including semiconductor lasers, solar cells and transistors (heterotransistors) to name a few. The combination of multiple heterojunctions together in a device is called a heterostructure although the two terms are commonly used interchangeably. The requirement that each material be a semiconductor with unequal band gaps is somewhat loose especially on small length scales where electronic properties depend on spatial properties.

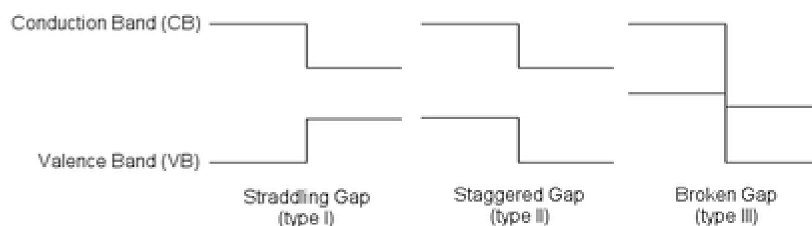

Fig.1.1: The three types of semiconductor heterojunctions organized by band alignment.

A more modern definition may be to say that a heterojunction is the interface between any two solid-state materials including crystalline and amorphous structures of metallic, insulating, fast ion conductor and semiconducting material. To allow conduction, semiconductors are doped with impurities which donate mobile electrons (or holes). However, these electrons are slowed down through collisions with the impurities (dopant) used to generate them in the first place. HEMTs avoid this through the use of high mobility electrons generated using the heterojunction of a highly-doped wide bandgap n-type donor-supply layer and a non-doped narrow-bandgap channel layer with no dopant impurities.

A. ENERGY BAND OFFSETS FOR IDEAL HETEROJUNCTIONS:

Semiconductor interfaces can be organized into three types of heterojunctions:

1. straddling gap (type I),
2. staggered gap (type II) or
3. broken gap (type III)

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There are three relevant material properties for classifying a given junction and understanding the charge dynamics at a heterojunction: band gap, electron affinity and work function. The energy difference between the valence band (VB) and conduction band (CB), called the band gap, is anywhere from 0eV for a metal (there is no gap) to over 4eV for an insulator.

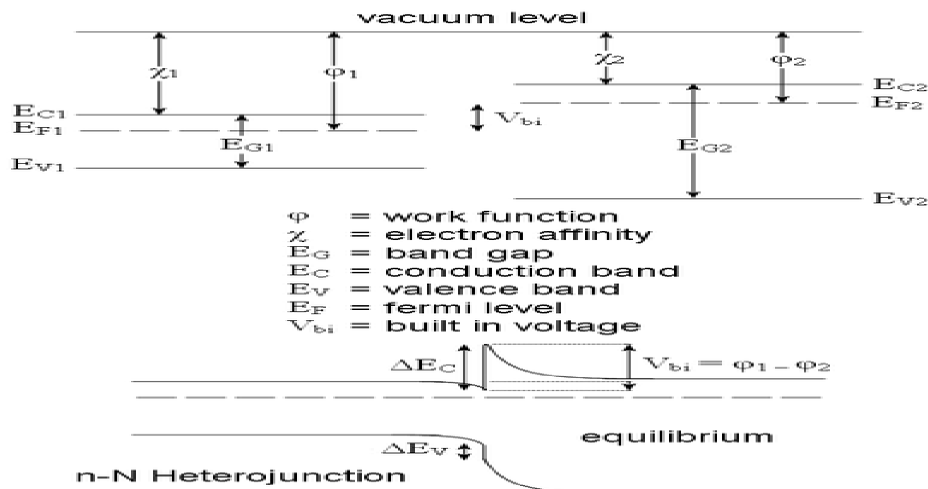

Fig1.2 heterojunction characterization

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Fig.1.2: The important variables for heterojunction characterization and analysis are defined for two semiconductors physically separated (top) and joined in chemical equilibrium (bottom).
The work function of a material is the energy difference between the Fermi energy (chemical equilibrium energy) and the vacuum level (where electron removal occurs). Finally the electron affinity of each material is needed which is the energy difference between the conduction band and the vacuum level.

Calculating energy band offsets for an ideal heterojunction is straightforward given these material properties using the Anderson's rule. The conduction band offset depends only on the electron affinity difference between the two semiconductors

$$\Delta E_C = \chi_1 - \chi_2 = \Delta\chi$$

Then using the change in band gap

$$\Delta E_{G2} = E_{G2} - E_{G1}$$

The valence band offset is simply given by

$$\Delta E_V = \Delta E_G - \Delta\chi$$

This confirms the trivial relationship between band offsets and band gap difference:

$$\Delta E_G = \Delta E_C + \Delta E_V$$

In Anderson's idealized model these material parameters are unchanged when the materials are brought together to form an interface, so it ignores the quantum size effect, defect states and other perturbations which may or may not be the result of imperfect crystal lattice matches (more on lattice considerations below). When two materials are brought together and allowed to reach chemical/thermal equilibrium the Fermi level in each material aligns and is constant throughout the system. To the extent that they are able, electrons in the materials leave some regions (depletion) and build up in others (accumulation) in order to find equilibrium. When this occurs a certain amount of band bending occurs near the interface. This total band bending can be quantified with the built in potential given by:

$$V_{bi} = \phi_1 - \phi_2 = (E_{G1} + \chi_1 - \Delta E_{F1}) - (\chi_2 + \Delta E_{F2})$$

Where $\Delta E_{F1} = E_{F1} - E_{V1}$ and $\Delta E_{F2} = E_{C2} - E_{F2}$

II.OBJECTIVES

The principle objective of this work is to improve Current to voltage characteristics over a wide range of operating conditions. We use harmonic balance load pull approach for a sub harmonic G-FET mixer.

- Calculate the total I_{ds} drain to source current.
- Calculate Rd drain resistance.
- Calculate and modeling the equation for small signal model in the GRAPHENE.
- Calculate transconductance cut off frequency
- Finally the model is to be numerically simulated using MATLAB and the results are to be validated with

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device simulation results obtained from TCAD.

ANALYTICAL LARGE SIGNAL MODEL FOR GRAPHENE BASEDTRANSISTOR

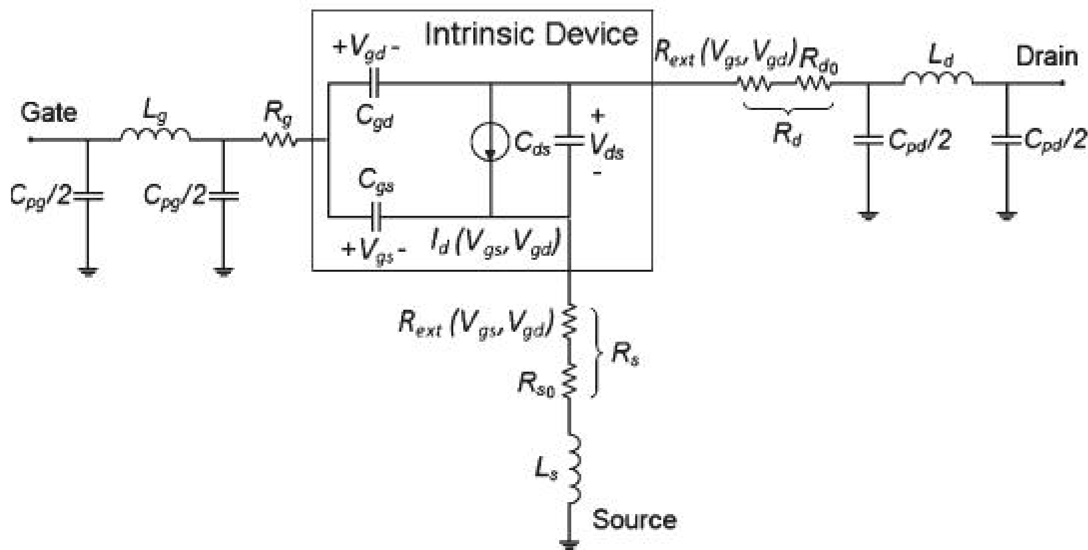


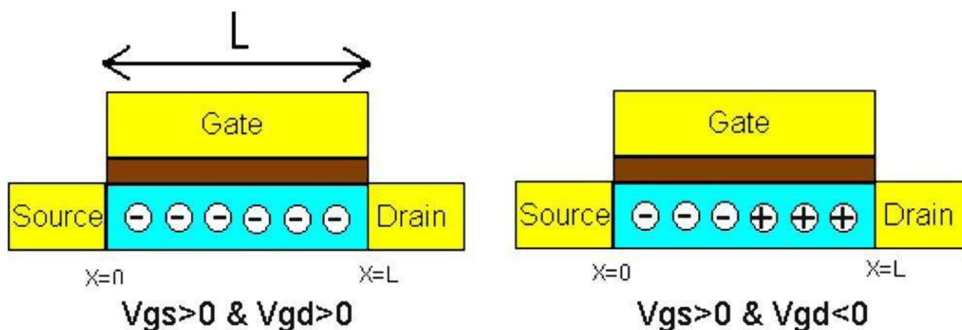
Fig. 4.1. Large-signal model of a G-FET. *C*pg, *C*pd, *Lg*, *Ld*, and *Ls* are pad parasitic capacitance values and inductances. *Rg* is the gate resistance, and *Rs* and *Rd* are the source and drain resistances including contact and access resistances.

The type of majority carriers in the G-FET channel can be determined depending on which quadrant of the *Vgs−Vgd* plane the device bias is: The carriers are electrons for (*Vgs* > 0, *Vgd* > 0), both electrons (near the source) and holes (near the drain) for (*Vgs* > 0, *Vgd* < 0), both electrons (near the drain) and holes (near the source) for (*Vgs* < 0, *Vgd* > 0), and holes for (*Vgs* < 0, *Vgd* < 0) (see Fig. 2 for the illustration). The current in the channel can be expressed as

$$Ids = q\frac{W}{L}\int_{0}^{l} n(x)Vdrift(x)dx$$

where *n*(*x*), *v*drift(*x*), *L*, and *W* are the carrier density, the carrier velocity, the channel length, and the channel width, respectively. Carrier density *n*(*x*) should be equal to the thermally generated carriers *n*th (8 × 1010 cm−2 at *T* = 300 K) for disorder-free graphene layer at zero gate voltage.

However, the measured data show that the carrier concentration at zero gate voltage is higher than *n*th .



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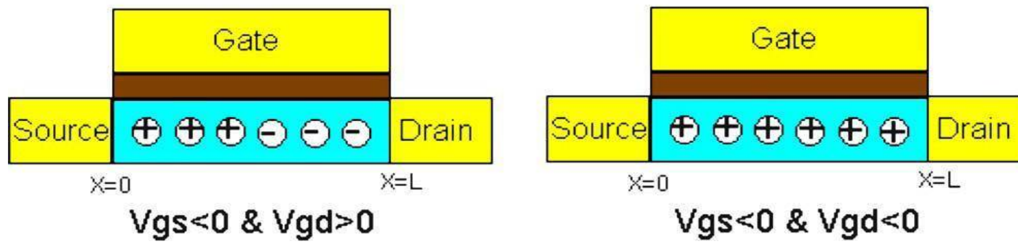

Fig. 4.2. Majority carrier type in a G-FET channel at four different *Vgs−Vgd* plane quadrants**.**

This is due to the charge impurities located at the graphene/dielectric interface or inside the dielectric, generating extra carriers (electrons or holes) in the graphene layer .This effect is modeled in by the following semi-empirical charge–voltage relation:

$$n(x) = \sqrt{(n_0^2 + (c * V(x)/q)^2)}$$

where n_0 is the residual carrier density due to disorder and thermal excitation. This is the minimum charge concentration of the graphene layer, and $C = (Cgs + Cgd)/(LW)$ is the gate capacitance per area. The total gate capacitance consists of the gate oxide capacitance *C*ox in series with the graphene quantum. capacitance *Cq*. In this model, since *Cq* ,*C*ox, the effect of
Cq is ignored. This is valid except for ultrathin gate dielectrics . We note that the above equation reduces to the familiar $n(x) = C \times V(x)/q$ at high gate voltage and to $n = n0$ at zero gate voltage. The carrier drift velocity is

$$Vdrift(x) = \frac{\mu E(x)}{\sqrt[m]{\left(1 + \left(\left(\frac{u * E(x)}{Vsat}\right)^m\right)\right)}}$$

In the first quadrant (*Vgs* > 0, *Vgd* > 0)

$$I_{ds} = q\frac{W}{L}\int_{V_{gd}}^{V_{gs}} \frac{\mu n(V)}{\sqrt[m]{1 + \left(\frac{\mu|E(V)|}{v_{\text{sat}}(V)}\right)^m}} dV.$$

$$\overline{v}_{\text{sat}} = v_F\beta / \sqrt[4]{n_0^2 + (C(V_{gs} + V_{gd})/2q)^2}$$

$$f(x, y) = x\sqrt{1 + x^2} - y\sqrt{1 + y^2} + \ln\frac{\sqrt{1 + x^2} + x}{\sqrt{1 + y^2} + y}$$

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and defining *Vgs* = *Vgs/V*0 and *Vgd* = *Vgd/V*0, where *V*0 = *Q*0/*C*, and therefore

$$I_{ds1} = \frac{\mu_e V_0 Q_0}{\sqrt[m]{1 + \left(\frac{\mu_e |V_{gs} - V_{gd}|}{L\overline{v}_{\text{sat}}}\right)^m}} \frac{W}{L} f(\bar{V}_{gs}, \bar{V}_{gd}).$$

$$I_{ds} = \frac{W}{L}\left(\int_0^{L_1} e \times n(x) v_{\text{drift},e}\, dx + \int_{L_1}^{L} e \times n(x) v_{\text{drift},h}\, dx\right)$$

After integration, we have

$$I_{ds2} = \frac{\mu_e V_0 Q_0}{\sqrt[m]{1 + \left(\frac{\mu_e |V_{gs} - V_{gd}|}{L\overline{v}_{\text{sat}}}\right)^m}} \frac{W}{L} f(\bar{V}_{gs}, 0) + \frac{\mu_h V_0 Q_0}{\sqrt[m]{1 + \left(\frac{\mu_h |V_{gs} - V_{gd}|}{L\overline{v}_{\text{sat}}}\right)^m}} \frac{W}{L} f(0, \bar{V}_{gd}).$$

In the third quadrant (*Vgs* < 0*, Vgd* > 0), using the same procedure as before

$$I_{ds3} = \frac{\mu_h V_0 Q_0}{\sqrt[m]{1 + \left(\frac{\mu_h |V_{gs} - V_{gd}|}{L\overline{v}_{\text{sat}}}\right)^m}} \frac{W}{L} f(\bar{V}_{gs}, 0) + \frac{\mu_e V_0 Q_0}{\sqrt[m]{1 + \left(\frac{\mu_e |V_{gs} - V_{gd}|}{L\overline{v}_{\text{sat}}}\right)^m}} \frac{W}{L} f(0, \bar{V}_{gd})$$

and finally, for the fourth quadrant (*Vgs* < 0*, Vgd* < 0), we have

$$I_{ds4} = \frac{\mu_h V_0 Q_0}{\sqrt[m]{1 + \left(\frac{\mu_h |V_{gs} - V_{gd}|}{L\overline{v}_{\text{sat}}}\right)^m}} \frac{W}{L} f(\bar{V}_{gs}, \bar{V}_{gd}).$$

The above equations describe *Ids* based on *Vgd* and *Vgs* in different quadrants. We combine the above equations and write *Ids* for all bias conditions as

$$I_{ds} = I_{ds1}\Theta(V_{gs})\Theta(V_{gd}) + I_{ds2}\Theta(V_{gs})\Theta(-V_{gd}) \times I_{ds3}\Theta(-V_{gs})\Theta(V_{gd}) + I_{ds4}\Theta(-V_{gs})\Theta(-V_{gd})$$

The transconductance *gm* = *d Id/d Vgs*/*Vds*=const of the intrinsic device can be approximated in the different quadrants .

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The transconductance at a I_{ds1}, I_{ds4} are differentiated and get

$$gm1{,}4 = \frac{2\mu_{e,h}}{\sqrt[m]{1 + \left(\frac{\mu_{e,h} Vds}{LVsat}\right)^m}} \frac{W}{L} C\left(\sqrt{\left(V_0^2 + V_{gs}^2\right)} - \sqrt{\left(V_0^2 + \left(V_{gs}^2 - V_{gd}^2\right)\right)}\right)$$

The transconductance at a I_{ds2}, I_{ds3} are differentiated and get

$$gm2{,}3 = \frac{2\mu_{e,h}}{\sqrt[m]{1 + \left(\frac{\mu_{e,h} Vds}{LVsat}\right)^m}} \frac{W}{L} C\left(\sqrt{\left(V_0^2 + V_{gs}^2\right)} - \frac{2\mu_{e,h}}{\sqrt[m]{1 + \left(\frac{\mu_{e,h} Vds}{LVsat}\right)^m}} \frac{W}{L} C \sqrt{\left(V_0^2 + \left(V_{gs}^2 - V_{gd}^2\right)\right)}\right)$$

The total transconductance to be the maximum of $gm1{,}4$, $gm2{,}3$.

$$g_{m,max} = \frac{2\mu_{e,h}}{\sqrt[m]{1 + \left(\frac{\mu_{e,h} Vds}{LVsat}\right)^m}} \frac{W}{L} C(Vds)$$

The drain-to-source resistance becomes

$$R_{ext}(Vgs, Vgd) = \frac{1 + \tanh(Vgs/V2)}{2} \frac{1 + \tanh(Vgd/V2)}{2} * R_{exto}$$

for Vgs , VDirac and

$$R_{DS} = 2R_0 + \frac{\alpha_{\mu_h}}{\sqrt{1 + (V_{gs}/V_0)^2}}$$

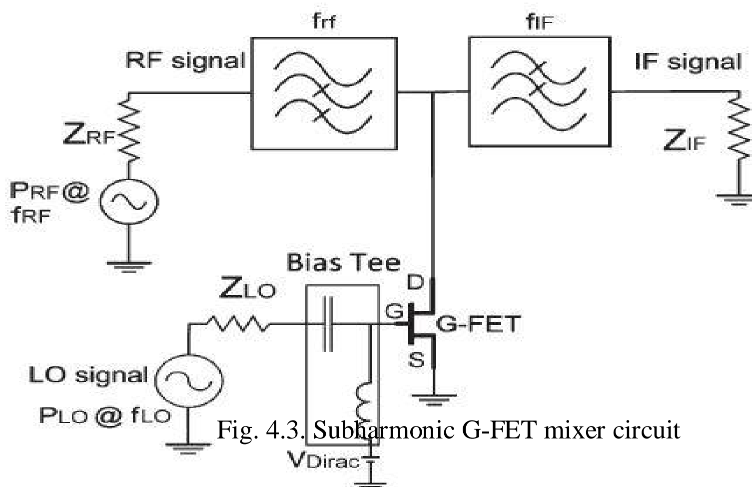

Fig. 4.3. Subharmonic G-FET mixer circuit

$$C_{gd} = -Y_{12}/j\omega, C_{gs} = (Y_{11} + Y_{12})/j\omega$$
$$C_{ds} = Im(Y_{22} + Y_{12})/\omega$$

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The rest of the parameters are calculated as follows:

$$C = (C_{gs} + C_{gd})/(LW)$$
$$Q_0 = CV_0$$
$$\mu_{e,h} = L/\left(W\alpha_{\mu_{e,h}}Q_0\right).$$

The circuit schematic of a subharmonic resistive G-FET mixer. The input-signal frequencies are 2 GHz (fRF) and 1.01 GHz (fLO), and the desired output-signal frequency (fIF = /fRF − 2 × fLO/) is 20 MHz. By running a harmonic balance loadpull simulation, the optimum RF and IF embedding impedance values for a given local oscillator (LO) power value PLO can be found.

III.RESULTS AND DISCUSSION

The transconductance characteristic curves at different V_{gs} are depicted in Figs. 6.1.

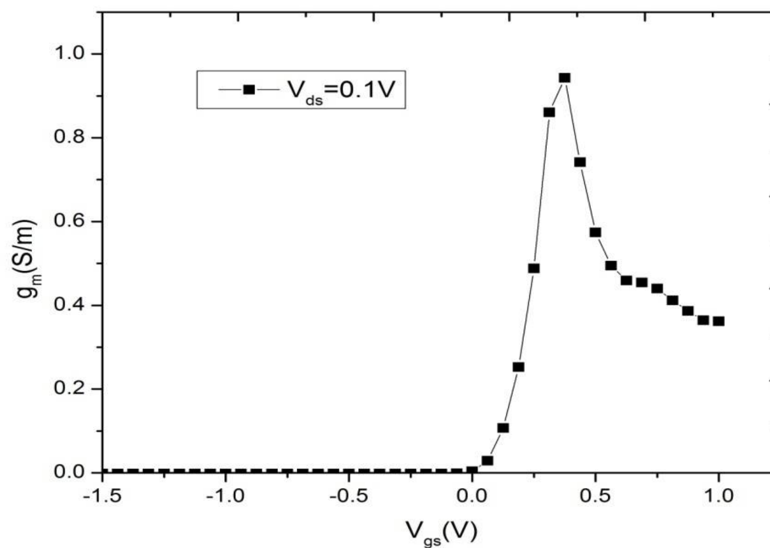

Fig 6.1 model versus measured data for the transconductance(V_{Dirac}=1v,V_{DS}=0.1v)

As can be seen, the model is in good agreement with the measurement. The simulated voltage range has been extended beyond the experiment range.

Device parameters are extracted from both dc and S-parameter measurements. The measured S-parameters are used in order to extract the extrinsic parasitic elements and the intrinsic capacitors. For parasitic elements, the S-parameters of the open and short structures are needed. In conventional FETs, the open and short structures are obtained by biasing the device under the forward-biased gate and pinched off current, respectively.

However, since the “open” and “short” structures do not include graphene in the channel, the parasitic drain and source resistances achieved by this method do not include the contact and access resistances.

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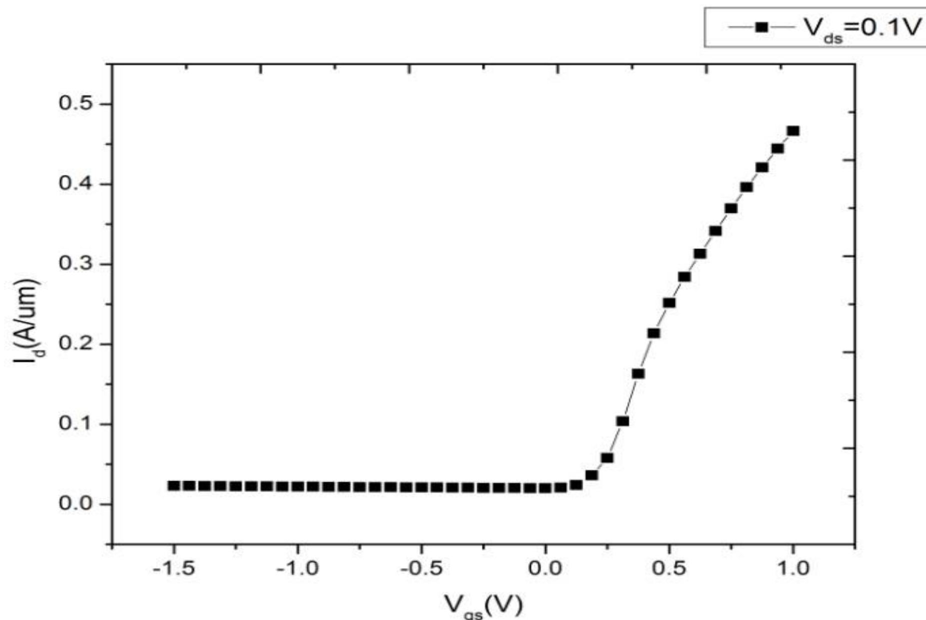

FIG 6.2 drain current versus gate to source voltage

In fig 6.2, the drain current to the gate to the source voltage is plotted in simulation.These resistances are the main contributions to the parasitic resistances, and as a result, this method underestimates the contact resistances.

These values are more than an order of magnitude lower than the lowest reported contact resistance for a single-layer graphene at room temperature.

For the *IDS–VDS* characterization, a pulsed *I–V* measurement was used to avoid the self-heating effect at high drain voltages . Since the intrinsic device of the equivalent circuit (see Fig. 6.3) has three terminals, i.e., gate, drain, and source, it is possible to express the drain current *Ids* as a function of any two voltages between these terminals.

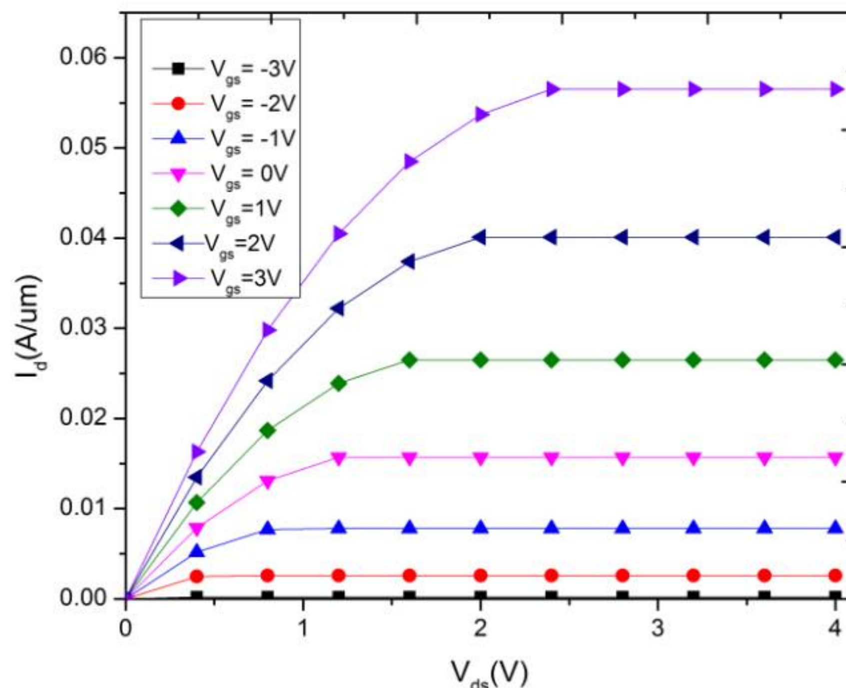

Fig.6.3 . Model versus measured data for the *IDS–VDS* characteristic curves at *VGS* −*V*Dirac = −3 to 3 V.

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We select *Vgs* and *Vgd* as independent variables because of the symmetric structure of the G-FETs and since the drain and source are interchangeable. In order to distinguish between intrinsic and extrinsic voltages, capital letters are used for the latter case, i.e., *VGS*..

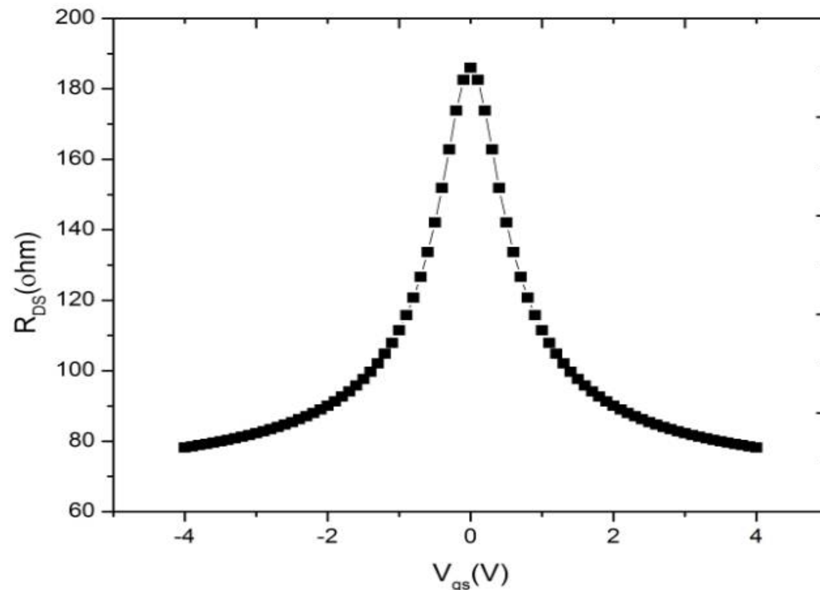

Fig 6.4 fixed data versus measured data for the drain source resistance

In fig 6.4 the drain resistance should be gradually increase and then it will be decrease. This effect mainly comes from the charge transfer between the graphene and the metal contact. The charge type can be electrons or holes depending on the work function of the deposited metal.

IV.CONCLUSION

In this Paper, we discuss about the basics of graphene, how it works, could become a potential replacement for silicon, where extract method gives a more accurate estimation of drain and source contact resistance compared with other approaches.

We have proposed and evaluated a closed-form large-signal model for the G-FETs. The model is semi-empirical and is derived for a single-layer zero-band-gap graphene. The model accepts different carrier mobility values for electrons and holes, and it can predict the asymmetric transfer characteristic of a G-FET. Using a semi-empirical approach reduces the complexity of the calculations and enables us to have an analytical model suitable for circuit-level simulations. This model has few fitting parameters, which can be straightforwardly extracted using a novel method.

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