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A Coarse Grained Recovery Boosting Technique to Enhance NBTI in SRAM Array

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ABSTRACT: Negative bias temperature instability (NBTI) is one of the most important silicon reliability problems facing processor designers. Static random access memory (SRAM) exhibit a major problem called negative bias temperature instability while storing the data "0" so large amount of energy is wasted. Hence in this paper, we attempt to recovery the negative bias temperature instability by using modified SRAM circuit. In this coarse grained recovery boosting technique, a single control signal puts the entire array into the recovery boost Mode instead of fine grained recovery boosting technique and also it is used for recovery the caches missing when occur the cache dead time. In this work, we introduce voltage feeding inverter solutions (modified SRAM circuit) to address this inefficiency. Our solutions rely on overcome cache missing by reducing gate oxide breakdown voltage that avoids SRAM dead time made to overcome cache failure.

KEYWORDS: Negative bias temperature instability (NBTI), static random access memory (SRAM).

I.INTRODUCTION

Processors have become highly susceptible to a variety of reliability problems in silicon, such as particle induced soft errors and hard errors. A key emerging hard error problem facing the microprocessor industry today is Negative Bias Temperature Instability (NBTI), which affects the lifetime of PMOS transistors. Providing protection for the processor against declining silicon reliability in order to meet service life guarantees can entail significant performance, power and area overheads.

NBTI occurs when a negative bias (i.e., a logic input of "0") is applied at the gate of a pMOS transistor. The negative bias can lead to the generation of interface traps at the Si/SiO2 interface, which cause an increase in the Vth of the device. This increase in the Vth degrades the speed of the device and reduces the noise margin of the circuit, eventually causing the circuit to fail [1], [3]. One interesting aspect of NBTI is that some of the interface traps can be eliminated by applying a logic input of "1" at the gate of the pMOS device.

Memory arrays that use static random access memory (SRAM) cells are especially susceptible to NBTI. SRAM cells consist of cross-coupled inverters that contain pMOS devices. Since each memory cell stores either a "0" or a "1" at all times, one of the pMOS devices in each cell always has a logic input of "0." Previous work on applying recovery techniques to SRAM structures aim to balance the degradation of the two pMOS devices in a memory cell by attempting to keep the inputs to each device at a logic input of "0" exactly 50% of the time [9], [1], [12] . However, one of the devices is always in the negative bias condition at any given time. In this paper, we propose a technique called coarse grained Recovery Boosting that allows both pMOS devices in the memory cell to be put into the recovery mode. The basic idea is to raise the ground voltage and the bit lines to Vdd when the cell does not contain valid data [5].

Coarse grained Recovery Boosting technique is implemented in caches to achieve less power. Cache dead time can increases cache missing significantly. SRAM cells (which are traditionally implemented using six-transistor cells) can limit SRAM stability concerns due to gate oxide breakdown. Eight-transistor (8T) cells were proposed to enhance gate oxide stability under voltage scaling. 8T cells, however, suffer from costly write operations caused by the column selection issue. Previous work has proposed Read-Modify Write (RMW) to address this issue at the expense of an increase in cache access frequency [8]. In this work, we introduce voltage feeding inverter solutions (modified SRAM circuit) to address this inefficiency. Our solutions rely on overcome cache missing by reducing gate oxide breakdown voltage that avoids SRAM dead time made to overcome cache failure.

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This paper is organized as follows: overview of NBTI is given in section 2. Basics of recovery boosting are given in section 3. Results and Discussion are given in section 4 and the conclusion is drawn in section 5.

II. OVERVIEW OF NBTI

Negative Bias Temperature Instability (NBTI) is a growing concern for CMOS technology and affects the lifetime of PMOS transistors. NBTI increases the threshold voltage of PMOS devices, which in turn degrades the speed of circuits[17]. During the fabrication process, hydrogen atoms form a Si − H bond along the Si/SiO2 interface.

Water molecules are often present during the contact and via formation of the IC fabrication process, which can increase the effects of NBTI by donating hydrogen to the silicon oxide interface. When a logic input of "0" is applied to the gate of a PMOS transistor (Vgs = -Vdd), NBTI occurs due to the generation of interface traps at the Si/SiO2 interface. When silicon is oxidized, most of the Si atoms at the surface of the wafer bond with oxygen while a few atoms bond with hydrogen.

When the transistor is being stressed, an electric field is placed across the oxide layer. When a negative bias (i.e., a logic input of "0") is applied at the gate of a PMOS transistor, the relatively weak Si − H bonds get disassociated[15] . These hydrogen atoms enter the oxide layer. The longer a hydrogen atom is in the electric field, the deeper into the oxide layer it will penetrate. Eventually the hydrogen atoms can reach the oxide/poly interface and cluster there.

By introducing positively charged ions/interface traps (hydrogen atoms) into the oxide layer, the part of the field that inverts the transistor channel is weakened. Over time, this reduces the number of hydrogen atoms that can break free. These interface traps cause the threshold voltage (Vt) of the PMOS transistor to increase, which in turn degrades the speed of the device and the noise margin of the circuit. This is known as the Stress phase for the PMOS.

The increase in Vt due to stress is given by

$$\Delta V_{ts} = \left(\frac{q t_{ox}}{e_{ox}}\right)^{\frac{3}{2}} . K_1 . \sqrt{C_{ox}(V_{gs} - V_t)} . e^{\frac{-E_a}{4kT} + \frac{2(V_{GS}-V_t)}{t_{ox}E_{01}}} . T_0^{-0.25} . t_{stress}^{0.25} \quad (1)$$

Where,

t_{stress} = The time under stress,
t_{ox} = The oxide thickness,
C_{ox} = The gate capacitance per unit area.

K_1, E_a, T_0, E_{01} and k are constants equal to 7.5 C−0.5nm−2.5, 0.49 eV, 10−8 s/nm2, 0.08V/nm and 8.6174 10−5eV/K respectively.

When a logic input of "1" is applied to the gate (Vgs = 0), the H atoms released in the stress process can anneal the broken bonds, or the H atoms may diffuse (or drift) away from the interface toward the oxide/poly interface. Therefore, this process helps in eliminating some of the traps[11]. This is known as the Recovery phase. During the recovery phase a positive electric field is placed across the oxide layer.

The field removes the inverted channel and hydrogen is free to reconnect with the available silicon by annealing[10],[13]. This process, much like stressing, can be exacerbated by increased temperature. As mentioned earlier, the hydrogen can move all the way to the Si/Poly interface making it possible that not all of the hydrogen can return to the Si/SiO2 interface. This effect creates a state of hysteresis, leaving behind a residual Vt after annealing.

The final increase of Vt after considering both the stress and recovery phase is[2]

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$$\Delta V_t = \Delta V_{ts}.(1 - \frac{2\xi_1 t_{ox} + \sqrt{\xi_2 e^{\frac{-E_a}{kT}} T_0 t_{rec}}}{((1+\delta)t_{ox} + \sqrt{e^{\frac{-E_a}{kT}}(t_{stress} + t_{rec})}}) \quad (2)$$

Where,

t_{rec} = The time under recovery,

ξ_1, ξ_2 are constants equal to 0.5, 0.9 and 0.5 respectively.

From the equations, it is observed that NBTI is exponentially dependant on the difference between Vgs and Vt, temperature and stress/recovery time.

A lower Vgs, temperature and stress time improves the lifetime whereas a higher Vt and recovery time improves it. A lower Vgs (which eventually lowers the temperature) will have an impact on performance

III. BASICS OF RECOVERY BOOSTING

Since the SRAM cell has cross-coupled inverters, each inverter charges the gate of the PMOS or NMOS device of the other inverter. Therefore, at any given time, one PMOS device will always be in the stress mode. The goal of recovery enhancement is to put the PMOS devices into the recovery mode by feeding input values to the cell that will transition them into that mode. However, due to the cross-coupled nature of the inverters, only one of the PMOS devices can be put into the recovery mode.

We propose a 6T SRAM cell design shown in Figure 1 which is capable of normal operations (read, write, and hold) as well as providing an NBTI recovery mode that we call the recovery boost mode where both PMOS devices within the cell undergo recovery at the same time.

The basic idea behind recovery boosting is to raise the node voltages (N0 and N1 in Figure 1) of a memory cell in order to put both PMOS devices into the recovery mode. This can be achieved by raising the ground voltage and bitlines to the nominal voltage through an external control signal. Raising the bitlines to Vdd allows for a fast transition into the recovery boost mode, which is important for high speed SRAM.

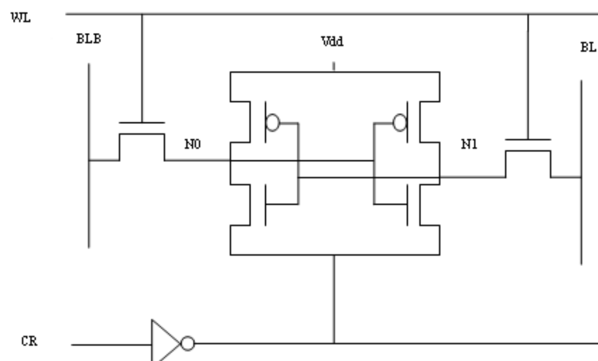

Fig. 1 Modified SRAM cell that support recovery boosting.

The modified SRAM cell has the ground connected to the output of an inverter, as shown in Figure 1. CR is the control signal to switch between the recovery boost mode and the normal operating mode. During the normal operating mode, CR has a value of ‘1’ (Vdd), which in turn connects the ground of the SRAM cell to a value of ‘0’. With this connection, the SRAM cell can perform normal read, write, and hold operations. To apply recovery boosting.

CR has to be changed to a ‘0’ in order to raise the ground voltage of the SRAM cell to Vdd. To raise the voltages of both Node0 and Node1 to Vdd, BL and BLB have to be charged to Vdd along with the raised ground voltage. This circuit configuration puts both PMOS devices in the SRAM cell into the recovery mode. A cell can be put

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into the recovery boost mode regardless of whether its word line (WL) is high or low. Unlike read and write operations on a cell, putting a cell into the recovery boost mode does not require an access to its word line.

Incorporating the modified SRAM cell into a memory array requires additional micro architectural design considerations. Recovery boosting can be provided at a fine granularity, such as for individual entries/rows of a memory array, or at a coarser granularity, such as for an entire array.

Coarse-Grained Recovery Boosting: A single control signal puts the entire array into the recovery boost mode. The control signal CR with a value of '0' raises the ground connection of each entry to Vdd.[4],[16].In this design (Figure 2), connections to the Vdd rail via the PMOS devices are not required. Instead we merely need to raise all the bitlines in the array to Vdd to transition all the cells in the array to the recovery boost mode[7].

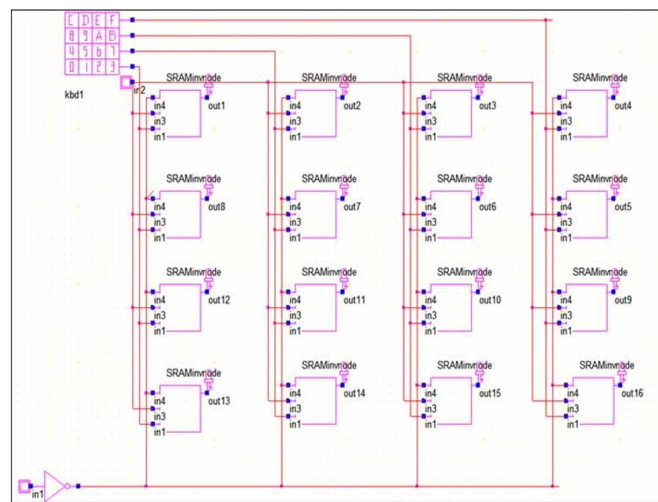

Fig. 2 Modified SRAM array for coarse grained recovery boosting.

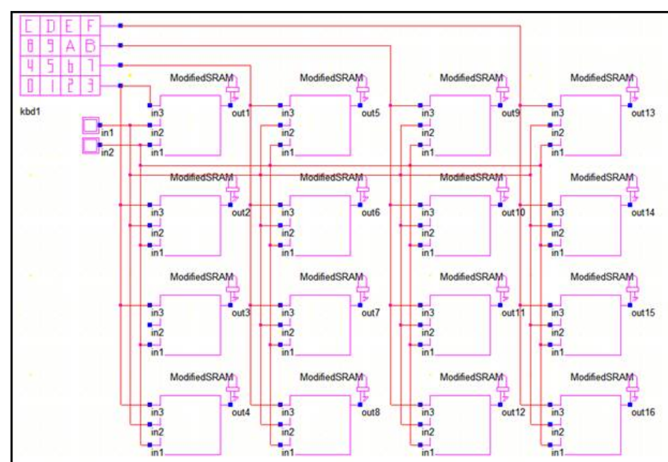

Fig. 3 Conventional SRAM array for coarse grained recovery boosting.

Caches: caches comprise much of the area in current and future microprocessors; it makes sense to target them when developing leakage-reducing strategies. Recent work by Powell et al. has shown that transistor structures can be devised which limit static leakage power by banking the cache and providing "sleep" transistors which dramatically reduce leakage current by gating off the Vdd current [6], [18].

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Our work exploits these sleep transistors at a finer granularity: individual cache lines. In particular, a basic premise of our work is that, surprisingly often, cache lines are storing items that will not be used again. Therefore, any static power dissipated on behalf of these cache items is wasted. We aim to reduce the power wasted on dead items in the cache, without significantly worsening either program performance or dynamic power dissipation. One can break this reference stream into generations. Each generation is comprised of a series of references to the cache line.

Using the terminology from [14], the i-th generation begins immediately after the i-th miss to that cache line, when a new memory line is brought into the cache frame. This generation ends when this line is replaced and a new one is brought into the cache frame.

Generations begin with zero or more cache hits. Following the last reference before eviction, the generation is said to have entered its dead time. At this point, this generation has no further successful uses of the items in the cache line, so the line is said to be dead. There is considerable prior evidence that dead cache lines comprise a significant part of the cache.

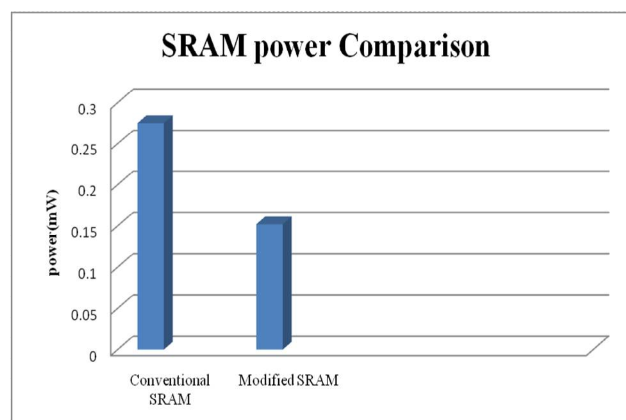
Our goal is to exploit dead periods, particularly long ones, and to be able to turn off the cache lines during them. This approach reduces leakage power dissipated by the cache storing data items that are no longer useful. The use of coarse-grained recovery boosting, which imposes less area overheads, for designing caches. Caches pose additional challenges, such as identifying when lines become valid to put them into the recovery boost mode. We plan to explore the use of techniques such as dead-block prediction [8] in conjunction with recovery boosting to mitigate the impact of NBTI on caches. The results are shown in figure 4.

IV.RESULTS AND DISCUSSION

The conventional SRAM array will leads to power dissipation by applying a negative bias (i.e., a logic input of “0”) at the gate of a pMOS transistor. This causes negative bias temperature instability. The Modified SRAM array will reduce power dissipation by providing a control line.

The proposed system enhances efficiency by error free transmission when used in nano-meter technology. The Table I shows that modified SRAM array power will be less when compared with conventional SRAM circuit. While using a modified coarse grained recovery boosting in caches, it is automatically recover the cache missing when reach the dead time.

Table I



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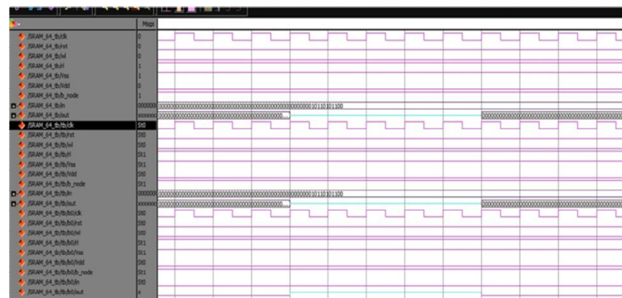

Fig 4. Caches (Dead Block Predication)

V. CONCULSION

Negative bias temperature instability (NBTI) is an important lifetime reliability problem in microprocessors. SRAM memory cells are especially vulnerable to NBTI since the input to one of the pMOS devices in the cell is always at a logic "0." In this paper by using coarse grained recovery boosting technique, a single control signal puts the entire array into the recovery boost Mode so that Modified SARM array(coarse grained) has less power when compare to the conventional SRAM array. It overcomes the cache missing when the cache dead time occurs.

REFERENCES

[1] S. V. Kumar, C. H. Kim, and S. S. Sapatnekar, "Impact of NBTI on SRAM read stability and design for reliability," in Proc. Int. Symp.Quality Electron. Design, 2006, pp. 210–218.
[2] W. Wang, V. Reddy, A.T. Krishnan, R. Vattikonda, S. Krishnan, and Y. Cao. Compact modeling and simulation of circuit reliability for 65-nm cmos technology. In IEEE Transactions on Device and Materials and Reliability, 2007.
[3] S.Park, K. Kang, and K. Roy, "Reliability implications of bias-temperature instability in digital ICs," IEEE Design Test of Comput., pp.8–17, Dec. 2009.
[4] S. Feng, S. Gupta, and S. Mahlke, "Olay: Combat the signs of aging with introspective reliability management," in Proc.Workshop Quality-Aware Design (W-QUAD), 2008.
[5] Taniya Siddiqua and Sudhanva Gurumurthi, "Enhancing NBTI Recovery in SRAM Arrays Through Recovery Boosting" University of Virginia, Department of Computer Science, Senior Member, IEEE Transactions on very large scale integration (VLSI) systems, 2011.
[6] M. D. Powell et al. Gated-Vdd: A Circuit Technique to Reduce Leakage in Deep-Submicron Cache Memories. In ISLPED, 2000.
[7] A. Tiwari and J. Torrellas, "Facelift: Hiding and slowing down aging in multicores," in Proc. Int. Symp. Microarchitecture (MICRO), Nov. 2008, pp. 129–140.
[8] S. Kaxiras, Z. Hu, and M. Martonosi, "Cache decay: Exploiting generational behavior to reduce cache leakage power," in Proc. Int. Symp. Comput. Architecture (ISCA), Jun. 2001, pp. 240–251.
[9] J. Abella, X. Vera, and A. Gonzalez, "Penelope: The NBTI-aware processor," in Proc. 40th IEEE/ACM Int.Symp. Microarchitecture, 2007.
[10] R. Vattikonda et al. Modeling and minimization of pmos nbti effect for robust nanometer design. In DAC, 2006.
[11] V. Huard and M. Denais. Hole trapping effect on methodology for dc and acnegative bias temperature instability measurements in pmos transistors. In Reliability Physics Symposium Proceedings, 2004.
[12] J. Shin, V. Zyuban, P. Bose, and T. M. Pinkston, "A proactive wearout recovery approach for exploiting microarchitectural redundancy to extend cache SRAM lifetime," in Proc. Int. Symp. Comput. Architecture, 2008, pp. 353–362.
[13] C. Shen et al. Characterization and physical origin of fast vth transient in nbti of pmosfets with sion dielectric. In IEDM, 2006.
[14] D. A. Wood, M. D. Hill, and R. E. Kessler. A Model for Estimating Trace-Sample Miss Ratios. In ACM SIGMETRICS, pages 79–89, June 1991.
[15] M. Denais et al. New perspectives on nbti in advanced technologies: modeling characterization. In Solid-State Device Research Conference, 2005.
[16] J. Srinivasan, S. V. Adve, P. Bose, and J. A. Rivers, "The case for lifetime reliability-aware microprocessors," in Proc. Int. Symp. Comput. Architecture (ISCA), Jun. 2004, pp. 276–287.
[17] G. Chen et al. Dynamic nbti of pmos transistors and its impact on device lifetime. In Reliability Physics Symposium Proceedings, 2003.
[18] S.-H. Yang et al. An Integrated Circuit/Architecture Approach to Reducing Leakage in Deep-Submicron High-Performance I-Caches. In Proc. HPCA-7, 2001.