ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijircce.com

Vol. 5, Issue 3, March 2017

Viterbi Algorithm Optimization for Storage Transient Error

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ABSTRACT: Data communication basically involves the transfer of data from one point to another. Error may be occurred by the channel which makes the data unreliable for user and hence we have different error detection and correction schemes. This paper proposes the viterbi algorithm for error detection and correction by using trellis method. In the data transmission, the error detection and correction with minimum latency and buffering is a major problem. This paper uses virtual channel to increase the throughput and efficiency of the system. It is the router which is used to move message and reply on different channels and never have loop on a single channel. Deadlock can be avoided during transmission. The viterbi algorithm uses feed forward control which means the error can be identified before processing the data. In this paper, the viterbi algorithm having the capability of correcting up to 8 bits and it doesn't need any separate buffer for storing the error bits.

Then we implement the design using Verilog, then simulated and synthesized using Modelsim SE 6.5 simulator and Xilinx ISE 13.2i respectively.

KEYWORDS: Viterbi algorithm, Virtual channel, Feed forward control, Efficiency, Error.

I. INTRODUCTION

In today's life, communication is very important for everyone. The world is feared to think beyond any communication gadgets. Data communication basically involves transfers of data from one location to another location. Error may be occurred in the channel which makes data unreliable for user. Hence we need different error detection and error correction schemes. Our main goal is to achieve High speed and less complexity. The proposed work is to detect and correct a multiple error using low complexity novel cross parity code at lower overhead. In that existing system error correction and error detection was done by Hamming code but existing system is fully depends upon feed backward control. In this proposed system, feed forward control algorithm is applied, here error detection and correction technique is Viterbi algorithm, and using this method we can save area, power and delay. These adaptive solutions are providing more stable network performance and optimizing the network path and resources. By doing so one can easily achieve a trade of between area and defect tolerance by simply avoiding the complex decoding implementations of the error correction codes. Even though the design is not perfectly handling with all error patterns, it is very rarely that some pattern that can obtain outside the scope of the proposed design. It is because of the fact that the prospects of the radiation particle intervention that can cause multiple bit flip. Hence the proposed design can contribute great error masking ability with area overhead as less as 99%. A code with minimum Hamming distance
(d), can detect up to d − 1 errors in a code word. Using minimum-distance-based error-correcting codes for error detection can be suitable if a strict limit on the least number of errors to be detected is desired. This strict upper limit is expressed in terms of the channel capacity. More theorems says that there exist codes such that with higher encoding length the probability

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of error on a discrete memoryless channel can be made arbitrarily small, provided that the code rate is lesser than the channel capacity. The code rate is defined as the fraction k/n of k source symbols and n encoded symbols. The actual maximum code rate allowed depends on the error-correcting code used, and may be lower.

II. LITERATURE SURVEY

[A.Inna Mary, Dr.Vanajashivakumar; 2016] Error detection and correction for improving FPGA was simulated by hamming code. In this paper, by using hamming code only 3 adjacent bits was detected and only 1 bit was corrected. Uses trace buffer for storing bits. If number of bits increased, performance reduced and system becomes complex.

[Jens Spinner, Jurgen Freuden berger, Sergo Shavgulidze; 2016]

In this paper, BCH code was used for the error correction and detection. BCH was used only for minimum error detection (2^m). In practical, this model does not produce accurate result and BCH code might not be acceptable for all application of flash memories.

[Vishal Chandale, Pallavi Gavali, Payal Giri, Mrs.Anjali Shrivastav; 2016]

Reed Solomon (RS) code was able to detect 4 bits and it correct only 2 burst of errors. RS codes are used to provide error protection against the burst error. It detect only upto 4 bits but correct 2 burst of error. In this RS code, the bits were grouped into a block afterwards it can correct the error. Due to this, delay occurs.

[Nikolay Kavaldjiev, Gerard J. M. Smit, Pierre G. Jansen; 2009]

The router has simple dynamic arbitration which is deterministic and fair.

III. VITERBI ALGORITHM

An efficient solution to the decoding problem is a dynamic programming algorithm known as the Viterbi algorithm, also known as the Viterbi decoder (VD). This is a maximum likelihood decoder in the sense that it finds the closest coded sequence ṽ to the received sequence ŕ by processing the sequences on an information bit-by-bit (branches of the trellis) basis.

Maximum-likelihood decoding

The likelihood of a received sequence Ŕ after transmission over a noisy memory less channel for the sent coded sequence V̂.

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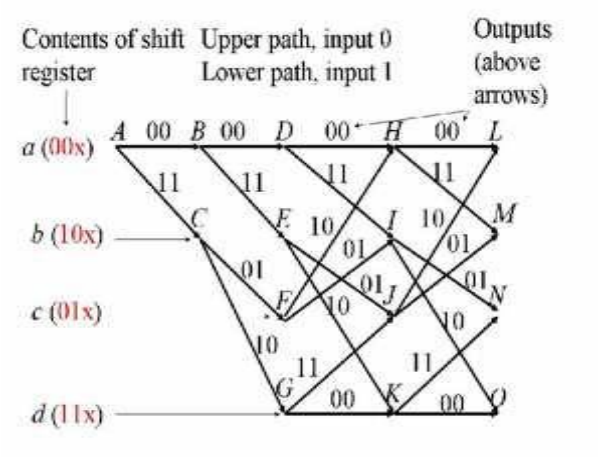

Figure 1 Trellis Diagram

SYSTEM ANALYSIS FEED FORWARD

In a feed forward system, the output is not taken into account. The system response in a predefined way without considering the effects of output. In a feed forward, the input parameters are also given to some other part of the system. The variable adjustment is not error based here. The feed forward control increases the accuracy. Energy consumption by this system is lower than other controls.

BLOCK DIAGRAM

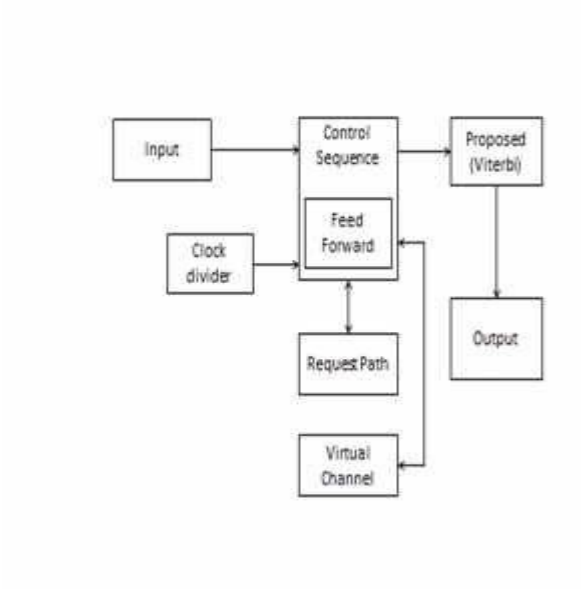

Figure 2 Block Diagram of Proposed Viterbi Algorithm

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VIRTUAL CHANNEL

Virtual channel is a router which is used to allocate the location. It is mainly used to free the space and avoid the traffic during the bit transmission.

The worm whole routing is good for Noc (Network-on-chip) because it provide low latency and less buffering requirement but it creates the deadlock. By using virtual channel, deadlock can be avoided.

The packets are allowed to hold some resources while requesting other, so that the dependency chain forms a cycle. Then there packets must wait forever. In virtual channel the separate path is allocated for each packet. The packet switches from low to high channel. The message move and replay on different channel that will never have loop on a single channel.

VITERBI ALGORITHM

Viterbi Encoder

In this paper convolution encoder is used. It accepts the input and generated encoded output. The first bit is send to the flip-flop 1 and next bit to the flip-flop 2. The bits are encoded Ex-OR operation. The encoded output bit is more than the input bit.

It is typically described by 4 parameters

1. n-no of bits produced at encoder output
2. k-no of input to encoder
3. m- Memory of encoder
4. K- Constraint length

Viterbi Decoder

Viterbi algorithm is an error correction codes also called as viterbi decoder.

Viterbi decoder is divided into 4 units:

1. Branch Metric Generation (BMU)
2. Add-Compare-Select (ACS)
3. Memory
4. Trace back Unit (TBU)

BMU

The BMU Unit execute the hamming distance calculation between the received code word and the ideally generated code sequence by encoder module inside the BMU unit.

ACS

The generated hamming distances are sending to the ACS unit. The ACS unit executes the adding comparing and then security the minimum path metrics and there respected state values among various metrics associated with each state of the decoder trellis diagram. These path metrics are calculated from the addition of the old path metric the hamming distance of the current branch of the virtual trellis diagram.

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Memory

The Memory unit which incorporated it with the ACS unit, it receives the values of the survivor metric respected to each state at each time

interval, lowest metric of the 4 survivor metric and the lowest state of the 4 stores them.

TBU

Finally the trace back receives the selected state that respected to the lower metric and start from this respected to the lower metric and start from this state following the survivor paths backwards, the tracing was done after a fixed time equal to depth of the decoder, which is=16.The tracing back process start from the lowest state from newer saved metrics and continues until the last state saved then the decoder generates the output of the last state.

After the generation of the new output the decoder shifts the new metrics and states in the decoding window.

IV. RESULT AND DISCUSSION

The design of viterbi algorithm has been made by using Verilog Hardware Description Language (Verilog HDL). The input which is given as 1010110011110000 and encoded sequence can be given in the fig. 3

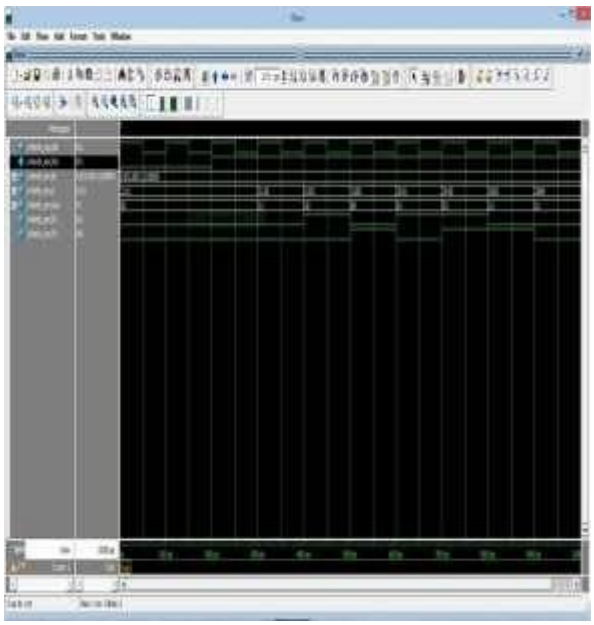

Figure 3 Simulation Output of Input Sequence

The encoded input is wire to the virtual channel. In Virtual Channel, we assign only the present state and next state value which can process and transmit the data in the desire direction/path is shown in fig. 4

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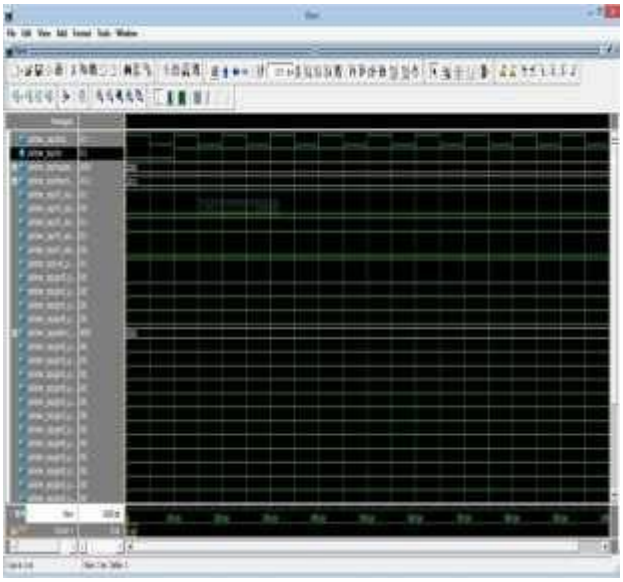

Figure 4 Simulation Output of Virtual Channel

The simulation results have been evaluated by using ModelSim 6.5. The simulation output for detecting adjacent bit error using viterbi algorithm is shown in fig. 5

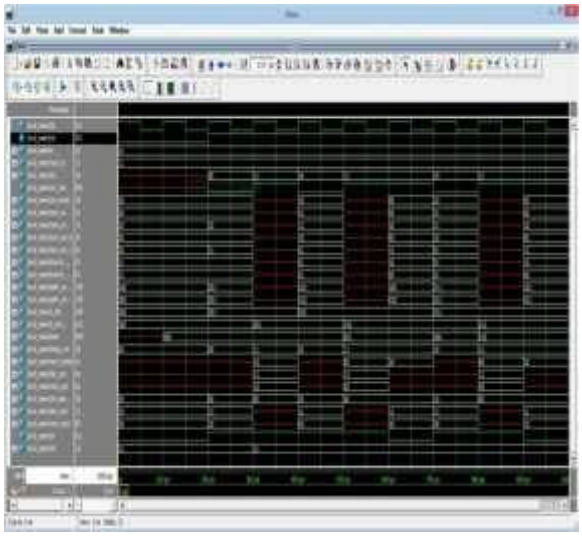

Figure 5 Simulation Output of Viterbi Algorithm

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V. CONCLUSION

In this paper, the viterbi algorithm was used for error correction and detection. By using this algorithm we can able to detect up to 16 bits and correct up to 8 bits and also deadlock can be reduced. The delay time and area is a major factor which can be minimized by using feed forward control.

Virtual channel which is used to identify the direction of data so it reduces the traffic occurred during data transmission. So the efficiency of the system will be increased.

In future, the delay time and area may be reducing by using some other algorithm.

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