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Real Time Issues for Designing of Low Power Compilers or Processors

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ABSTRACT: As the electronics usage are increasing day today which are battery usage. So these electronic gadgets demands a low power consumption, and the circuits are designed with those specifications. While designed such circuit designer will face a difficulty in size, complexity of the chips to overcome the heat dissipation which will limit the cost or functionality of the computing systems. So to solve these drawbacks various methodology and software tools have been proposed to design the low power consumption circuits. So in this paper we are describing about some trustful techniques for the low power consumption design. For this we doing some survey analysis on the existing methods. In each methodology we are discussing about the pure advantages and drawbacks in the analysis. So in this we are focusing whole on the digital circuits where we will restrict the usage of CMOS circuitry which is mostly used technology in the VLSI design.

KEYWORDS: Low power, compilers, optimization, ULP CMOS.

I. INTRODUCTION

Power consumption or life time of the circuit has become one of the major issues in designing of the circuit. As the present day electronic gadgets are portable have designed with complex circuitry integrated systems are powered with lightweight which will give life time of some hours in charging and discharging way, it is shown in below fig: 1. So both battery lifetime and system cost are heavily impacted by power consumption.

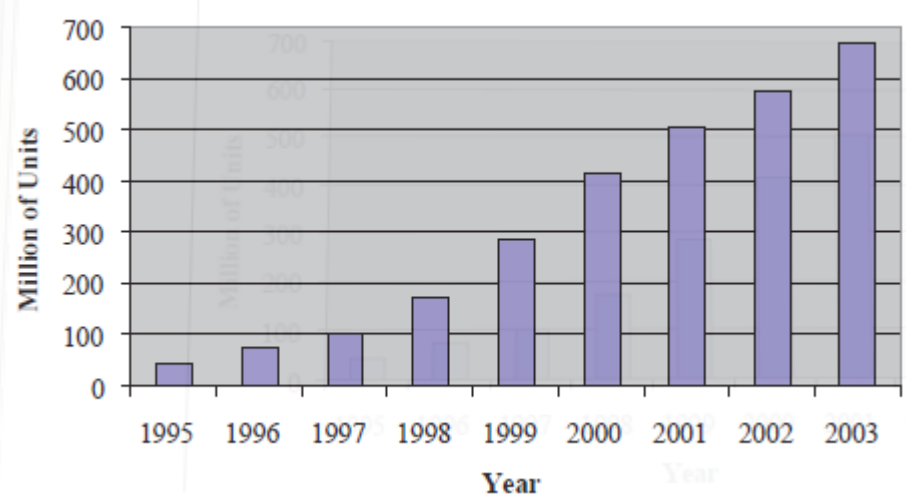

Fig:1 usage of cell phone in the global markets

Our main theme of this paper is provide some techniques used for the design of the low power consumption devices. In the literature survey we briefing about the concepts like nature of the chips and the silicon based manufacturing how they are minimizing the power. The power minimization targets on maximum of average power to be used for the devices. Then the devices which operates on battery operated exhibits the heat dissipation which constraints power supply and power grid systems. In designing the low power consuming devices power minimization

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is not only important but also the performance will also be considered as an important metric while designing. So many approaches have been proposed in the past time. In these designs PDP is an very important metric to analyze the power consumption. Whenever the high priority is given to the performance than the power consuming, the EDP can be adopted tightly control of performance degradation or reduction [1]. To solve this type of degradation we can use the constrained optimization approach. On the other hand flexibility Vs power is also one of the main power constraints which have to achieve the maximum power efficiency without compromising of flexibility/programming. So to maintain some uniformity we choose designs which will have more market end. So these are briefing with some examples below

1. The Transmeta`s Crusoe processor family is a x86 processor which have high end portable appliances. It is used as a general purpose processor and have a good features of low power consumption[2]
2. ARM microprocessors [3] are group of families which will represent the Low power integrated core and peripherals for PDA, PC etc.,
3. Texas instruments microprocessors [4] are typical processors with very low power consumption which are used for the programming of DSP for baseband processing in wireless communications
4. Tosibha processors [5] are application specific which can be programmed in ISP and system on chip for multimedia support

So from this we are analyzing that the processors will be selected based on the application or product specific which can exhibit the low power dissipation in the devices.

1. Optimization Principles for LPD:

As in the design of IC we use CMOS technology for manufacturing of digital IC. In the power dissipation three major constraints are included. They are a. Switching power, b. Short circuit power, and c. Leakage power. Then the total power consumption/ dissipation is shown in the below equation 1

$$P = P_{Switching} + P_{Short\text{-}Circuit} + P_{Leakage} \quad \text{---------[1]}$$

Designing of low power IC implies to rise the ability of to reduce the three components for the better power consumption in the development of the electronic products. So optimization of power can be done by facing various problems in design and technology. So the speed optimization initially applied and then the supplied voltage scaling will be applied by the designer which will brings the original timing of the device.Optimization approaches which will have a lower impact on performance of the devices which can allow significant power saving, are those targets on minimization of switched capacitance through the area optimization and switching activity reduction via exploitation of various types of signals correlations. Initially optimization techniques are of two types static and dynamic optimizations to achieve different types of design abstraction.

In technology and circuit level optimizations are used in the VLSI technology and developing amazingly since from past thirty years. In this the basic scaling theory which is called as constant field scaling [6] which synergistic scaling of geometric and silicon doping features to maintain the constant filed across the oxide layer of the MOS transistor. So in this to maintain the constant field scaling regime the silicon technology evolution is probably is the most effective way to address power issues in Digital IC design which is shown in the fig 2.

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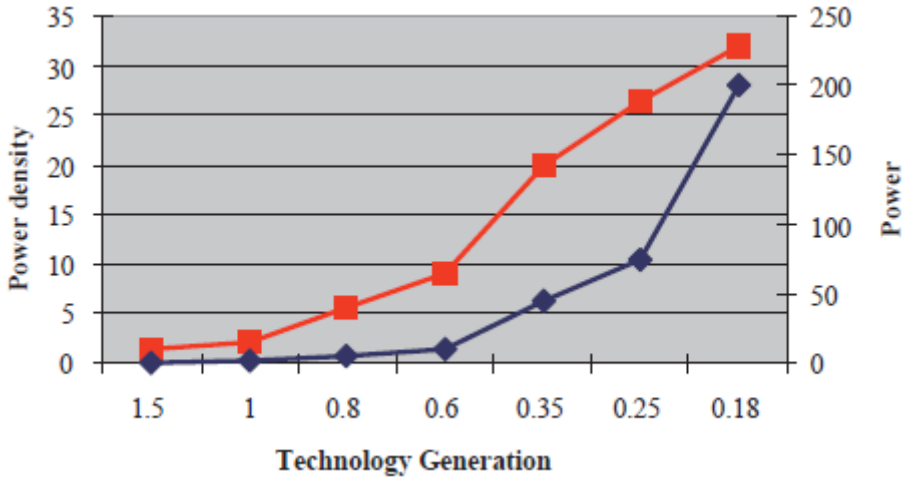

Fig:3. Power Vs power density Vs technology generation.

II. DESIGN OF LPC PRACTICAL CIRCUITS

Most widely the power reduction technique is used for the digital IC [7] which is well known as "power driven voltage scaling". It is important to see how the speed of the transistor does not depend on the supplied voltage and also on the gate over drive which acts a threshold voltage [8]. So by optimizing the V_{DD} and V_T for minimum energy lay product leads to surprisingly get low values. This approach is known as Ultra low power CMOS [9]. This is most probably not used widely in real time because of two reasons one is in real time implementation threshold control is not accurate and the second one is sub threshold current is depends on temperature exponentially which is not cost effective.

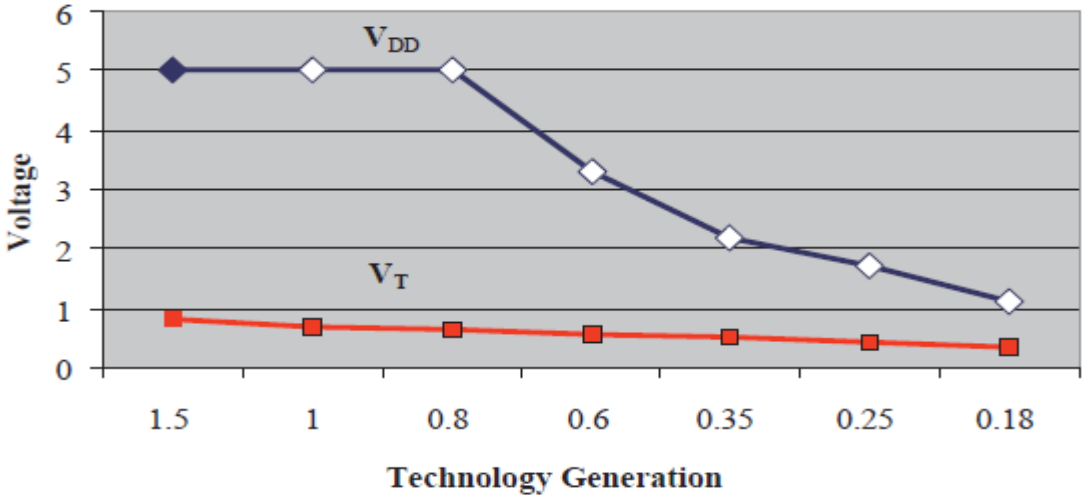

Fig:3. Supply voltage Vs threshold voltage

The supply voltage has been decreased w.r.t to the device size but shows the high performance for transistors [10]. So for the point of view of the power reduction technology driven circuits for voltage scaling. These have two important consequences, they are leakage power and the quiescent power. So to meet the leakage power constraints multiple threshold and different threshold values will be proposed, among those LTT are very fast and leaky in nature. HTT are slower when we compare with LTT. So the multiple threshold scheming has timing critical transistors which can be powered with high voltage. The drawbacks of these are design of multiple power distribution grids and power efficient level shifters to combine the low level and high level voltage circuits.

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III. OPTIMIZATION IN TERMS OF LOGIC AND ARCHITECTURAL VIEW

As the IC technology is gradually increasing a lot complexity in compiler design also increases with respect to the logical level optimization [11] which is extremely expensive and cost effective for structural logic also [12]. For this several optimization techniques have been proposed and real time implemented which enables the logic level power optimization even for the unstructured logic and low volume [13] VLSI IC digital circuits. If the critical path length remains constant then a common setting is used for constrained power optimization, in which a logic network can be turned to minimize the power dissipation. Other types of logic level power minimization techniques are used for digital IC design are refactoring, remapping, phase assignment and pin swapping. Such types of approaches are called as local transformers. So achieve such power saving the sixe also be considerable.

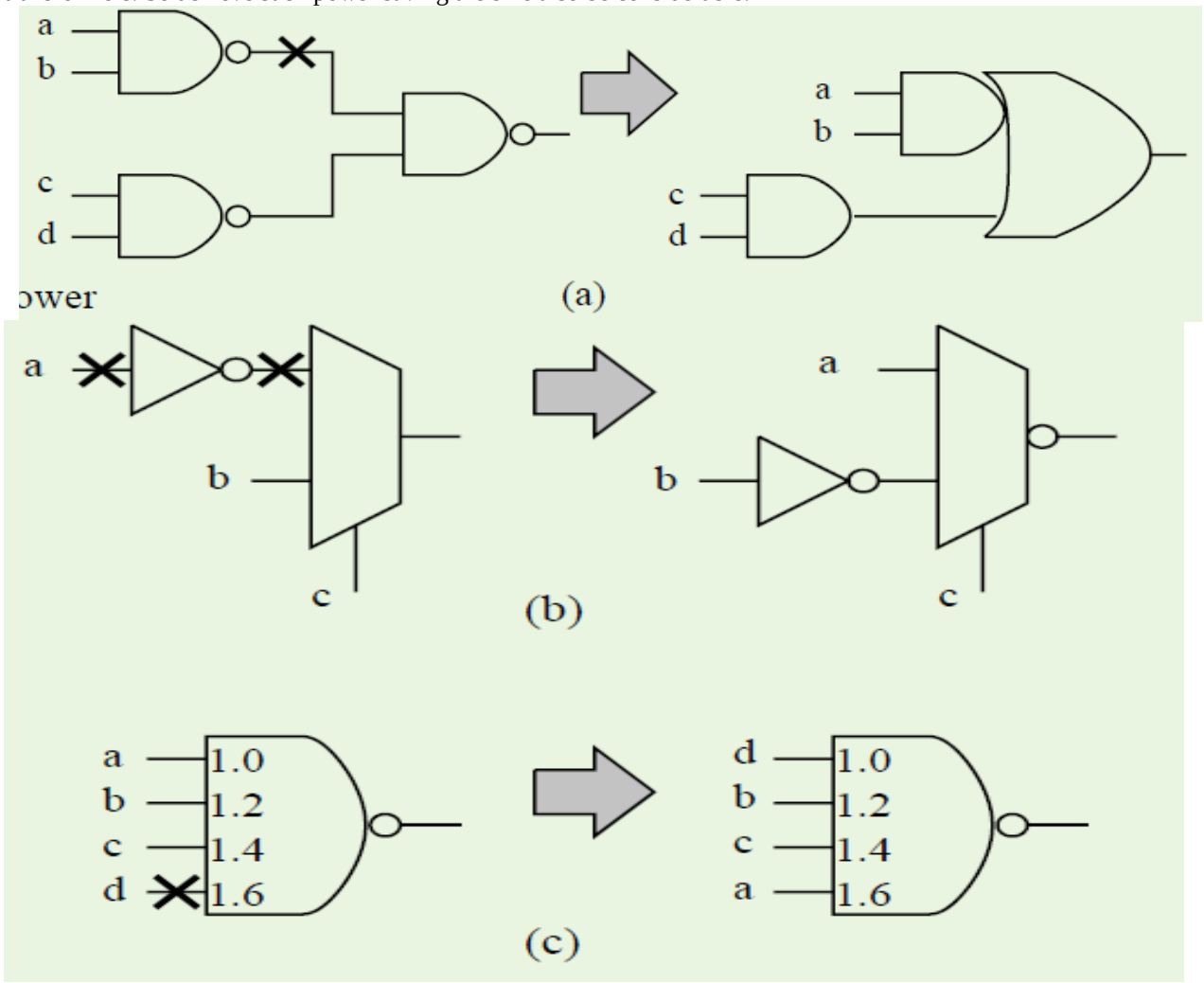

Fig:4: Local transformation for IC

IV. OPTIMIZATIONS IN TERMS OF SOFTWARE AND SYSTEM LEVEL

Generally all the electronic devices consists of hardware platforms which includes software in each layer. So most of the electronic systems/devices depend on the combination of the hardware and software. But the software does not consume any part of energy while the coding can be done using the software where the code is stored at memory which will use the energy to execute it w.r.t the software. Mainly the energy used for the executing the program and the power will be used for the hardware execution. The energy usage of the machine code is affected by the back end compilation

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of the software which can controls the operations of the task. So each software instruction can be characterized by energy required per cycle to execute each instruction. The main goal of the compiler is to speed up the execution time and reduce the code size.

Energy efficient compilations strives to achieve machine code which require less energy for the execution of the program. So this EE compilation software can be achieved by the enforcement of specific writing styles or by allowing the reduction of the source code transformation to reduce the power consumption. EE software will works as one operating systems which can be achieved by designed an energy aware task scheduler. Mainly OS achieve huge energy savings by implementing DPM of the system resources. The DPM dynamically configures the electronic systems/devices with the minimum number of components the requested services will be performed [13]. DPM can be implemented in various forms, it won`t limit the clock gating, supply voltage shutdown etc., in the electronic devices

Various System level designs will be explored to reduce the power dissipation/ energy consumption. There are many design choices for various combinations in the domain of the hardware and software design of the low power compilers. Let us consider the ACPI standard initiated by various companies like Intel, Microsoft, Toshiba etc., will provide the hardware and the software design separately which will be easy to implement the DPM policies for PC etc.,

V. CONCLUSION

In this paper we are briefing about aims & goals in electronic design strikes a balance between performances of the device w.r.t. the power efficiency. So designing of low power devices will have some design issues to satisfy the system specifications and provides a good degrees of freedom that designer should have to reach the level of good power reduction. In this paper we showed various types of design option for the low power devices development and advantages and disadvantages of each approach. Even though we explained about some samples of design techniques. Based on the drawbacks of the present approaches some new approach can be implemented to overcome those for future better development of digital IC which will have a good low power dissipation.

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