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Design of a Novel Counter Based NCO

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ABSTRACT: Numerically Controlled Oscillator (NCO) generates synchronously sequentially digitized samples .There are many types of NCO which are CORDIC Based, LUT Based, Counter Based etc. Here a new counter based NCO is designed to give more output of each varying range, without altering the design. This has vast application in many fields where different module works on separate frequency ranges. The most advantage of proposed NCO is that, through put is high, output can be easily configured to enable and disable where as the conventional counter NCO produces single output, and to alter it the values have to be recomputed. A Manchester decoding application is done by applying proposed NCO as clock to the design.

KEYWORDS: LUT, CORDIC, DDS, CLC Blocks, FSW, FCW, Fosc , Fclk, Verilog HDL.

I. INTRODUCTION

Numerically Controlled Oscillator (NCO) is invented by J.Tierney in 1971.The name "numerically controlled" means that the tempo at which sine wave samples emerge at the output of the NCO and the number of sine samples per period can be set by a microcomputer or a microcontroller. It synchronously and sequentially generates digital samples of the sine wave. NCO is the foremost edifice slab of the frequency- or waveform synthesizers. Frequency synthesizers co-operate an important function in contemporary communication and instrumentation gear where they are worn to generate a sinusoidal or digital signal with required occurrence. Waveform synthesizers are worn to produce sinusoidal voltages with incredibly precise efficient worth, which stature can be defined by the user [1].

Since NCO is a computerized motion generator, which integrates a discrete time, discrete-esteemed show of a sinusoidal waveform that can disregard the impact of requirement discreteness in simple frameworks. It is a vital part of balancing and demodulating component in advanced correspondence frameworks. Besides NCO is the centre course of each advanced frequency synthesizer and motion generator. As the strategy for understanding a NCO by the sine lookup table, expense a gathering of rationale assets, with the mounting of advanced correspondence innovation, the demand for less expensive NCO turns out to be more dire.

II. RELATED WORK

In [5], the author talks about the important clock of NCO like adder and phase register. This paper presents, as a substitute of LUT there is a built-in special coprocessor to calculate each sine sample in the real time. They use two different inputs to generate NCO shown in fig 1, one is the digit N and the other is key clocking signal. Also have supplementary coprocessor, to estimate 1/N. Output frequency of the signal generated by this NCO sine wave is equal to: Fo = fs / N.

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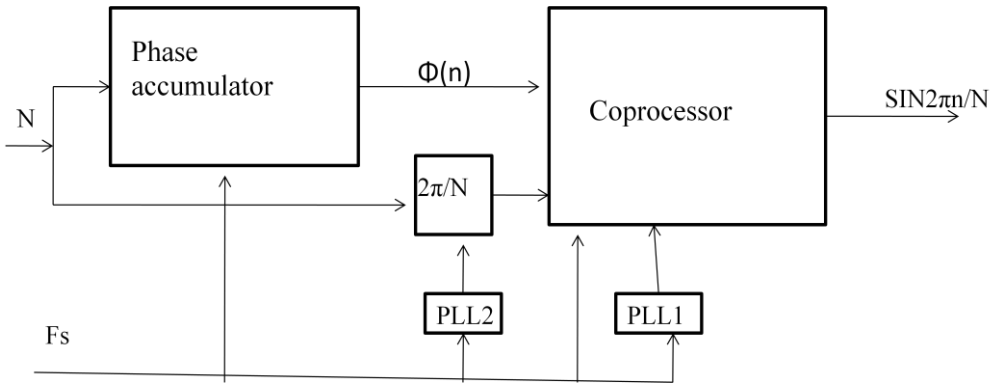

Fig 1: Block diagram of Taylor series based NCO

In [4], the author designed error-free NCO to increase the performance, as the traditional sine LUT has low performance. By this module they say that the frequency switching time is condensed as compared to the conventional digital oscillator. The designer finally makes this NCO as an outstanding contestant for applications requiring fast and phase-continuous frequency switching In [2] the author proposes a new technology of Frequency synthesis. The designer includes sub modules like phase Accumulator and Look-Up Table in Design and Realization of the NCO as seen in fig 3. In this work, Area is optimized by using Coefficients for only quarter cycle of sinusoidal waveform, which means the left over element is flipped and for negative cycle it has been inverted..

III. CONVENTIONAL COUNTER BASED NCO

So far there have been numerous methods predictable for implementing a NCO i.e., LUT NCO, Galois architecture based NCO, CORDIC algorithm based NCO[1] and so on .The elementary law in traditionalist methods mentioned above are, the phase accumulator yield increments with the same favoured increments to make favoured frequency .In conformist process, the consequent amplitude morals are weighed down into LUT. In LUT based approach, FCW resolute the output frequency, whose width in spin decides the figure of output frequencies that can be synthesized. The amount of feasible output frequencies is preset for a design and to alter it, the standards are to be recomputed.

Counter based NCO has been projected here with the objective to shrink the architecture complication, to preserve stable figure of samples irrespective of the production frequency. This move towards trim down the inflexibility in mounting the amount of achievable output frequencies. Here, the simulation results of counter based technique are presented and new approach of counter based NCO to increase productivity is achieved.

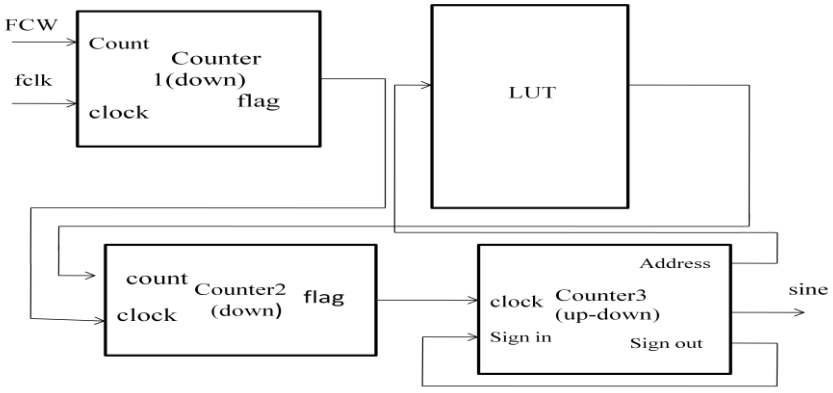

Fig 2: Counter based NCO block diagram

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Fig 3 shows the result of conventional counter based NCO. The planned scheme has numerous compensation which is as follows. The amount of samples are preset irrespective of the preferred frequency; the architecture is straightforward – only counters and LUT are used; there is no idleness as all the stored ideals are worn for each occurrence. Merely on altering the range of counter1, the output frequency range can be altered. The LUT extent required may not to be altered unless accuracy is to be changed. Also the LUT values must not to be recomputed. Though, the master clock frequency is to be scaled down by $4*2^M$ to attain the maximum probable output frequency, for this reason the architecture is retrained only for low frequency applications. If the quantization error has to be condensed, then the LUT word-length should be increased, which confines the highest output frequency possible for a given clock frequency.

Hence we can wrap up that for a meticulous LUT word-length there is an optimum value for the figure of samples which gives maximum SFDR and least quantization error. For a particular LUT word-length, if the figure of samples are not as much of the optimum value, then the quantization error is more since condensed number of quantization level. If the figure of samples are more than the optimum value custody M is constant, then also quantization error increases because the accurateness in LUT values corresponding to the sampling intervals is mislaid.

IV . **PROPOSED NCO**

In the conventional method, NCO produces single output with predefined set of frequency. To change the range the values have to be recomputed. The design produces only single output using three counters. Usage of area, power is more but produces single output. Hence the enhanced counter NCO is designed using frequency divider concept method .This method produces four outputs with different frequency range, which saves the hardware complexity. It has Global reset to reset the complete design. The proposed NCO architecture has multiple outputs for given input clock. Hence its throughput is more as conventional counter NCO. Instead of LUT Frequency divider is used to produce multiple outputs for given input.

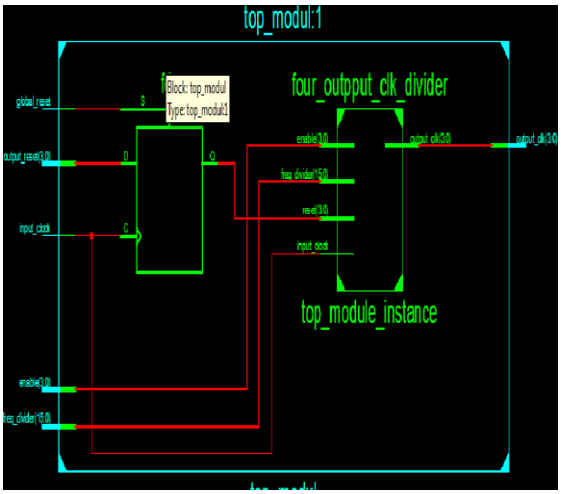

Fig 3: Proposed NCO block diagram with prime inputs

Using enable input of 4bit value, the frequency divider will divide the input clock to produce output. The input frequency is divided by user defined value. Fig 3 shows the schematic representation of four output clock. The main advantage of this design is only the required number of output can be enabled, rest can be disabled. This makes the NCO to give multiple outputs if the design needs many modules in single plat form such as System on Chip (SOC), system on board level. The output configuration for any design becomes easier by enabling and disabling outputs. For FPGA Spartan series PLL's are used to peak clock from nearest one. By making NCO to place in FPGA the required clock of particular frequency can be extracted easily, however system clock is to be applied initially to the design as input.

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V. APPLICATION OF NCO IN MANCHESTER DECODER

As we know there are many ways to approach design of a serial data-communications interface. Designer will use industry-standard protocols, such as I2C, UART, or SPI, as these are easier and more cost-effective. But in some cases even if the designer desire to revolve their own customized protocol, an admired approach is required to base and is called line code, or more generally known, digital baseband modulation. The waveform prototype of voltage or current which represent the 1s and 0s of digital data on a communication tie is called line coding. Line coding consists of representing the digital signal which is to be elated by an amplitude- and time-discrete signal and is optimally tuned for the explicit properties of the physical channel (of the receiving equipment).

The common types of line encoding are NRZ and Manchester encoding. NRZ encoding is a binary code in which 1s are represented by a positive voltage and 0s as a negative voltage, by means of no extra impartial or respite state. These pulses include extra energy than a RZ code. Contrasting RZ, NRZ does not contain a rest state. Since NRZ is not intrinsically a self-clocking signal and thus it requires some additional synchronization technique. Now the Manchester coding technique comes into picture which is self –clocking.

Here the goal is to show how the NCO and CLC peripherals are utilized as a Manchester Decoder, which are start in PIC Microcontroller. Conventional calculations which are utilized before takes firmware requesting and leaves greatly modest measure of CPU cycles to inspect application needs. Presently the accompanying methodology work freely of the CPU clock and incorporate zero CPU usage, which permits the architects to analyze their applications from the start with coding information. Information is accessible amid the first or second 50% of bit time contingent upon the encoding standard which are of two sorts "G.E. Thomas" , a "0" is transmitted by low-to-high move and a "1" is communicated by high-to-low move and "IEEE 802.3",where a '0'is transmitted by high-to-low move, "1" is communicated by low-to-high move which is the inverse of G.E. Thomas. This application utilizes G.E. Thomas strategy for coding.

The PIC Microcontroller uses this implementation which has four CLC blocks to realize combinational logic along with NCO to produce precise bit time. The following part covers the implementation of these blocks.

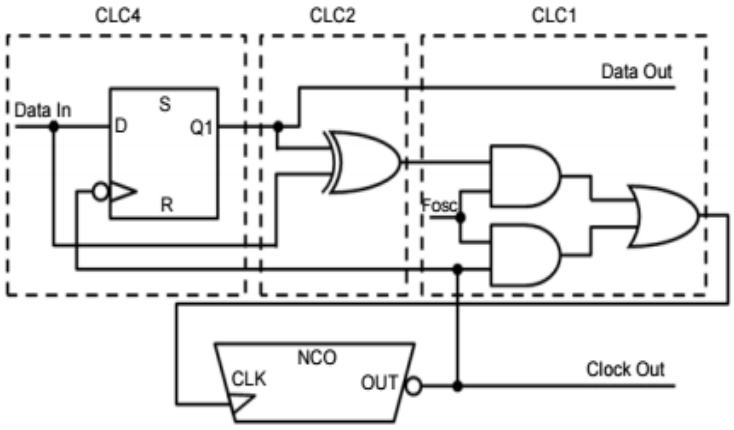

Fig4: Full Decoder block diagram

Stage 1 – D Flip-Flop (CLC4)

In this stage Manchester information is hooked customized on the declining edge of the clock signal, therefore the Recovered yield information is encouraged into the microcontroller. On clock falling edge information is examined and on raising edge information is steady to peruse, on the grounds that the information line on a rising clock edge

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Stage 2 – XOR Gate (CLC2)

As a transformation is guaranteed amidst every piece in Manchester encoding, a XOR door to guarantee that each mid-piece change gives us a rising edge for Stage 3. At the end of the day we are synchronizing our decoder in the main issue of each piece.

Stage 3 – NCO + AND-OR (CLC1)

The PIC microcontroller has a NCO unit which produces ¾ bit-time to limit information esteem. The NCO is worn in dynamic low Pulse Frequency mode to edit a heartbeat while ¾ bit time lapses. To include a settled esteem over and again at a predetermined clock rate to a collector, a clock source is required and is supplied by CLC1.These In the decoder these two pieces are the most critical in light of the fact that for every rising edge approaching out of Stage 2 , the squares produce an altered length beat. The yield of the NCO is nourished patron into the AND-OR door, hence that while the yield of Stage 2 goes to zero, then NCO will hold on timing anticipating it to flood. After the division is preeminent arranged, it gives a solitary ¾ bit length beat which is craved to set the NCO in its dynamic low state. The NCOCLK register is arranged for NCO attending to the yield beat width in dynamic state. On one event when a clock source is flourishing, NCO ends its dynamic heartbeat.

VI. SIMULATION RESULTS

The simulation studies involves the coding and simulation of the design which are done in cadence tool and some part of the design in Xilinx 14.7 tool. The conventional counter based NCO has 10 MHz operating frequency and the Proposed NCO has 50 MHz operating frequency. In the following sections, the simulation result of each module is discussed in detail. The Fig5 gives the result of single output counter based NCO, which has input values FCW=1,fclk=10khz .The output counter 3 is 4-bit valued counter, it produces only one output of 10 khz. Fig 6 shown below gives four output clock result ,in which two are enabled and each output is of variable frequency value of different range of detrimental value 2.output clock has 4 outputs among which output0,output1 are enabled and rest two outputs are disabled.output0 gives div by 10 , div by 5 and output 1 shows div by 2,div by 3.It has global reset of 1 bit to disable all outputs. Input clock is of 50Mhz. Fig 7 shows the Manchester decoded output, which uses NCO output as input clock, Fosc of 10ns.Data_in is encoded sequence 1101001 and decoded data is 110.the NCO gives 3/4th time of duty cycle, Fosc is of 10ns,which provides active pulse for NCO to work.

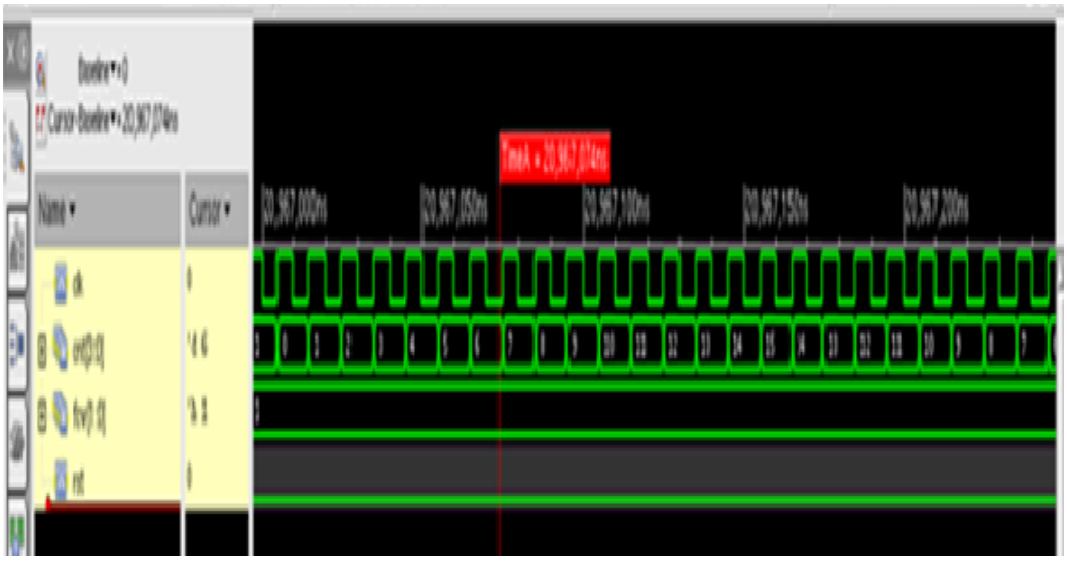

Fig 5: Simulation results of Conventional counter NCO

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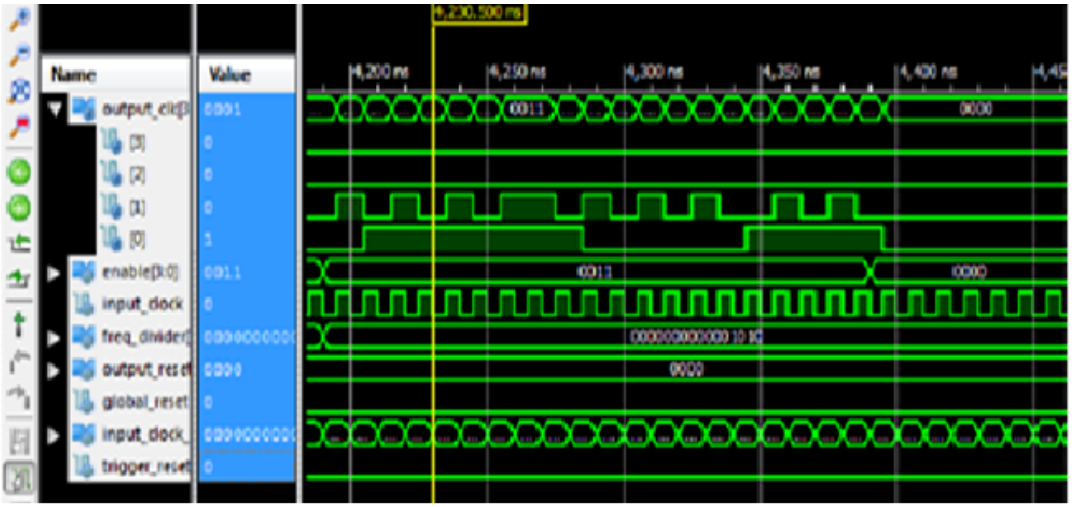

Fig 6: Simulation result of proposed counter NCO

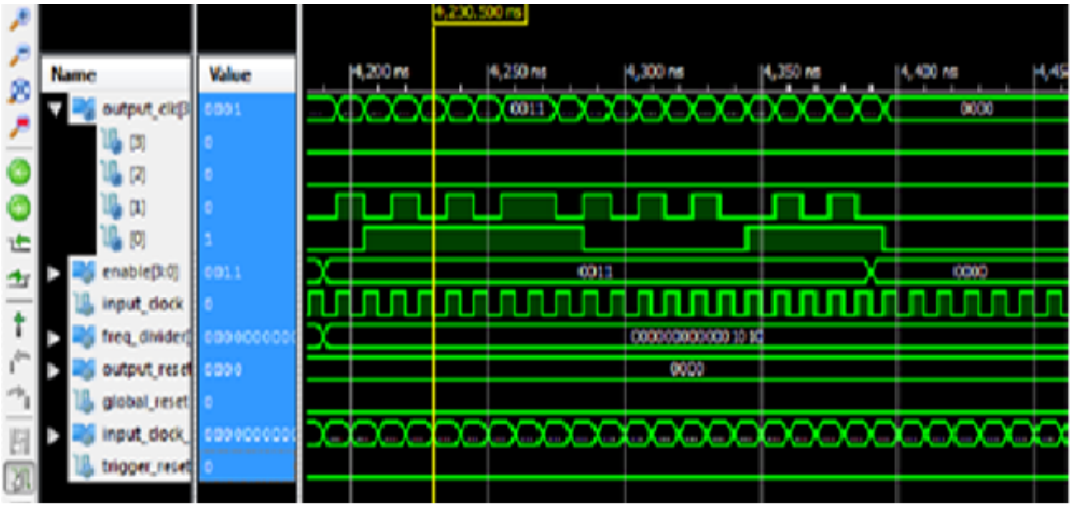

Fig 7: Simulation result of Manchester decoder

VII .CONCLUSION AND FUTURE WORK

The simulation results showed that the proposed algorithm performs better than Conventional counter using LUT. It produces single output with more delay for accessing count value from LUT. Hence new design is proposed which gives multiple outputs with minimum delay and counters. The advantages of this method are that output frequency range can be increased without altering the design and any re-computation. Also the numeral of samples inside the signal ruins constant irrespective of the output frequency of the signal. The proposed new NCO Produces multiple output with different frequency range which is user defined one. This signal is fed as input to Manchester decoder logic to collect the data bits which are encoded.

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The new counter based NCO can be enhanced further to produce many outputs by reducing still hardware(counter), and in the Manchester application the assumption is made that the first edge was a mid-bit transition. Application can be enhanced further in SOC Designs which works at multiple frequencies. In Manchester coding the problem is that one ¾ bit length following the first mid-bit transition have already missed first bit of data. So before the first bit is transmitted, it needs to occur a ½ bit length so the remaining data will synchronize with the mid-bit transitions. To return the encoded data line back to its default state a Stop bit may be necessary.

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