ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering
(An ISO 3297: 2007 Certified Organization)
Website: www.ijircce.com
Vol. 5, Issue 5, May 2017

Design and Implementation of Address Generator for WiMAX Deinterleaver

Rasika Ramchandra Kulkarni[1],Prof.Preeti Rajput[2],Dr.V N Nitnawre[3]

[1]PG scholar, Dept. of Electronics & Telecommunication, D Y Patil School of Engineering Academy, Ambi, Pune, India

[2]Assistant Professor, Dept. of Electronics & Telecommunication, D. Y. Patil School of Engineering Academy, Ambi, Pune, India

[3]Principal and Professor, D. Y. Patil School of Engineering Academy, Ambi, Pune, India

ABSTRACT: The project is about implementing the address generation circuitry of the 2-D deinterleaverused in the WiMAX transreceiver using the Xilinx field-programmable gate array (FPGA) for all permissible code rates and modulation schemes. Since the implementation is done on FPGA, the techniques take the advantage of digital domain. Finite machine based address generator for all permissible code rates and modulation schemes reduces the complexity of implementation on FPGA.2-D translation of the functions used in WiMAX channel deinterleaver to claim efficient hardware architecture. The disadvantages of the derivations used in the existing systems do not clearly explain the design issues, particularly for 64-quadrature-amplitude modulation (QAM). Hardware implementation of floor function is very complex and consumes abnormally large amount of resources as well as Conventional LUT-based technique is found to be unattractive from many aspects such as slowness in operation, consumption of large logic resources leading to inefficiency in resource utilization, etc..

KEYWORDS: Energy efficient algorithm; Manets; total transmission energy; maximum number of hops; network lifetime

I. INTRODUCTION

WiMAX is a standards-based technology enabling the delivery of last mile wirelessbroadband access as an alternative to wired broadband like cable and DSL. WiMAX provides fixed , nomadic, portable and mobile wireless broadband connectivity without the need for direct line-of-sight with a base station [7].

There are two types of usage models for WiMAX family of standards - fixed usagemodel and mobile usage model. The difference between these two systems is the ground speed at which the systems are designed to manage. Wireless access can be divided into 3 classes : stationary, pedestrian and vehicular. The stationary and pedestrian classes are served by the fixed wireless access system and mobile wireless access system address the vehicular class.

Fixed WiMAX is used to refer to systems built using 802.16-2004 (802.16) and theOFDM PHY as the air interface technology. Fixed WiMAX offers cost effective point to point and point to multipoint solutions. WiMAX provides fixed, portable or mobile non-line-of sight service from a base station to a subscriber station, known as customerpremise equipment (CPE).Mobile WiMAX is used to refer to systems built using 802.16e-2005 and the OFDMAPHY as the air interface technology. Both fixed and mobile services are delivered by using mobile WiMAX implementations[1].

II. RELATED WORK

In [2] reduce the frequency of memory access in a deinterleaver, the incomingdata streams are grouped into block. This is done by using a conventional LUT based CMOS address generator for WiMAX. This is applicable for DVB and IEEE 802.16 standards. The deinterleaving functions is based on multiple single-port memory banks. This method can also be applied to other communication systems which adopt the similar deinterleaving approach.In paper [3] address interleaver for the WLAN application is implemented byusing conventional LUT-based technique on FPGA.This paper [4] describes a hardware description language (VHDL) based implementation of address generator for IEEE 802.16e channel interleaver. In this, the implementation is based on careful analysis of the address generation patterns used for WMAN standard. The architecture obtained is implemented in FPGA and has less area and delay.This paper [5]

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering
(An ISO 3297: 2007 Certified Organization)
Website: www.ijircce.com
Vol. 5, Issue 5, May 2017

implements a finite-state machine (FSM)-based address generator of the interleaver for all permissible code rates and modulation schemes. The architectureobtained is implemented in FPGA and has higher operating frequency and betterresource utilization in FPGA.. In this paper [6] to get efficient hardware architecture, a 2-D translation of the functions used in WiMAX channel deinterleaver is used. The disadvantage of this is that modulus and floor operators are used within the interleaver functions.

III. PROPOSED ALGORITHM

A. *Interleaver/ Deinterleaver:*

Interleaving is a process to make a system more efficient, fast and reliableby arranging data in a noncontiguous manner. There are many uses forinterleaving at the system level, including:

- Storage: As hard disks and other storage devices are used to store userand system data, there is always a need to arrange the stored data in anappropriate way.
- Error Correction: Errors in data communication and memory can becorrected through interleaving.
- Multi-Dimensional data structures.

B. *Address Generation in Interleaver:*

The block interleaver/deinterleaver exploits different interleaver depths Ncbps. to incorporate various code rates and modulation schemes forIEEE 802.16e. The data stream received from the RS-CC encoder is permutedby using the two-step processes described by equations 1 and 2. Thesesteps ensure mapping of coded bits onto nonadjacent subcarriers and alternateless/more significant bits of the modulation constellation.

$$m_k = \left(\frac{N_{cbps}}{d}\right) . (k \,\%\, d) + \left\lfloor \frac{k}{d} \right\rfloor \qquad \text{eq (1)}$$

$$j_k = s . \left\lfloor \frac{m_k}{s} \right\rfloor + \left(m_k + N_{cbps} - \left\lfloor \frac{d . m_k}{N_{cbps}} \right\rfloor \right) \% \, s \qquad \text{eq (2)}$$

The address generator of WiMAX deinterleaver along with itsmathematical background is presented. Due to the presence of a floor function in their direct implementation on an FPGA chip is not feasible. As =16 is chosen, the number of rows are fixed (=d) for all "Ncbps", whereas the number of columns are given by "Ncbps/2". The mathematical foundation of the correlation between the addresses, as derived in this brief, is represented by equations 3 and 4, i.e.

$$k_{n,\,QPSK} = \{d . i + j \quad for \ \forall j \ and \ \forall i \qquad \text{eq (3)}$$

$$k_{n,\,16\text{-}QAM} = \begin{cases} d . i + j & for \ j\%2 = 0 \ and \ for \ \forall i \\ d . (i+1) + j & for \ j\%2 = 1 \ and \\ & for \ i\%2 = 0 \\ d . (i-1) + j & for \ j\%2 = 1 \ and \\ & for \ i\%2 = 1 \end{cases} \qquad \text{eq (4)}$$

Where j =0,1,..., −1 and i=0,1,..., ( )-1 represent the row and column numbers respectively. In addition, Ncbpsrepresents the deinterleaver addresses. General validity of equations 3 and 4 to represent thecorrelation between addresses has formally been proven using the algebraic analysis in [6], which lacks the involvement of equations 3 and 4. The outcome of this analysis using equations 3 and 4 provides the same result. Thus, equation 3 and 4 play the pivotal role in establishing formal mathematical foundation of address generator for WiMAX deinterleaver. The address generator for WiMAX deinterleaver eliminates the requirement of floor function while generating write addresses.

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering
(An ISO 3297: 2007 Certified Organization)
Website: www.ijircce.com
Vol. 5, Issue 5, May 2017

IV. SIMULATION RESULTS

The Verilog [10] code is developed for the WiMAX deinterleaver addressgenerator for QPSK, 16-QAM and 64-QAM for all Ncbps values. The design issimulated and synthesized using Xilinx ISE design suite tool and it is successfullyimplemented on Xilinx SPARTAN-3E FPGA (XC3S500E) device [11]. HDLsynthesis report is shown in Table 1.

WiMAX Project Status (05/16/2014 - 23:20:51)			
Project File:	wimacombined.xise	Parser Errors:	No Errors
Module Name:	WiMAX	Implementation State:	Synthesized
Target Device:	xc3s500e-5fg320	• Errors:	No Errors
Product Version:	ISE 14.6	• Warnings:	94 Warnings (54 new)
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	
Environment:	System Settings	• Final Timing Score:	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	27	126800	0%
Number of Slice LUTs	703	63400	1%
Number of fully used LUT-FF pairs	22	708	3%
Number of bonded IOBs	16	210	7%
Number of BUFG/BUFGCTRLs	1	32	3%

Table 1: HDL Synthesis report

The address generator for WiMAX deinterleaver approach is compared with LUT based approach with respect to FPGA parameters. In WiMAX deinterleaver approach, three block RAMs are used, i.e., one for each modulation scheme to house the address LUT of various interleaver depths (Ncbps). Table 2shows the comparison between proposed approach and LUT based approach with respect to FPGA parameters. In spite of the smart use of block RAM in LUT.based approach, this results in a significant reduction in occupancy of FPGAslices (by 100%) and LUTs (by 94.16%). This comparison clearly proves the low complexity and hardware efficiency of WiMAX deinterleaver approach over LUT APPROACH.

FPGA Parameters	Performance of proposed technique	Performance of LUT based technique[8]	% Reduction/ Improvement in resource utilization	Remarks
Slices	0%	17.66%	- 100	Significant reduction
Flip Flops	3%	0.78%	74	Significant improvement
4 input LUTs	1%	17.15%	-94.16	Significant reduction
Operating frequency	89.902 MHz	62.51 MHz	30.46	Significant improvement

Table 2: Comparison between proposed approach and LUT base

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering
(An ISO 3297: 2007 Certified Organization)
Website: www.ijircce.com
Vol. 5, Issue 5, May 2017

APPROACH

Furthermore, to make the design more hardware efficient, embeddedmultiplier of the Xilinx SPARTAN-3E FPGA is used to implement the ML3 block of Fig. This comparison also shows almost 30.46% improvement in this workwith respect to operating frequency over LUT approach as FPGA equivalent maximum frequency of the latter is found to be 62.5 MHz, whereas maximum frequency for WiMAX deinterleaver approach is found to be 89.902 MHz. The reasons behind these improvements are low-complexity, optimized and shared hardware design and the use of FPGA‟s embedded multiplier, which, in turn, reduces interconnection delay inside FPGA. RTL schematic of the address generator for WiMAX deinterleaver. The hardware implementation setup is shown in Fig.

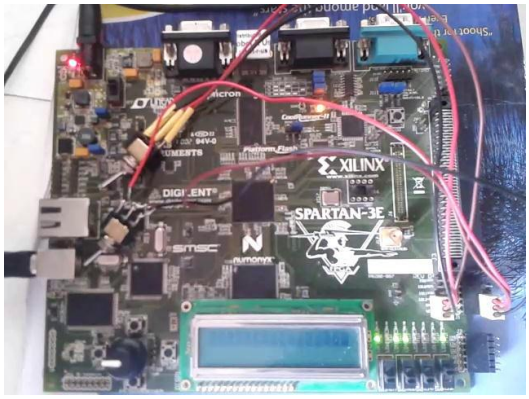

Fig: Hardware implementation setup

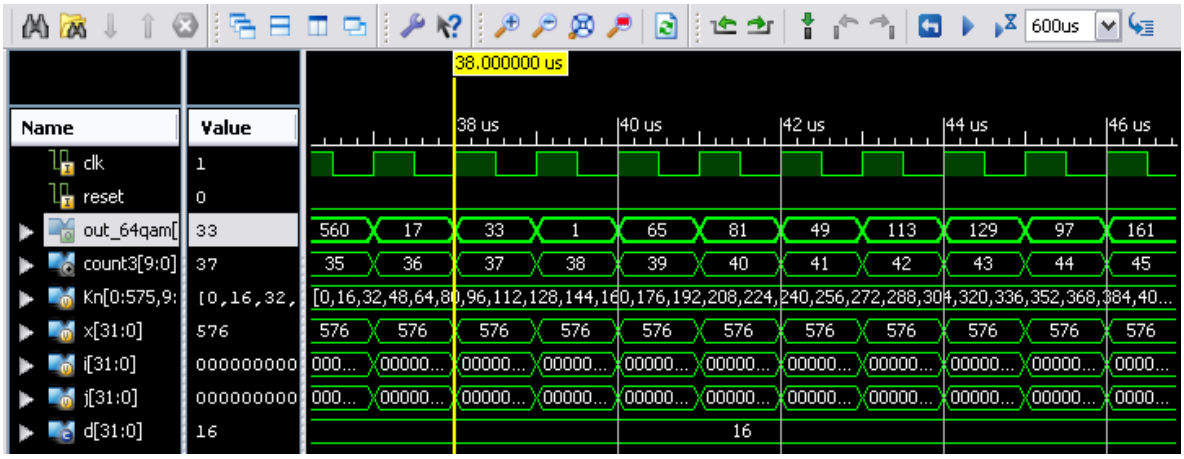

Fig.2.1: Simulation result of combined structure when mod_type = 00

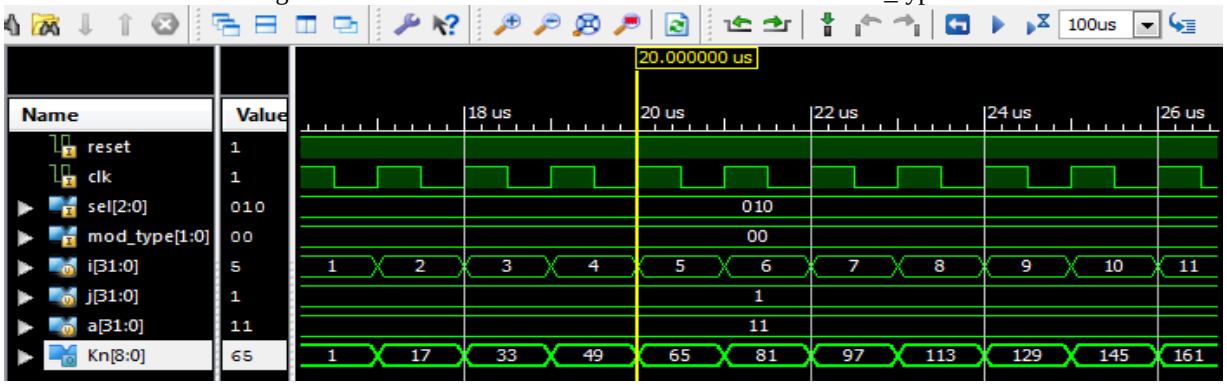

Fig.2.2: Simulation result of combined structure when mod_type = 01.

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering
(An ISO 3297: 2007 Certified Organization)
Website: www.ijircce.com
Vol. 5, Issue 5, May 2017

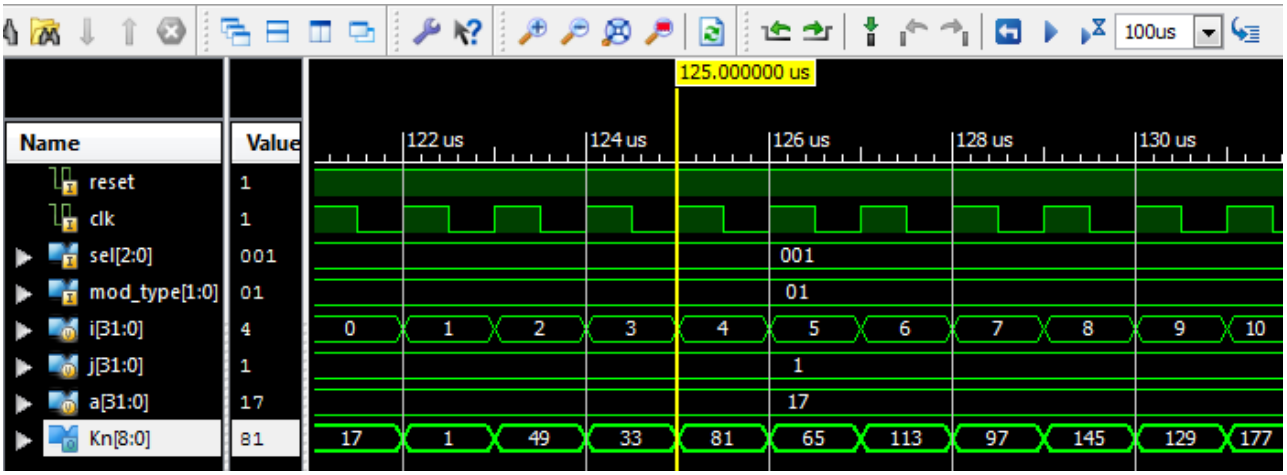

Fig.2.3: Simulation result of combined structure when mod_type = 10.

V. CONCLUSION AND FUTURE WORK

WiMAX Transceiver is a system which is used for transmission and reception ofwireless data in the WiMAX technology. A detailed literature survey is carried out on WiMAX deinterleaver address generator. A design along with its mathematical formulation for address generation circuitry of the WiMAX transceiver deinterleaver is presented. It supports all permitted code rates and modulation schemes as per IEEE 802.16e.

The design is coded using Verilog HDL. Simulation and synthesis is carried out using Xilinx ISE Sim. The simulation results for QPSK, 16-QAM and 64-QAM for all Ncbps values are presented.

The design is successfully implemented on Xilinx SPARTAN-3E FPGA (XC3S500E) device for all Ncbps values and modulation schemes. Synthesis report is also presented and compared with LUT based approach with respect to FPGA parameters. In future the design of address generation circuitry for WiMAX deinterleaver can be extended for higher Ncbps values and other modulation schemes.

REFERENCES

1. J. G. Andrews, A. Ghosh and R. Muhamed, Fundamentals of WiMAX:Understanding Broadband Wireless Networking. Upper Saddle River, NJ,USA: Prentice-Hall, 2007.
2. W. Konhauser, “Broadband wireless access solutions progressive challengesand potential value of next generation”, Wireless Pers. Communication. vol.37, no. 3/4, pp. 243–259, May 2006
3. Y. N. Chang and Y. C. Ding, “A low-cost dual mode deinterleaver design”,Proc. International Conference Consum. Electron, 2007,
4. A. A. Khater, M. M. Khairy and S. E. D. Habib, “Efficient FPGA implementationfor the IEEE 802.16e interleaver,” Proc. International Conference Microelectron.,Marrakech, Morocco, 2009, pp. 181–184.
5. B. K. Upadhyaya, I. S. Misra and S. K. Sanyal, “Novel design of addressgenerator for WiMAX multimode interleaver using FPGA based finite state machine”, Proc. 13th International Conference Computer and InformationTechnology, Dhaka, Bangladesh, 2010, pp. 153–158.
6. R. Asghar and D. Liu, “2D realization of WiMAX channel interleaver forefficient hardware implementation”, Proc. World Academy ScienceEngineering Technology, Hong Kong, 2009, vol. 51, pp. 25–29.
7. B. K. Upadhyaya and S. K. Sanyal, “Efficient FPGA Implementation ofAddress Generator for WiMAX Deinterleaver” IEEE Transaction on Circuitsand Systems-II: express briefs, vol. 60, no. 8, august 2013.
8. Local and Metropolitan Networks - Part 16: Air Interface for Fixed BroadbandWireless Access Systems, IEEE Std. 802.16-2004, 2004.
9. B. Sklar, Digital Communications: Fundamentals and Applications, Prentice-Hall, Englewood Cliffs, NJ, USA, 2nd edition, 2001
10. Muthukumar S, Dr.Krishnan .N, Pasupathi.P, Deepa. S, “Analysis of Image Inpainting Techniques with Exemplar, Poisson, Successive Elimination and 8 Pixel Neighborhood Methods”, International Journal of Computer Applications (0975 – 8887), Volume 9, No.11, 2010