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Power Efficient 16-bit Shift Register Using GDI Based Delayed Pulsed Generator and Dual Edge Latch In 35nm Technology

Shailendra Yadav[1], Deepak Kumar[2]

M.Tech Scholar (VLSI Design & Embedded System), Dept. of ECE, RGPV, VIST, Bhopal, M.P., India[1]

Assistant Professor, Dept. of ECE, Vidhyapeeth Institute of Science and Technology, Bhopal, M.P., India[2]

ABSTRACT: Power consumption, delay and area reduction play major role in a sequential circuit design. A noble approach to design a dual edged delayed pulse latch based shift register with reduce area and power is proposed. The Shift register is a basic functional unit in digital circuit and image processing such as digital filers, transceivers and image processing ICs. This paper basically focuses on the implementation of the shift register using compact logic of modified delayed clock pulse generator (by using GDI technique) and sequential array of dual edge pulse latches. A 16 bit shift register is designed using latches and delayed clock generator with Vdd=0.3V and simulation isdone byusing Tanner EDA v16.01 TOOL in 35nm CMOS technology.

KEYWORDS: Dual edge pulse latch, GDI (Gate Diffusion Input), Delayed clock pulse generator, Integrated Circuit (IC), Image processing, Complementary metal oxide semiconductor (CMOS).

I. INTRODUCTION

A shift register is a sequential logic circuit which can shift its data in one or both directions. The simplest shift register simply connects the flip-flops to their respective neighbour with the clock controlling the operation. Several D flip-flops may be grouped together with a common clock signal to form a register. Because each flip-flop can store one bit of information, a register with n D flip-flops can store N bits of information. But in recent flip-flops are replaced with pulsed latches for compacting the layout dimensions because pulse latch is smaller than a flip-flop. By using multiple non overlapping trigger signals generated by delayed clock pulse generator, timing problem between pulse latches can be solved. Shift register are commonly used in many applications such as digital filters, communication transceivers and image processing ICs.

The organization of paper starts with a brief introduction pertaining to the section I. There after section II proposes the steps approaching the shift register. Section III illustrate brief description of the proposed architecture of delayed pulsed generator and latches. Section IV comprises the simulation and result of shift register. Finally significant result are summarized in section V.

II. ARCHITECTURE OF SHIFT REGISTER

The 16 bit shift register is divided into four sub shift register to reduce the number of delayed pulse signal. A 4 bit sub shift register with four word length consist of five latches and it performs right shift operations with five non overlap delayed clock pulse signals (CP1, CP2, CP3, CP4, T). In the 4 bit sub shift register_1, IN is a data signal input followed by first latch, here four latches store 4bit data (Q1, Q2, Q3, Q4) and the last latch stores one temporary data bit T1 which will be stored in first latch (Q5) of the 4 bit sub shift register_2 and this process further continue for next sub shift register. For implementing 16 bit shift register four sub shift register having five latches are essential, it means sub shift register having four word length. Total 20 latches are used to design 16 bit shift register. By using the same process we can implement N number bit of shift registerfor increasing the storage size of shift register. T1, T2, T3, T4 are temporary bits.

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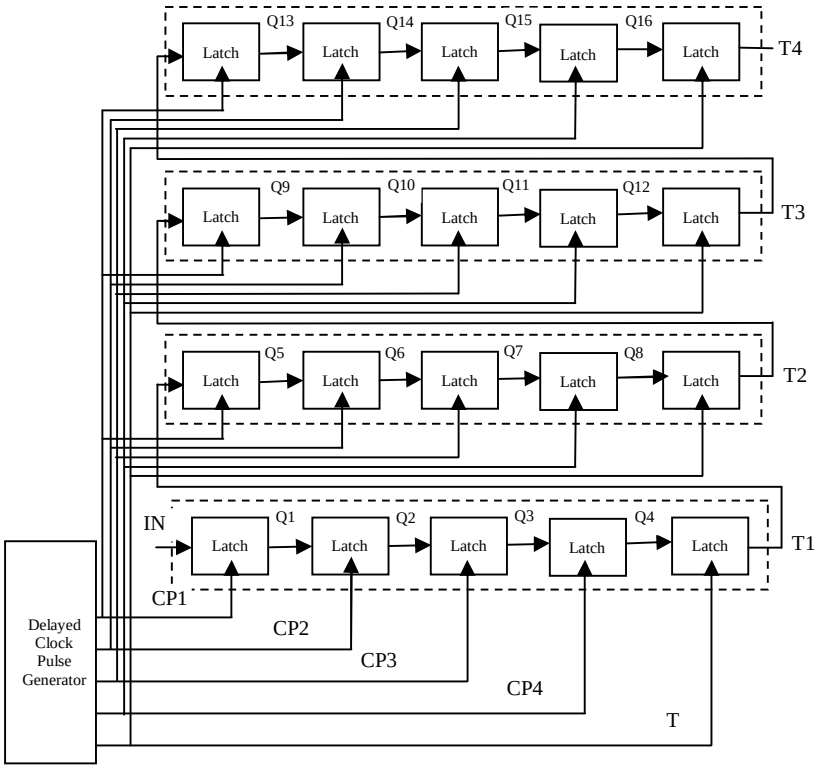

Fig. 1. Block diagram of proposed 16bit Shift Register.

Main components of shift register are Pulsed latch and delayed pulsed clock generator, that are briefly described in this section. Now a days flip-flop is replaced by pulse latch to reduce the power consumption in shift registers. Delay should be introduce to overcome timing problem. It has two inputs data (D), clock (CLK) and a output (Q) as shown in fig. 2.

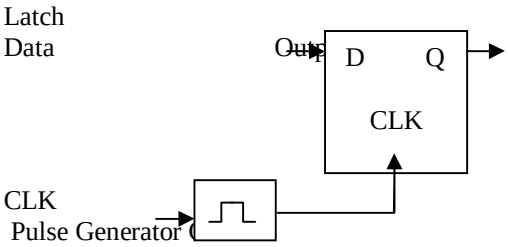

Fig. 2. Block diagram of latch with clock pulse.

For generation of non-overlap delayed clock pulse a pulse generator is required. Figure 3 illustrate the basic block diagram of delayed clock pulse generator circuit and also illustrates clock pulse circuit.It uses separate clock pulse circuit, here delay is introduce between the clock pulse circuit to generate delayed clock pulse which does not overlap each other. For bit word length 16 bit shift register requiresdelayed clock pulse generator having five clock pulse circuit with four delay. At the output of clock pulse circuit a buffer is used to produce strong output signalsCP1, CP2, CP3, CP4, Tas shown in fig. 5.

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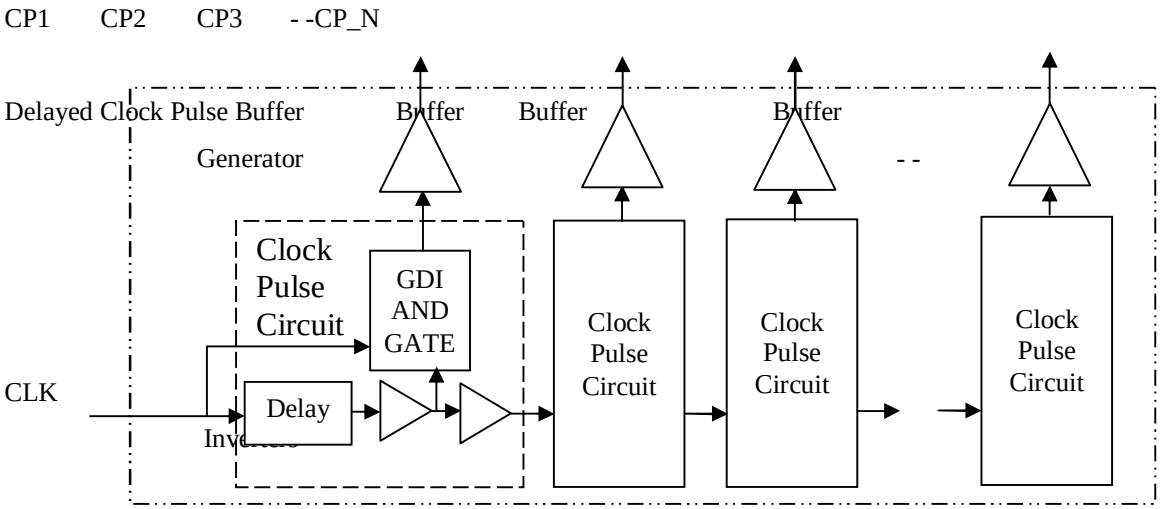

Fig. 3. Block diagram of delayed clock pulse generator.

III. PROPOSED ARCHITECTURE OF DELAYED PULSED GENERATOR AND LATCHES

The modified latch uses two cross-coupled inverters in fig. 4 which consist four transistors and update the data with two NMOS transistors N_1 and N_2. It has two differential data inputs D, Db and a clock signal CLK. When clock signal CLK is high both N_1, N_2 turns ON and the input data D, Db is updated. On the contrary when clock signal is low both N_1, N_2 turns OFF. This design uses less amount of transistors than SSASPL.

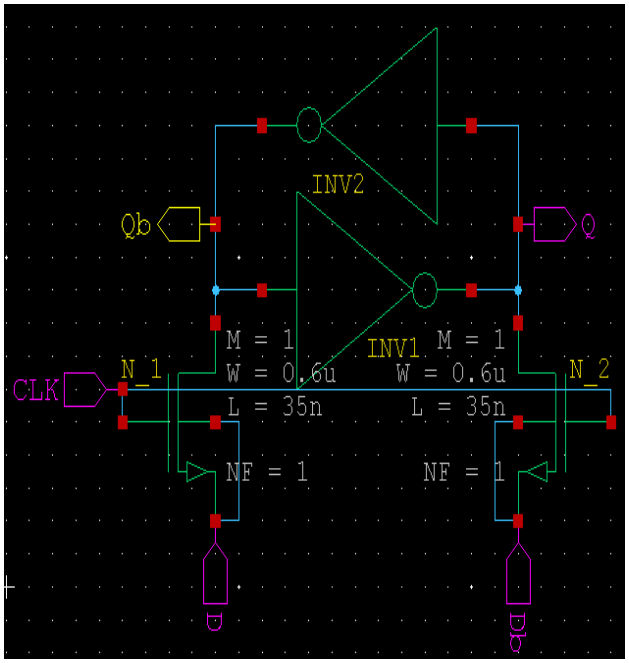

Fig. 4. Schematic of proposed Latch

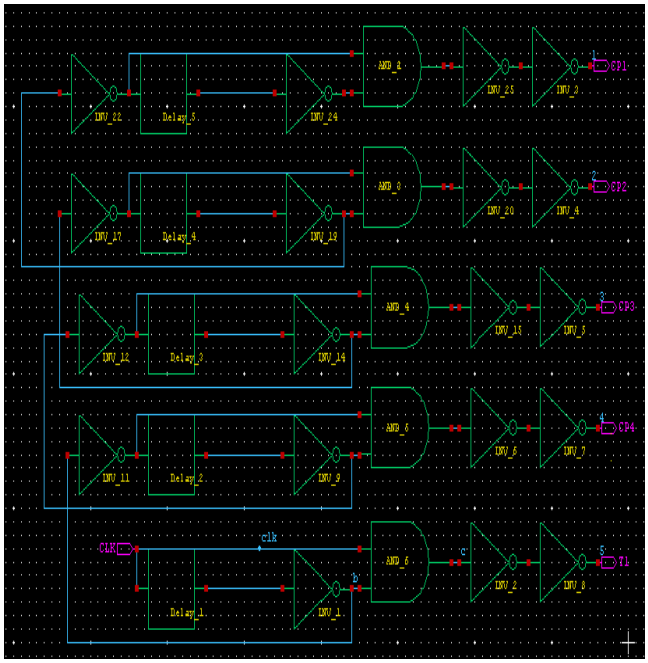

Fig. 5. Schematic of proposed Delayed clock pulse generator.

Delayed clock pulse generator is implemented similarly shown in fig. 3. In proposed delayed clock pulse generator mod-GDI technique is used for anding clock inputs to generate non-overlapped delayed clock pulses. Fig. 4 and fig. 5 illustrate the schematic of proposed latch and delayed clock pulse generator respectively. Both of these reduce the average power, static power, dynamic power and area.

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IV. RESULTS AND DISCUSSION

This paper describes the design and implementation of power efficient shift register by using modified delayed clock pulse generator and dual edge latch. Simulation is done using Tanner EDA tool v16.01 in 35 nm technology. The table 1 shows theperformance parameter of Latch, in this table we also compare the number of transistor used in both SSAPL based latch and proposed dual edge latch.

Table 1. Performance parameter comparison of latch.

S. No.	Parameters		SSASPL	Proposed Latch
1.	No. of Transistor	Total	7	6
		Clock	1	2
2.	Total power consumption		3.3	0.62
3.	Power consumption of data path (uW)		2.57	0.58
4.	Power consumption of clock load (uW)		0.73	0.04

Table 2 shows the Performance parameter comparison of Delayed clock pulse generator respectively. It shows the 10 number of transistor is used to implement delayed clock pulse generator circuit on the other hand clock pulse generator requires 14 number of transistor. Hence the proposed delayed clock generator is area efficient. It also consume less power as compare to clock pulse generator.

Table 2. Performance parameter comparison of delayed clock pulse generator.

S. No.	Parameters	Clock pulse generator	Proposed delayed clock pulse generator
1.	No. of Transistor	14	10
2.	Power consumed by each clock pulse circuit (uW)	27.6	2.53

The table 3 show the comparative analysis of proposed shift register with single edge and dual edge SSASPL shift register. Results of power consumption are showing in both microwatt and percentage. Proposed shift register consume 40.54 micro watt which is 50.73 percent of single edged SSASPL based shift register.

Table 3. Performance comparison of 16bit shift register.

S. No.	System	Power consumption (in uW)	Power consumption (in %)
1.	SSASPL based shift register (single edged)	79.9	100
2.	SSASPL based shift register(dual edged)	45.31	56.70
3.	Proposed shift register	40.54	50.73

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Fig. 6 is showing schematic block diagram of proposed 16 bit shift register. Fig. 7 showing the result of 16 bit shift register, it is a snapshot of log file generated by T-spice.

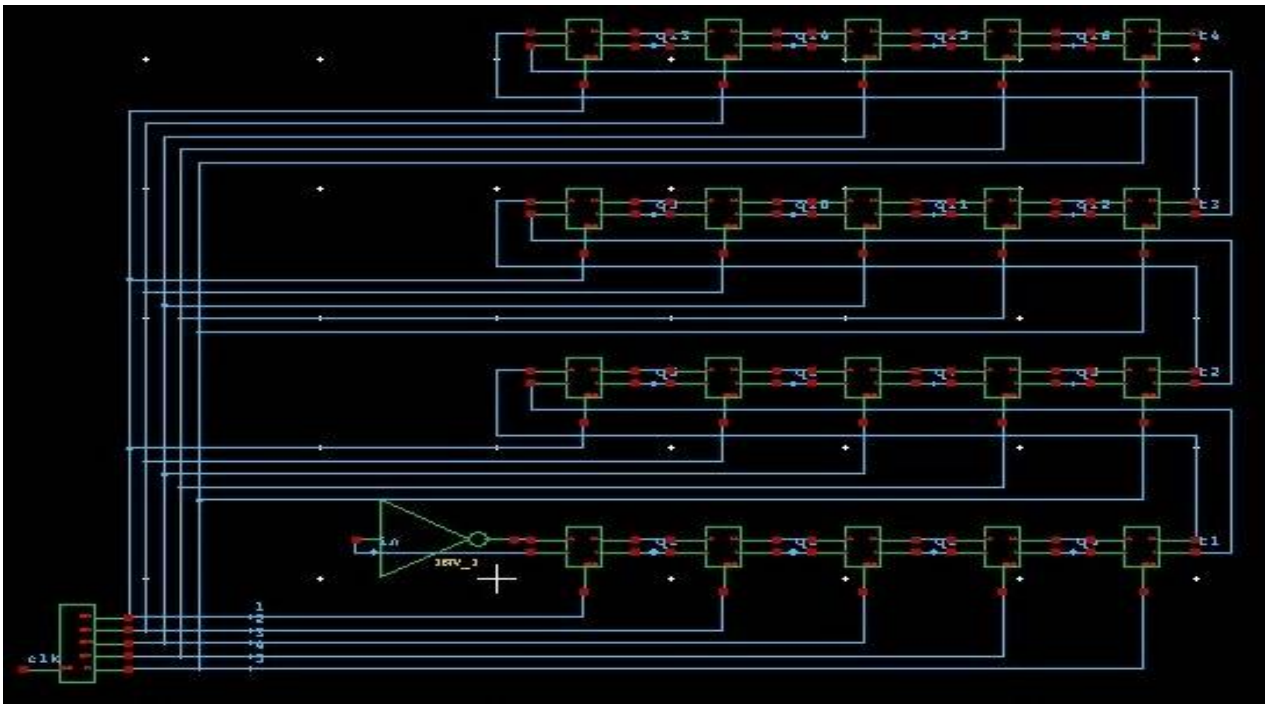

Fig. 6.Schematic diagram of 16bit proposed shift register.

Fig. 7 showing the result of 16 bit shift register, it is a snapshot of log file generated by T-spice. It shows value of average power consumed which is 4.054153e-005 watts also showing the value and time of maximum and minimum power consumed.

```
Power Results

vi from time 3e-009 to 4e-008
Average power consumed -> 4.054153e-005 watts
Max power 3.285769e-004 at time 3.93951e-008
Min power 1.677740e-008 at time 7.41039e-009


Parsing                              0.05 seconds
Setup                                0.20 seconds
DC operating point                   0.80 seconds
Transient Analysis                  27.25 seconds
Overhead                             0.70 seconds
-----------------------------------------------
Total                               29.00 seconds

Simulation completed
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Fig. 7.Result log file of 16bit proposed shift register.

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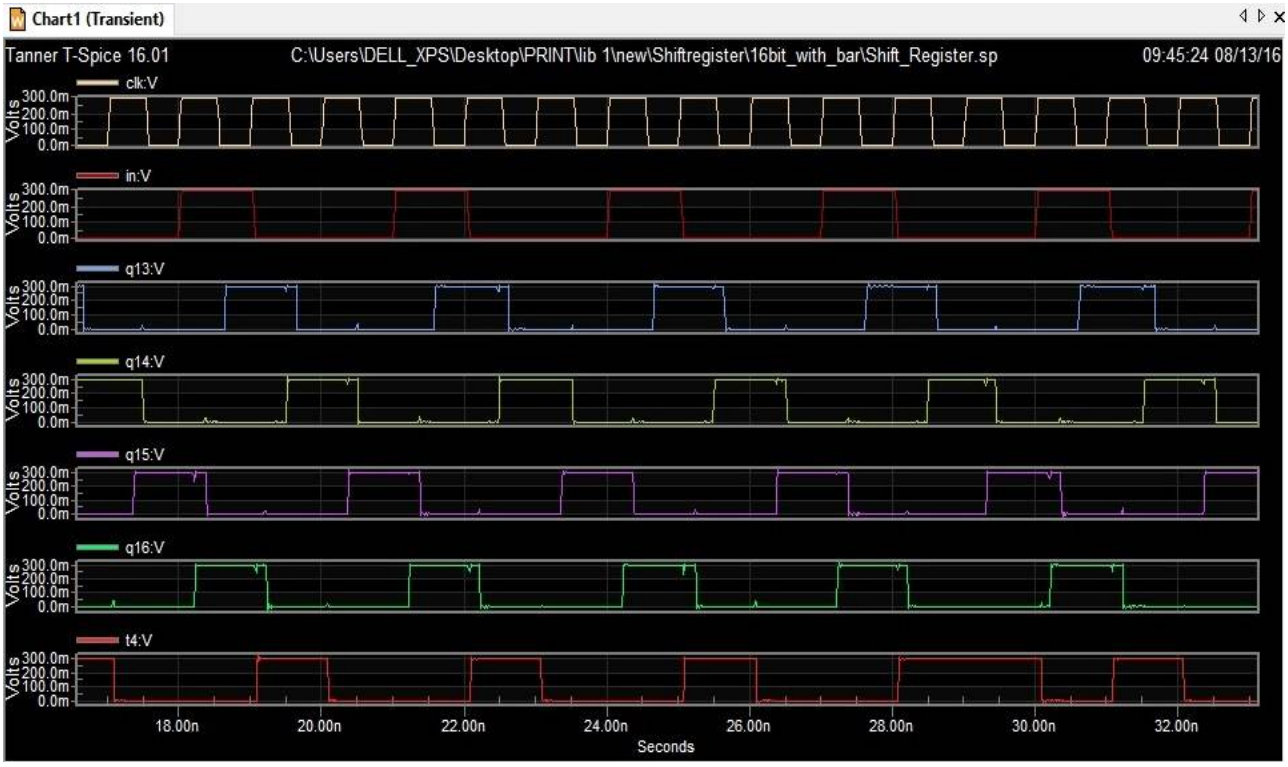

Fig.8. Waveform of 16bit proposed shift register.

Fig. 8 illustrate the timing diagram of proposed 16 bit shift register here waveform showing transition of input (in) through latches, q13, q14, 15, q16 and t4 is output of latches in forth sub shift register.

Chart 1.Power consumption graph of proposed 16 bit shift register.

Chart 1 shows the power consumption with respect to time of proposed 16 bit shift register and the average power consumption is40.54uW.

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Chart 2 is showing the comparison of power consumption by proposed 16 bit shift register with SSAPL based shift register in percentage (%) and micro watt (uW). First two bar indicating power consumed by SSAPL single edge based shift register, the second two bars indicating the power consumption of SSASPL Dual edged and the last two shows the power consumed by the proposed shift register which is less as compare to other two.

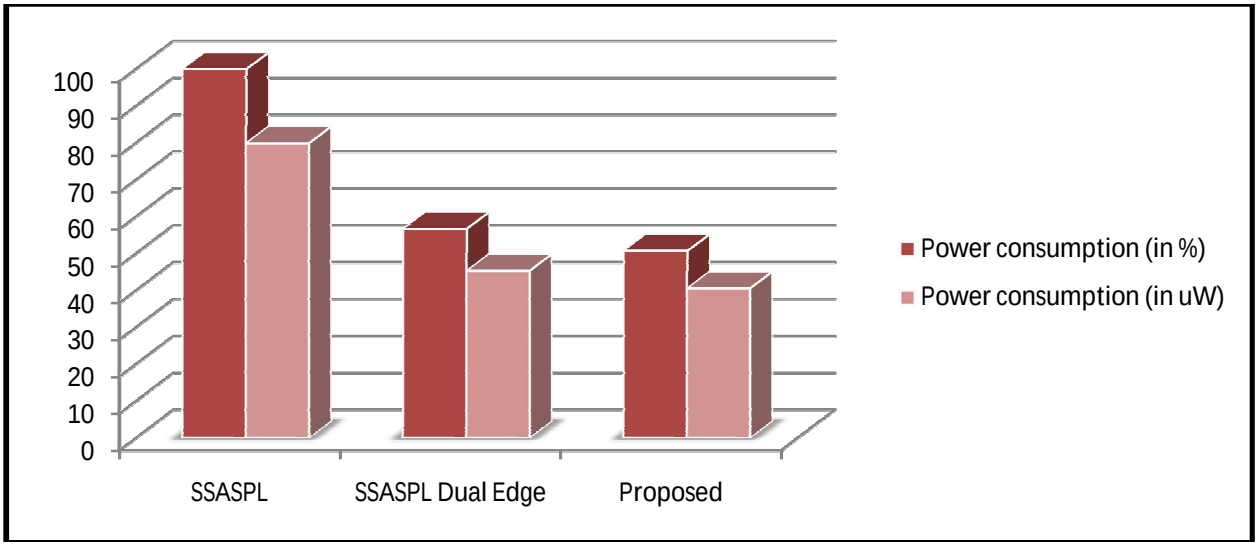

Chart2. Comparison of power consumption by proposed 16 bit shift register with SSAPL based shift register.

V. CONCLUSION AND FUTURE WORK

In this paper we have proposed power efficient modified shift register using modified delayed clock pulse generator and duel edge latch. Simulation is done using Tanner EDA v16.01 Tool in 35nm technology. Since our objective was low power consumption in shift register and power consumption is found to be 40.54uW it is 50.73% of SSASPL based shift register (single edged), hence we achieved our objective. In this paper we have design shift register without using MTCMOS or adiabatic technique.Design a shift register using these techniques can lead to enhance overall performance by reducing leakage current.

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BIOGRAPHY

Shailendra Yadav,attained his B.E. in Electronics & Communication Engineering from Trinity Institute of Technology and Research, Bhopal, MP, India, in 2013. And M.Tech. Scholar in the stream of VLSI design and Embedded System from Vidhyapeeth Institute of Science and Technology, Bhopal, MP, India in 2016. His current research interests include low power and area efficient VLSI design, digital IC design and embedded system.