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# Design and Implementation of Fault Tolerant Digital System

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**ABSTRACT**: This paper proposes an architecture for self- repairing digital system inspired by an endocrine cellular communication in human body. Fault tolerance means system should be able to continue functioning even in the presence of fault. This system simplifies the rerouting process without any additional hardware and minimizes unutilized resources. It consists of structural layer and gene control layer. The structural layer consists of working modules, spare modules and their interconnections. In these system, each module connecting with four spare modules for replacing faulty working modules at four times. Gene control layer controls the operation of modules. The module is the encoded data, called the genome, contains information about the function and the connection.

**KEYWORDS**:Self- repairing system; stem cell; Index changing unit; differentiation unit; working cell

## I. INTRODUCTION

Reliability has always been an issue with digital system. Reliability means measurement of whether a system can run continuously without failure. Reliability is theoretically defined as the probability of success, as the frequency of failures; or in terms of availability, as a probability derived from reliability and maintainability.

Various types of faults that can occur in VLSI system can be classified as either soft (transient) or permanent (hardware) ones. Transient faults are induced by temporary environmental conditions, such as cosmic rays and electromagnetic interference. Permanent faults are the result of irreversible device and circuit changes.A new system is proposed which improves routing by lowering hardware overhead along with increasing the size of circuit and reducing hardware unutilized for fault recovery. Fig. 1 shows endocrine cellular communication.

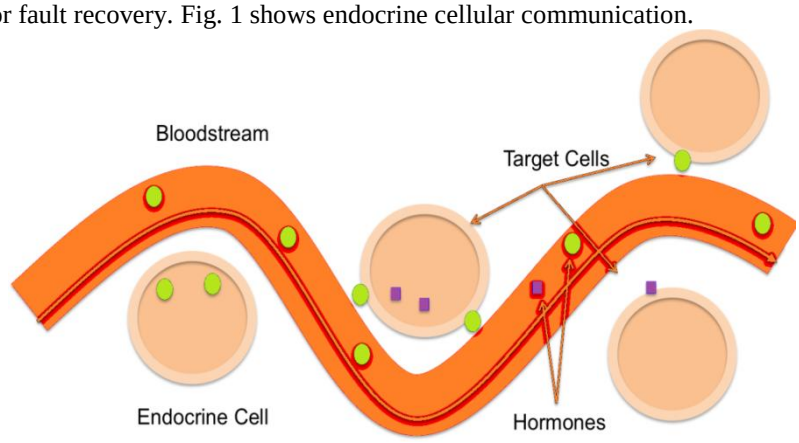


Fig. 1 Endocrine Cellular Communication

Endocrine cellular communication [1]is the most common type of cell signalling and involves sending a signal throughout the whole body by secreting hormones into the bloodstream of animals or the sap in plants. The cells that produce hormones in animals are called endocrine cells.Endocrine cells release hormones (green) into the blood stream where they are able to travel and bind to target cells located downstream. The binding of these hormones to target cells may lead to cellular responses such as the release of a second hormone (blue).

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## II. RELATED WORK

During the past few years, dual modular redundancy (DMR) and triple modular redundancy (TMR) [2] methods were used for development of fault tolerant system. Triple modular redundancy (TMR) [3], consists of parallel digital components (modules), all of which have equivalent logic and the same truth tables. The same input is fed to the modules and a voter gives the majority as the system output. One usage of TMR is for the protection of combinational and sequential logic in reprogrammable logic devices, called Functional Triple Modular Redundancy (FTMR).

MUXTREE Method [4]selects one of several analog or digital input signals and forward the selected input into a single line. In this system if a fault cannot be recovered at the molecular level, it can be recovered at cellular level. MUXTREE method offers better self- repairing and replication, but has only less fault coverage.

Self Healing System [5]-[7] is more closed to proposed approach. It consists of functional cell and spare cell. Spare cell replaces the faulty functional cell in the system. Each functional cell is surrounded by 2 spare cell and 2 router cells. Router cell mainly perform two functions; transfer output of functional cell to destination cell and transfer output of a spare cell to original destination cell. Therefore the system needs a complex communication for rerouting. This paper presents a new methodology to overcome these problems, thereby using endocrine cellular communication for self-repairing [1] in digital systems. The self-repairing digital system inspired by endocrine cellular communication improves the fault detection and also reduces hardware overhead for digital system design.

## III. PROPOSED SYSTEM

Self-repairing digital system becomes alternative for fault tolerant system [8].The proposed self-repairing digital system automatically detectsthe fault and correcting with high efficiency. It consists of structural layer and gene control layer. Each module is connected with 4 spare modules for replacing faulty working module at 4 times. Gene control layer controls the operation of modules. Gene control layer consist of Index Changing Unit (ICU), Differentiation Unit (DU). It determines the proper spare cell in the structural layer to replace the faulty cell without collision. This self-repairing mechanism is operated in parallel. So, even several faults occur in different modules at same time, the system can recover them.

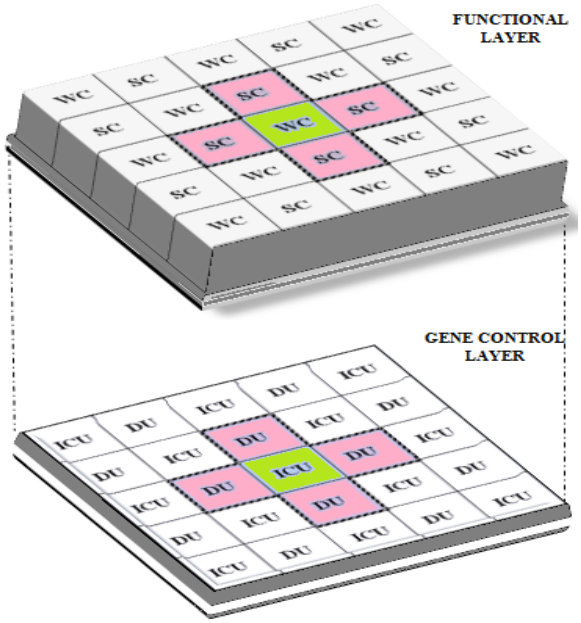


Fig. 2 Self Repairing Digital System

Fig.2 shows the proposed architecture for implementing self-repairing in digital systems based on the principles of the human immune system. Fault detection unit is mainly for detecting the fault and correcting it.

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A. *Gene Control Layer:*

A spare cell can be replaced by any of the four neighboring working cell in this self-repairing system. The gene control layer is placed in parallel with structural layer(functional layer). It composed of ICU and DU. Gene control layer controls the operation of cells in the structural layer. Every ICU is responsible for every WC and its four neighboring SC's. DU is assigned proper SC for fault recovery. When the fault occurred, it propagates to the ICU. ICU changes the SC's index bits and isolates the WC. Then DU in the SC differentiates the SC from the faulty WC. Every SC has index bit, which is in the gene control layer. Index bit shows the state of each cell in structural layer. There are three types of index bits. State bit: It shows the spare cell is available or not. Direction bit: It shows the direction of spare cell. Differentiation bit: It differentiate spare cell from WC.

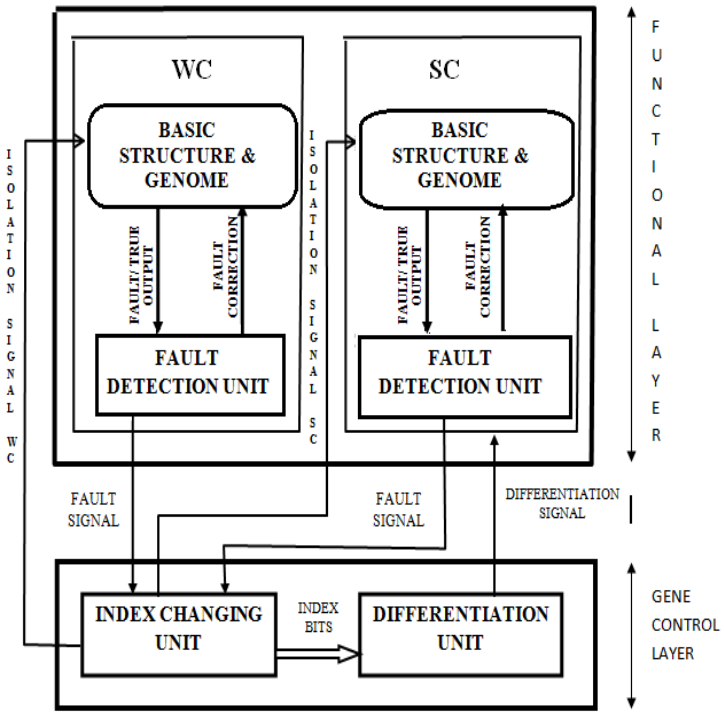


Fig. 3 Interaction Between Working Cell And Spare Cell

B. *Fault Detection Unit:*

The drawbacks of existing system are it requires large memory for fault detection and correction, and less functional fault recovery. Therefore proposed architecture uses elementary operational unit as shown in Fig 4. First up all the elementary unit produce bitwise fixed result corresponding to inputs of WC. Then this result is fed into comparator unit 1 and cross check the data whether it is true or fault output. Then a flag is set if there is any mismatch. Faulty data and its location can be found out by using comparator unit2. If it is a transient fault, then try to correct it using elementary unit and perfect genome and send corrected data to cell. If the fault appears simultaneously, even after fault correction and genome replacement, then it is a permanent fault.Transient faults are induced by temporary environmental conditions, such as cosmic rays and electromagnetic interference. Permanent faults are the result of irreversible device and circuit changes It is due to the fault in genome, the entire cell has to be replaced then set a fault signal and given to gene control layer.

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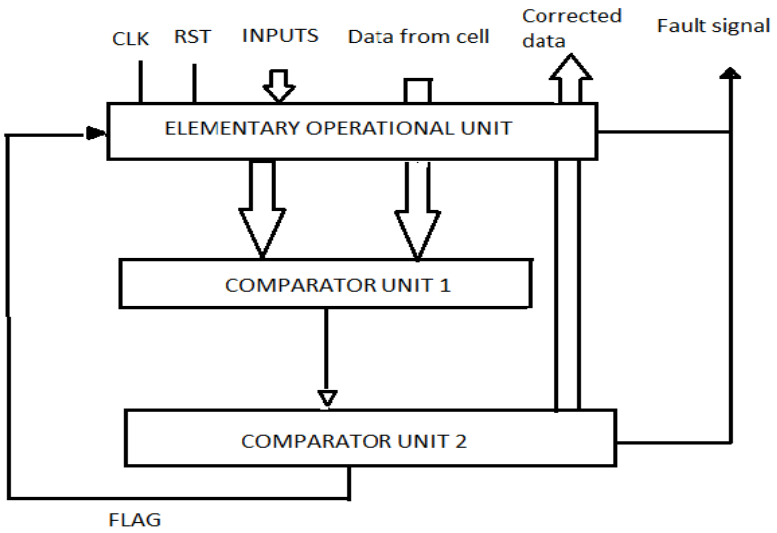


Fig. 4 Fault Detection Unit

C. *ICU And DU:*

ICU is responsible for changing the index bits in four neighbouring SCs of the WC. When all the spare cells corresponding to a working cell is used and there are no more spare cells for fault recovery, the system stops operating and moves on to system failure. Every spare cell has a DU that differentiates the spare cell referring to the differentiation bit and the direction bits. If the differentiation bit of the spare cell is changed to "1" while having the direction bits of "10," the spare cell is differentiated into a cell like the WC, which is located on the right side. After differentiation of the spare cell is over, the DU changes the differentiation bit. The entire process will be repeated if faults occur in any of the working cells.

Table 1. Index Changing Unit

| The condition for the change | | | | | state before fault | | | | | state after fault occurence | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Fault signal | | | | | state bit | | | | | differentiation bit | | direction bit | | | | | | | |
| W | LS | DS | RS | TS | W | LS | DS | RS | TS | W | LS | DS | RS | TS | W | LS | DS | RS | TS |
| 1 | | | | | | 0 | | | | | 1 | | | | | | | | |
| 1 | | | | | | 1 | 0 | | | | | 1 | | | | | 01 | | |
| | 1 | | | | | 1 | 0 | | | | | 1 | | | | | 01 | | |
| 1 | | | | | | 1 | 1 | 0 | | | | | 1 | | | | | 10 | |
| | 1 | | | | | 1 | 1 | 0 | | | | | 1 | | | | | 10 | |
| | | 1 | | | | 1 | 1 | 0 | | | | | 1 | | | | | 10 | |
| 1 | | | | | | 1 | 1 | 1 | 0 | | | | | 1 | | | | | 11 |

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## IV. SIMULATION AND IMPLEMENTATION RESULT

The simulation and the implementation results of the project is shown in this chapter. Xilinx ISE are the software used for the simulation. Xilinx ISE is a software tool produced by Xilinx for synthesis and analysis of HDL designs, which enables the developer to synthesize (compile) their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer. The proposed design is developed using Verilog and is embedded in a digital platform with an Xilinx Spartan 3E FPGA for the application of an ALU.

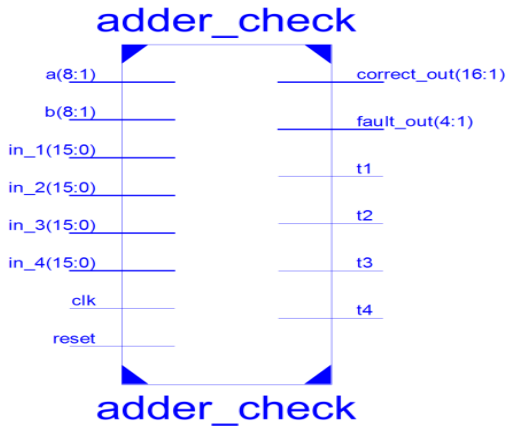


Fig. 5 Fault Detection And Correction Unit

Here the Fig.5 shows modified architecture of Fault detection and correction.By using this fault detection unit the memory usage of proposed fault tolerant digital system is less than existing self-repair. The Fig.6 shows thesimulation result of fault tolerant digital system.


Fig. 6 Simulation Result

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Here a working module is designed for four different operations like addition, subtraction, multiplication and shifting. The main aim of the proposed architecture is to reduce the area, memory usage, time delay and thereby increase scalability and accuracy. This scheme reduces hardware overhead and additional rerouting along with increasing size of the circuit. The entire architecture is divided in two layers and each layer has its own importance in maintaining the functions of the system even after fault recovery. This capability has made the system to operate in remote environments, such as outer space or deep sea.

## V. CONCLUSION AND FUTURE WORK

The fault tolerant digital system provides good scalability and fault coverage. New architecture for fault detection offers less memory usage and having good fault coverage. The exact control in the gene-control layer offers fault recovery without collision. This system simplifies the rerouting process without any additional hardware and minimizes unutilized resources. For further improvement of the proposed fault tolerant digital system, there remain several issues awaiting further studies. The primary goal of developing a fault tolerant goal is to develop self-repairing digital circuits using six stem cells.

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## BIOGRAPHY

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