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Design and Novel Approach for Ternary Decoder and Encoder Circuits

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ABSTRACT: At beginning era of digital design, the binary logic is used in all industrial applications. The binary logic uses 2 states i.e. 0's and 1's to represent each state. Since the binary logic uses 2 states, it requires more number of bits to represent a number. For example, the number 29 is represented in (11101)2 in this format. So this number 29 requires 5 bits to represent it. And also occupies more area and more power is required in designing the circuit. Therefore ternary logic is introduced. Here the ternary logic uses less number of bits to represent a number compare to binary logic. It also reduces the area and also the power of the circuit. The ternary logic uses 3 states i.e. 0,1,2 where logic 0 is considered as low state and logic 1 is considered as middle state and logic 2 is considered as high state. The same number 29 to represent in ternary logic requires 3 bits. i. e. It is represented as (1002)3 in ternary logic. Here In this Paper, the 2:9 Ternary Decoder and 9:2 Ternary Encoder is represented.

KEYWORDS: binary logic, ternary logic,ternary decoder,ternary encoder, digital design.

I. INTRODUCTION

The digital design has different kinds of number systems.it includes binary number system, octal number system, decimal number system, hexadecimal number system. Every number system has different kinds of radix indices. For example the radix of binary number system is 2.similarly the radix of ternary number system is 3. The radix of decimal number system and hexadecimal number system is 10 and 16 respectively[2]. Here the 2:9 ternary decoder and 9:2 ternary Encoder is represented. The decoder is a combinational circuit which converts binary number to a decimal number. Similarly, the Encoder is also a combinational circuit which converts decimal number to a binary number. The Ternary Decoder has n inputs and 3^n outputs and the Ternary encoder has 3^n inputs and n outputs. Here n=2 which means there are 2 inputs and 9 outputs. i.e. The 2:9 Ternary decoder has 2 inputs and 9 outputs. The inputs is a combination of 3 digits (0,1,2). The Ternary Decoder and Encoder Combinational circuit also helps in selection of memory cells in design of memory interfacing. Further, the ternary Decoder and Encoder is also helpful in advancement of Processors and controllers. Finally The Ternary Processor with Ternary Instruction set can be designed which is also a part in development of digital design.

II. METHODOLOGY

The truth table of 2:9 Ternary decoder is as shown in Table-1.
The 2:9 Decoder has 2 inputs and 9 outputs. The inputs are a,b which is a combination of 3 digits (0,1,2) and the outputs are represented by the variables P,Q,R,S,T,U,V,W,X.

a	b	P	Q	R	S	T	U	V	W	X
0	0	2	0	0	0	0	0	0	0	0
0	1	0	2	0	0	0	0	0	0	0
0	2	0	0	2	0	0	0	0	0	0
1	0	0	0	0	2	0	0	0	0	0
1	1	0	0	0	0	2	0	0	0	0
1	2	0	0	0	0	0	2	0	0	0
2	0	0	0	0	0	0	0	2	0	0
2	1	0	0	0	0	0	0	0	2	0
2	2	0	0	0	0	0	0	0	0	2

Table-1 Truth table of 2:9 Decoder

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Here the inputs a, b is having 9 input combinations and 9 outputs. The outputs will be high whenever the corresponding inputs are activated. For example, when input combination (0,0) occurs, the Output P becomes high. Similarly when the input combination (2,2) occurs, the output X becomes high.

Switch Diagram of 2:9 Decoder

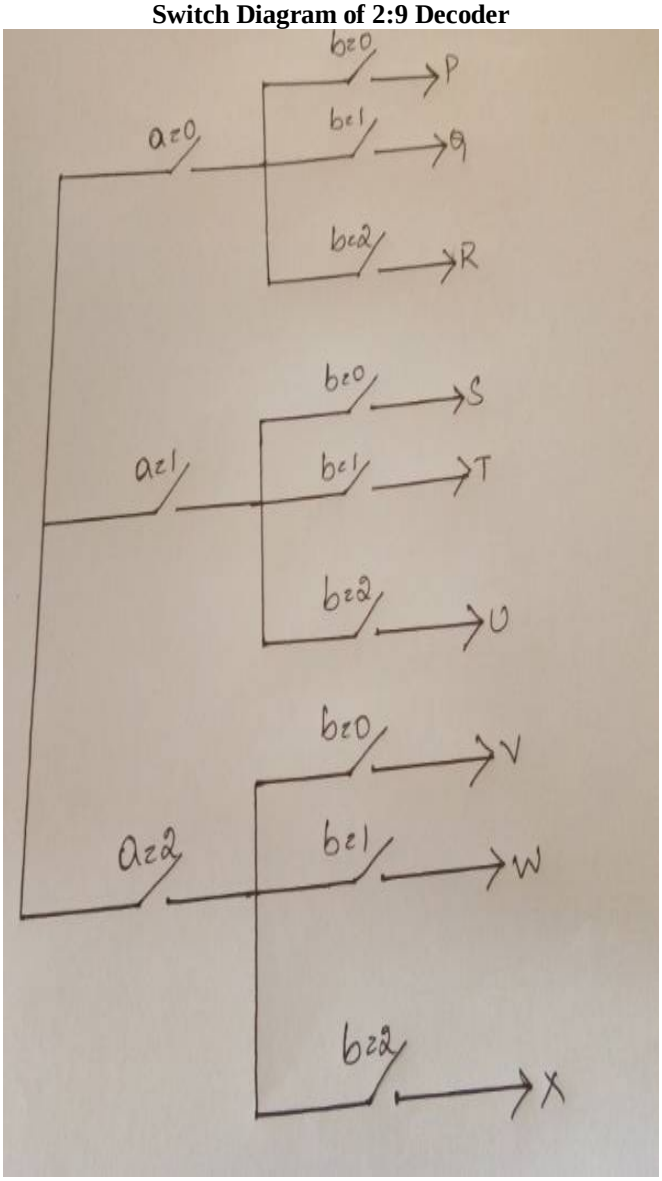

Fig-1 Switch diagram of ternary decoder

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The truth table of 9:2 Ternary Encoder is as shown in Table-2. Here, The Ternary encoder has 9 inputs represented as P,Q,R,S,T,U,V,W,X and 2 outputs as a,b.

P	Q	R	S	T	U	V	W	X	a	b
2	0	0	0	0	0	0	0	0	0	0
0	2	0	0	0	0	0	0	0	0	1
0	0	2	0	0	0	0	0	0	0	2
0	0	0	2	0	0	0	0	0	1	0
0	0	0	0	2	0	0	0	0	1	1
0	0	0	0	0	2	0	0	0	1	2
0	0	0	0	0	0	2	0	0	2	0
0	0	0	0	0	0	0	2	0	2	1
0	0	0	0	0	0	0	0	2	2	2

Table-2 Truth table 9:2 Encoder

Here the outputs a, b is having 9 combinations i.e. 9 outputs. The outputs will be indicating corresponding decimal number whenever the corresponding inputs are activated. For example, when input U becomes high, the Output combination will be (1, 2) which represents the decimal number 5. Similarly when the input combination X becomes high, the output combination will be (2,2) which represents the decimal number 7.

Switch Diagram of 9:2 Ternary Encoder

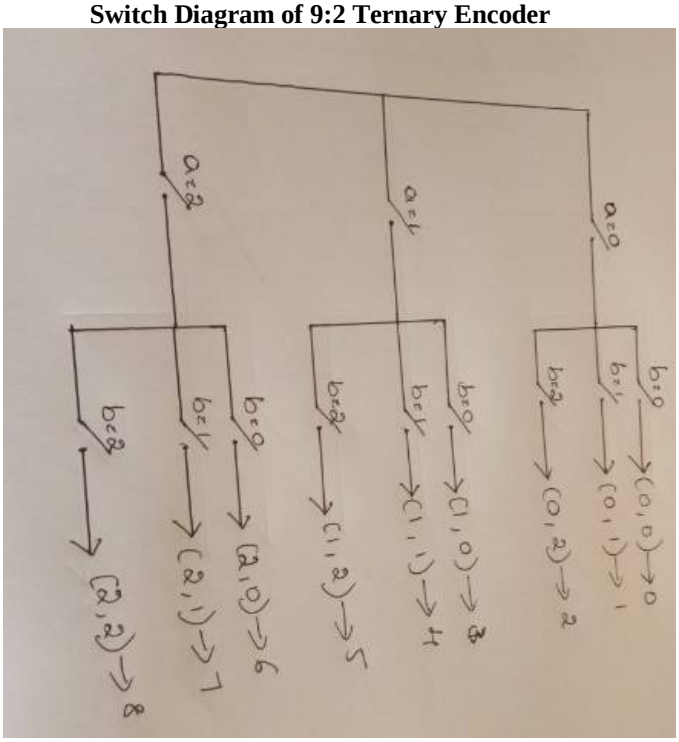

Fig-2 Switch diagram of ternary encoder

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III. CONCLUSION

The Switch diagram of 2:9 Decoder and 9:2 Encoder indicates that it consumes less area and less power in designing of circuit. The Switch diagram of 2:9 Decoder has 2 inputs and 9 outputs. Each input is having 3 different possibilities (0, 1, 2). Similarly, the Switch diagram 9:2 Encoder has 9 inputs and 2 outputs. Further, the Ternary Decoder can be extended 3:27 Decoder and 4:81 Decoder. Similarly Encoder can also be extended to 27:3 Encoder and 81:4 Encoder. The Ternary Decoder and Ternary Encoder also helps in the development of processors and controllers. Finally the Ternary Decoder and Encoder is helpful in advancement of Digital design.

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