ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijircce.com

Vol. 5, Issue 5, May 2017

Review on Configurable and Low-Power Mixed Signal SOC for Portable ECG Monitoring Applications

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ABSTRACT: This paper describes a mixed-signal ECG System-on-Chip (SoC) that is capable of implementing configurable functionality with low-power utilization for convenient ECG moni-toring applications. ECG works generally by detecting and amplifying the modest potential changes on the hand that are caused when the electrical signal in the heart muscle is charged and spread during each heartbeat. Achieving reliable and high integrity recording however remains a challenge, especially under daily-life activities. In this paper we introduced a system approach to motion artifact reduction in ambulatory recordings. A low-voltage and high performance analog front-end extracts 3-channel ECG signals and single channel electrode-tissue-impedance (ETI) measurement with high signal quality. This can be utilized to assess the quality of the ECG measurement and to filter motion artifacts. A custom digital signal processor consisting of 4-way SIMD processor gives the configurability and advanced functionality like motion artifact removal and R peak detection. Analog to Digital Converter (ADC) is capable of adaptive sampling achieving a compression ratio of up to 7, and loop buffer integration decreases the power consumption for on-chip memory access. The SoC is implemented in 0.18 m CMOS process and expends 32 W from a 1.2 V while heart beat detection application is running, and integrated in a wireless ECG monitoring system with Bluetooth protocol. Thanks to the ECG SoC, the overall system power consumption can be reduced significantly.

KEYWORDS: Bio potential recording, ECG, motion artefact reduction, R peak detection, System-on-Chip (SoC).

I. INTRODUCTION

The expanding utilization of ambulatory monitoring system, not only continuous signal collection and low-power utilization, additionally brilliance with robust operation under the patients' every day routine is required. The objective is emerging to enable configurability for various applications, ranging from simple heart rate calculation towards more complex medical diagnostics under ambulatory conditions, with extreme low power utilization and high precision (Fig. 1). Especially, one of the major problems in ambulatory ECG monitoring system is the presence of motion artefact's, which prompt to poor signal quality, and potentially wrong clinical diagnosis. High signal integrity recording quality and robust operation under the presence of signal artifacts will allow a higher level of physical activity for the subjects. In order to address this challenge, local data processing with advanced functionalities is required, such as motion ancient rarity decrease and accurate feature detection.

Wearable and wireless devices allow delocalizing ECG checking from hospitals to home environments. Accomplishing reliable and high integrity recording however remains a challenge in ambulatory conditions because of the high level of noise introduced by motion artifacts. For Holter systems, motion artifacts often lead to difficult interpretation of ECG signals, and the output of the device must be discarded. For event recorders or detection devices, recognizing curios for the great operation of the device. The proposed mixed-signal SoC consists of an AFE that supports continuous and simultaneous monitoring of 3-channel ECG monitoring, with electrode-tissue-impedance (ETI) measurement and band-power (BP) extraction for extracting signal fluctuations in the specified frequency band, with sampling rate of 512-sample/sec and 64-sample/sec, respectively. A 12-bit successive approximation (SAR)

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analog-to-digital converter (ADC) with adaptive sampling scheme is capable of compressing the ECG data by a factor of 7 before digital signal processing, which in turn reduces the processing power of the DSP and the wireless information transmission [1].

The custom DSP back-end, utilizing SIMD processor architecture, hardwired accelerate unit, effective duty cycling, on-chip memory reduction schemes, and clock gating, gives low power operation while performing multichannel ECG processing. Further, because of the high integration level, a small form-factor can be accomplished with negligible utilization of external components enabling to reduce the system complexity. This paper is organized as follows. In Section III, we describe the target application of ECG monitoring. Section IV and V describe the details of analog front end and digital back end architecture, respectively, section VI and VII gives the details of on-chip memory power reduction and ECG monitoring system integration followed by conclusion in Section VIII.

II. LITERATURE SURVEY

Ambulatory monitoring of ECG signals can be compromised by motion artifacts. Change of electrode-tissue impedance may be utilized to monitor the presence of such motion artifacts. In any case, challenge arises from the requirement of measuring the impedance without disturbing the ECG signal in a low-power manner. The electrode-tissue interface is stimulated with two AC currents at frequency, f(0°), being equivalent to 1kHz. Any DC component of this stimulation current aggravates the motion artifact signal. The resulting AC voltage over the electrode-tissue interface is only demodulated by the CT impedance monitoring channels. This enables the separation of ECG and impedance signals in the frequency domain by utilizing a low-pass filter. In this manner, signal band-power, ECG signal, and electrode-tissue impedance can be checked simultaneously with low-power dissipation. The output is amplified and compared against a threshold voltage detecting the presence of high-frequency activity during which the sampling rate of the ADC is increased from 64Hz to 1024Hz. This esteem can be adapted based on the heart rate considering the possible presence of high frequency artifacts[1].

It consists of three stages: a preprocessing stage, a processing stage, and a classification stage. The digitized ECG is applied at the input to the preprocessing stage. The preprocessing stage uses a filtering unit to filter out the artifact signals from the ECG signal. These signals include baseline wander, power line interference, and high-frequency noise. The processing stage consists of heartbeat detection and feature extraction modules. The heartbeat detection module attempts to locate all heartbeats. The feature extraction modules are required because, although it is possible for the classification stage to process the ECG samples directly, greater classification performance is often achieved if a smaller number of discriminating features (than the number of ECG samples) are initially removed from the ECG[2]. The ECG preprocessing module is the main component of the wireless ECG monitoring system. Its functionality permits the total system power utilization to be essentially lessened compared to conventional ECG acquisition systems. The analog ECG preprocessing ASIC simultaneously amplifies the ECG signal, extracts the power components of the signal within the frequency band of interest for detection of the QRS complex, and furthermore gives a continuous measurement of the electrode-skin impedance. The built-in analog-to-digital converter (ADC) performs adaptive sampling on the ECG signal, whereby the regions with rapidly changing signal (e.g. the QRS complex) are sampled at 1024Hz to allow optimal time resolution for the R peak search, while the moderate parts of the signal are sampled at 64Hz[3]. Numerous techniques for noise reduction and motion artifact removal have been proposed in literature. This is especially valuable when the noise is non-stationary, like in the case of ambulatory motion artifacts. However, a reference signal has to be additionally recorded together with the ECG. Previous solutions using a general purpose processor have restricted functionality [4], limited programmability [4], or can't achieve very low power utilization [5]. Though, the processors [6], [7] are executed to optimize the biomedical signal processing, they include only the digital processor, so require the external sensor module for biopotential signal acquisition [8], [9].

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III. TARGET APPLICATION ANALYSIS

The propelled usefulness such as signal filtering, ECG feature extraction, analysis, and motion artifact suppression typically required for the monitoring system. In any case, the ambulatory systems have exceptionally strict requirements in terms of power consumption, signal quality, system complexity, and small form-factor. To meet these necessities, hardware optimization should be accomplished on the characteristics of the target application.

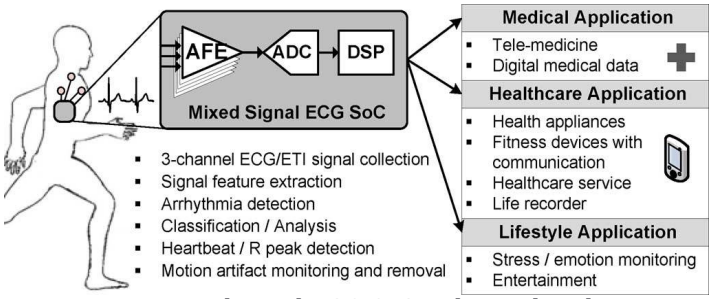
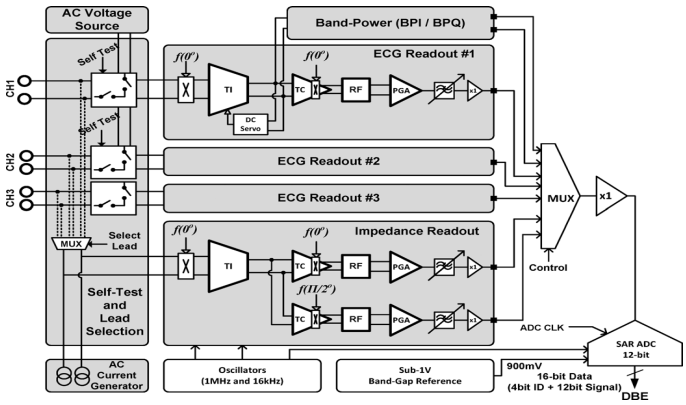


Fig.1 Mixed-signal ECG SoC and typical applications.



A. Motion Artifact Reduction

Many motion artifact decrease algorithms were presented, and the conventional algorithms can be classified into two major groups, the adaptive filtering [11] and the blind source separation method (BSS). Thanks to the completely integrated ASIC, the ECG SoC can give both methods as indicated by the need. Adaptive filtering, such as Least Mean Square (LMS) and Recursive Least Squares (RLS), should act optimally while tracking the non-stationary changes in signal and noise [11], [10]. Adaptive filtering algorithms can be implemented with single channel input. However, in order to accomplish high filtering performance, a reference signal having a good correlation with the noise has to be accessible to estimate the noise characteristics.

In this work, the electrode-tissue impedance (ETI) signal, which has high correlation with the motion artifact, is presented for the reference signal. The ETI signal can be recorded consistently together with ECG signal by sharing the electrode, so that the external device is not important to be coordinated on the system. Principal Component Analysis (PCA) and Independent Component Analysis (ICA) are generally utilized algorithms for the BSS technique, which requires linearly independent multi-channel ECG recordings to separate the parameter constructing of eigenvector matrix. The ECG SoC gives synchronous recording of the three ECG channels, and they are processed with several seconds window to reflect the environment perturbation. BSS method has been well known to achieve the good performance for motion artifacts reduction. PCA is chosen because of its moderately low computational complexity compared to ICA.

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B. Feature Extraction

The feature extraction and the heartbeat classification have been presented, which are the most fundamental devices for the analysis of an ECG signal. The feature extraction is researched by ECG morphology, heartbeat interval features, derivative-based methods [12], band-power extraction method, and frequencybased methods. The accuracy of R peak detection is crucial for reliable analysis, because the R peak contains the primary parameter for arrhythmia examination like the determination of RR interval and heart-rate-variability (HRV). In this paper, the R peak detection algorithm based on the continuous wavelet transform (CWT) is chosen to give the best execution. The CWT-based technique accomplishes the accurate peak detection with a positive predictive value (+P) of 99.8%. Though the CWT-based algorithm gives a high accuracy performance, it is a moderately computationally intensive algorithm because of the repeated convolution operation over all samples.

IV. ANALOG FRONT END

Fig. 2 demonstrates the architecture of the analog front end (AFE). Each readout channel includes a low-noise and low-power instrumentation amplifier (IA), a ripple filter (RF), a programmable gain amplifier (PGA), and a programmable low-pass filter. The IA is a chopper stabilized current balancing IA redesigned for operation from a 1.2 V supply. The fundamental advantage of this type of IAs is that the common-mode rejection ratio (CMRR) doesn't depend on coordinating of passives, and can give a CMRR in excess of 100 dB. In addition, the AFE also incorporates a built-in self-test and lead selection block. During the self-test mode, the input leads are connected to a differential on-chip voltage source. This enables the direct measurement of the channel gain and gain matching even during remote monitoring applications. In addition to these main functional blocks, all the supporting building blocks have been implemented in the ECG SoC so that the ASIC can be utilized within a system with a negligible number of external components.

A. Instrumentation Amplifier

Fig. 3(a) shows the architecture of Instrumentation Amplifier. An external floating high pass filter is given for suppression of differential DC-signals because of electrode polarization. This filter does not suppress common-mode DC signals. So the common mode input range of the IA is intended to be adequately large of 300 mV range. The IA itself is a continuation of the previous generation IA, which is a chopper-stabilized current-balancing IA architecture. The complete IA operates within choppers, clocked at 2 kHz to reduce the amplifier 1/f noise. A DC-servo, like to the one utilized as part of [13] is included which operates within the choppers and effectively realizes a high-pass filter for the offset of the Trans conductance stage (TC) block as well as the chopper-induced offsets.

The IA consists of a trans conductance stage (TC) and a trans impedance (TI) output stage. The TC output current can be copied to multiple TI outputs stages, which is valuable in the alternate channels, for example, ETI and BP extraction channels to decrease the power utilization. The main benefit of the proposed IA architecture is the way that the input signal sees a gate, which is inherently very high input impedance, and that the amplifier CMRR doesn't rely on matching of passives. The TC stage is basically a flipped voltage follower structure.

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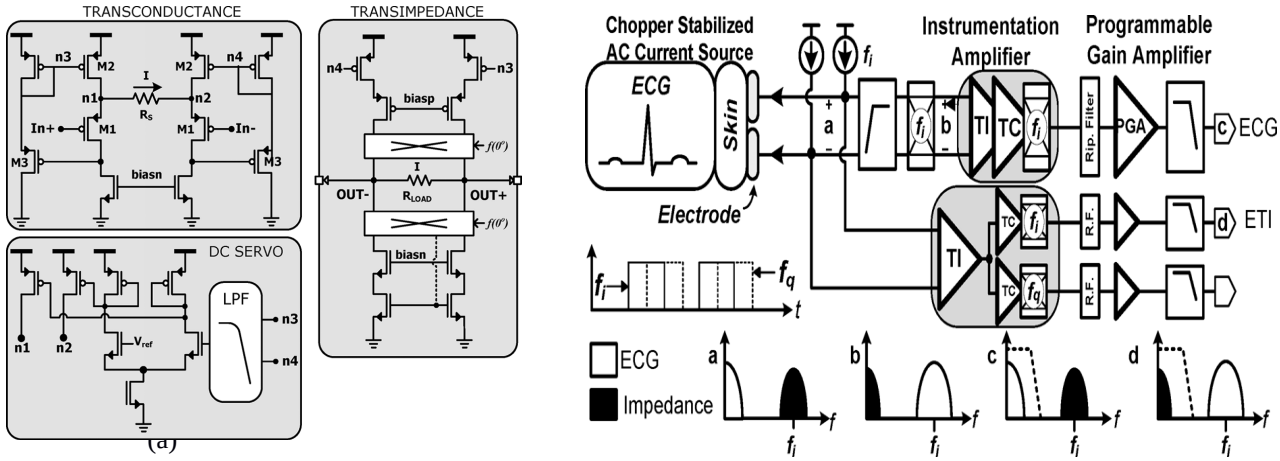

Fig. 3Architecture of the instrumentation amplifier (IA) (b) Continuous electrode tissue impedance (ETI) monitoring circuit

B. Electrical-Tissue Impedance Monitoring

Fig. 3(b) demonstrates the design of the impedance measurement circuit for consistent and simultaneous ETI condition monitoring with the ECG signal. The channel consists of a chopper stabilized IA, a ripple filter and a PGA. Chopper modulation is a power efficient solution for modulating analog signals and shifting their frequency spectrum to a desired frequency with low power consumption. The proposed arrangement utilizes chopper modulation to separate the frequency bands of the ETI signal and ECG signal. Lowering the impedance measurement frequency has advantages in terms of evaluating the capacitive part of the electrode impedance, since the impedance of the capacitive part decreases with increasing frequency. An important design criterion is to successfully isolate the ECG signals and impedance monitoring signals, so that each estimation doesn't influence the other, limiting the crosstalk.

V. DIGITAL SIGNAL PROCESSING BACK -END

In advanced digital signal processor back-end (DBE), which performs user application programs. Like the AFE, the DBE also works from a 1.2 V supply with a 1 MHz system clock generated by on-chip ring oscillator. The DBE consists of a pre-processing unit, 4-way SIMD, on-chip SRAM for data and program memory, clock management unit, timer, AES-128 accelerator, and several peripheral components. Moreover, there are three SPI blocks for getting the on chip memory, interfacing with ADC interface, and supporting the external device connections, respectively. JTAG and GPIOs are integrated for ongoing troubleshooting. 46 kB SRAM is incorporated for on-chip information and program memory (PMEM). An information memory (DMEM) comprising of 4 banks can be accessed both by vector and scalar units through the memory judge square, and a coefficient memory (CMEM) is incorporated to enhance the convolution for parallel information stacking. DMA, three SPIs, and processor memory interface are interconnected by a mutual transport with need coding to maintain a strategic distance from the memory get to blockage.

The pre-processing performs the essential requirement functions before sending data to the main processor. Since the pre-processing should handle ECG input stream in real-time and repeatedly to the every sample, the unit is composed with the dedicated hardware to achieve high throughput. A direct memory access (DMA) controller supports the sampled data to be written continually into the input buffer in the data memory without interrupting the processor, even when the processor is in sleep mode or running mode with other tasks. 8 DMA channels are prepared for all the input channels from AFE and external device, and each channel can be separately configurable by programming. In order to accomplish low power utilization, the power management is adequately employed. Each channel in AFE has separated power domain, so that only necessary channel can be turned on according to the user application.

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VI. ON -CHIP MEMORY POWER REDUCTION

A large memory capacity brings not only increase of the area occupation, as well as increase of the get and leakage power consumption. Fig. 4(a) demonstrates the power break from the power simulation when R peak detection algorithm is performed with continuous sampling rate of 512 S/s, and the total power consumption is 71µ W. According to the pie chart, we can see that the power utilization for processing and data/program memory getting are dominated. Therefore, well optimized memory architecture helps diminishing the system power essentially. In this work, further on-chip memory power lessening is exploited on both of data memory and program memory.

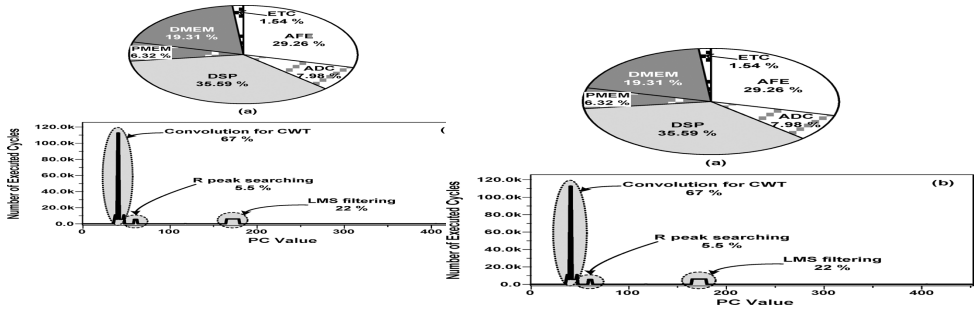

Fig. a. Analysis of a mixed signal ECG processing platform simulation when CWT-based R peak detection and LMS filtering algorithms are running. (a) Power breakdown of the system. (b) Profiling of the number of execution cycle per program counter (PC).

VII. ECG MONITORING SYSTEM INTEGRATION

A wireless ECG patch has been produced using the ECG SoC to perform streaming ECG monitoring with real-time motion artifact decrease and arrhythmia detection (Fig. 5). The system consists of ECG SoC, low energy bluethoothSoC (BLE), a 3-axial accelerometer for activity monitoring, and a MicroSD card for information logging, and disposable ECG electrodes. The ECG SoC monitors concurrent 3-channel ECG signal and performs the required application, such as motion artifacts reduction and the R peak detection algorithm. The information is processed and analyzed locally, and relevant events and information is wirelessly transmitted in real time and/or stored on a micro SD card. Due to the Bluetooth chip, the system provides connection to PCs and mobile phones through a standard protocol, and maintains very low power consumption for long-term monitoring in home environment.

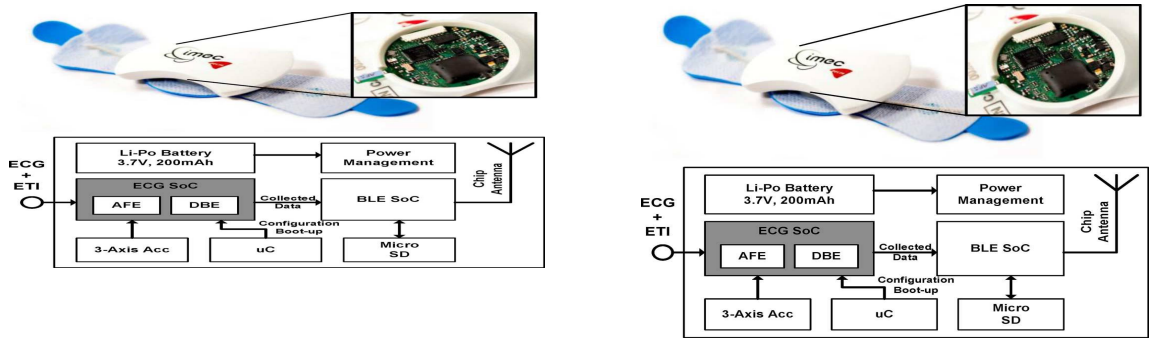

Fig. 5. Photograph and its architecture of the wireless ECG monitoringsystem utilizing the ECG SoC.

In order to demonstrate the benefits of the ECG SoC on the system power consumption, three different operation modes have been implemented. The first two modes are streaming data transmission mode. The raw ECG signal and impedance signals are collected at 512 Hz and transmitted without local processing but down sampling with 256 Hz in digital domain.

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And the second data transmission mode performs a small local processing with only LMS-based motion artifact removal algorithm, and transmit the filtered ECG with 256 Hz sampling rate. Then again, in the last mode, the system utilizes full local processing of accurate R peak search mode with the LMS-based motion artifact removal and CWT-based heart beat detection algorithm using the ECG SoC and transmits only the heart beat rate periodically, once a second (1 Hz). In general, since the most power consuming part is the radio, the last approach, which is as much data processing as possible before transmission, is a proficient technique method to diminish the total system power utilizes.

VIII. CONCLUSION

This paper presented a mixed-signal ECG SoC, with incorporated analog front-end and DSP back-end. The AFE supports concurrent 3-channel ECG monitoring, with impedance measurement and band-power extraction. The custom digital signal processor consisting of a 4-way SIMD processor provides configurability for a wide range of application and advanced functionality like motion artifact removal, accurate R peak detection algorithm, arrhythmia classification and HRV analysis. Various algorithms are possible, allowing different power-performance trade-offs depending on the application requirements. An adaptive sampling ADC significantly reduces the equivalent data-rate of the ADC output without affecting the information content of the input signal, leading to a reduction of data memory access and processing complexity in the DSP domain. The loop buffer integration enables decrease in the access power of the program memory. The presented SoC consumes a best-in-class power consumption of only 31.1 W from a 1.2 V supply in beat detection mode. The SoC has been integrated in a wireless ECG monitoring system with Bluetooth protocol. This paper proposes a comprehensive approach to the problem of motion artifact reduction in ambulatory ECG recordings.

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