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Review on Network on Chip (NoC) Router Design

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ABSTRACT: Number of processing elements on single chip called system on chip (SoC). As the traditional system on chip having bus based communication, with increasing processing elements on chip form very complicated structure of SoC. To reduce this complexity Network on chip (NoC) is best , it provides high level of parallelism in communication and improves the performance of on chip communication. Router is the central device of NoC which is required to obtain the efficient on chip communication. This paper reviews NoC router and NoC parameters which affects the router design.

KEYWORDS: system on chip, network on chip, topology

I. INTRODUCTION

Number of processing elements are increased continuously on bus base system on chip, they face design challenges and complexity increases. This system on chip is not scalable for a complex system , In system on chip data flow limited by resourses, results in slow communication occur.This bus base design needs to be replace with latest network architecture called network on chip. Network on Chip (NoC) is a new paradigm to make the interconnections inside a System on Chip (SoC) system. It reduces complexity of designing wires and also increases speed and reliability [1]. It is able to address the increasing interconnect complexity challenges[5]. It improves scalability of SoC and power efficiency of complex SoC. To carry on chip communication router play important role, it is use to route the incoming data towards the destination , and design of router is one of the the most important factor that impact on network performance.

II. LITERTATURE SURVEY

Router are used on network for directing the data from source to destination, author design router to increases the performance of NoC, author gives the impact of FSM controller used in router design so every channel get chance to transfer data also utilizing the buffer at both sides congestion get reduce and performance increased[1]. In this paper author design 5 port router with simple decoding logic, design of router consist components buffering registers, demultiplexer, First In First Out buffer, and schedulers. The scheduler base on round robin algorithm[2]. Paper[3] Shows the work on NoC router which is efficient in terms of area and power, router consist 2 types of crossbar as multiplexer and try state buffer ,44% area increased in 32 bit-try state buf design and as compare to multiplexer design and 61% less power required for multiplexer design so router design with multiplexer type of crossbar provide improvement in area and power than matrix buffer router design. Storage space required to store the incoming data at router, buffering done at input side (Input buffer router) or output side (Output buffer router) or both side of router. Router proposed in [4] paper is distributed shared buffer router, it contain 2 stage of crossbar switches in between two crossbar switches memory place, It indicated significant improvement in performance. This router architecture achieves higher throughput and latency get reduce. In [5] Author propose router with two adaptive routing, fully adaptive and proximity congestion awareness, combine this two routing techniques is effective in terms of latency and throughput, this router supports fast parallel routing arbitration it consist routing decision and arbitration in one stage.

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III. OVERVIEW OF NOC PARAMETER

Design of NoC router also depends on network topology, flow of data and routing path. Overview of such parameters is given bellow

A. *Topology*:

Topology is the interconnection of network, overview of some topology

1. Mesh:

Mesh shape network consists m columns and n rows and at each intersection router is situated and this router is connected to the adjacent router, it is simple type of topology and easy to implement. Position of router in 3X3 mesh architecture for NoC is as shown in fig.1.

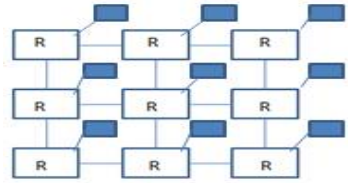

Fig.1.Mesh network (R Router)

2. Torus :

Torus network is same as mesh, each node is connected to the nearest neighbors, But in torus network all end node are also connected together. Torus network has better path diversity than mesh network[6], it has minimal routes to transfer data from source to destination. Fig 2 shows torus architecture for NoC and position of router in torus network.

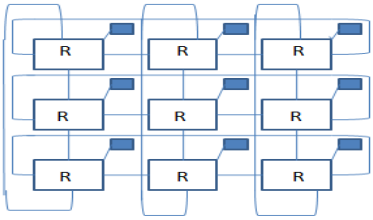

Fig.2. Torus network

Torus topology takes less time as compare to mesh topology to reach destination [7].

3. Polygon:

The polygon network is a circular network, where packets travel circularly from one router to other. When chords added to circle to connect all possible router form different network and only if opposite routers connect then structure of network is called spidergon[6]. Architecture of polygon network with all chords is as shown in Fig. 3 and position of router in network.

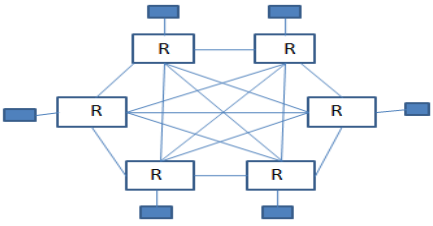

Fig.3. polygon network

4. Butterfly flat tree:

In tree network, router is present at the node of tree and computational resources is at the leaves of tree[6], butterfly flat tree network is also same as tree network, in this butterfly flat tree network hierarchy is maintain, upper nodes

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are connected to the lower nodes in hierarchy and level of it depends on the number of IP [8]. fig.4 shows the butterfly flat tree network.

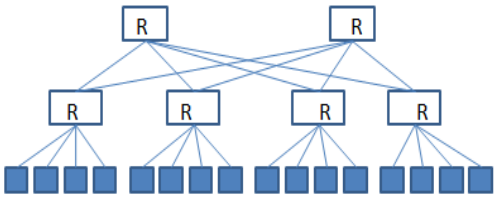

Fig.4. Butterfly network

5. Star:

A star network consist router in the middle position of the star, this router having large capacity, and other computational resources or sub networks in the spikes of the star. Traffic between the all spikes goes through the central router and because of this capacity requirements of the central router are quite large. Traffic between the all spikes goes through the central router causes a possibility of congestion in the middle of the star[6]. Star architecture of NoC is as shown in fig.5 it consist router at middle position.

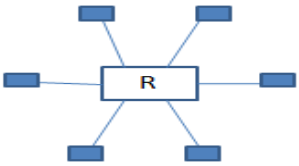

Fig.5. Star network

B. Switching techniques:

Switching technique is important parameter of NoC . It determines the flow of data through routers in the network. Circuit switching and packet switching are two type of switching techniques, In circuit switching path is reserved in between source and destination and data travel along this path, In packet switching method does not reserve path like circuit switching, each data packet travel independently[1]. Packet switching further classified as follows:

1. Store and forward :

In this method entire packet store in the router buffer before it forward to the next router, so the buffer space required for router is large, and at every hope wait to receive entire packet then it forward towards next.

2. Virtual cut through:

In virtual cut through switching techniques packet forwards to next router as soon as the next router gives permission, when it having sufficient space to store the packet this switching techniques also required large storage space[6].

3. Wormhole:

In this switching techniques packet is divided in to small and equal size of flit. 1st header flit transfer, it contain routing information, then all flit follows the same path. Hence no packet reordering required at destination. Buffer space required for router is small but the disadvantage is if 1st flit block whole packet get block [9].

C. Routing algorithms:

Routing algorithm decides the path for data transfer from source to destination. There are many ways to classify routing in NoC.

- Deterministic routing
- Adaptive routing

In deterministic routing technique the routing path from the source to destination is determined in advance, by the source and the destination addresses. In adaptive routing, several paths from the source to the destination are possible. The output port selection depends upon the network conditions such as congestion and link faults. When a packet comes at router, header of packet having destination address and accordingly the routing function computes all possible output ports where this packet can be forwarded to. Then a routing function selects one of the proper output ports to forward.[10].

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Description of some routing algorithm:

1. XY routing algorithm:

In 2-D mesh topology NoC, each router having identity by its coordinate (X,Y). If (Xc,Yc) current router address and (Xd,Yd) destination router address. In XY routing algorithm compares the current router address (Xc,Yc) to the destination router address (Xd,Yd) of the packet, stored in the header flit of packet. Packet routed to the core port of the router when the address of the current router (Xc,Yc) is equal to the (Xd, Yd) destination address. If source and destination address not equal then first compared Xd address with Xc (horizontal) address and packet will be routed to the East port when Xc<Xd, to West when Xc>Xd. If Xc=Xd then, vertical address copaired. Packet will be routed to South when Yc<Yd, to North when Yc>Yd. If header flit block all flits packet will be block [11].

2. Surrounding XY Routing:

In surrounding XY routing, it works as simple as basic XY routing, routes packets first along x-axis and then along y-axis. This simple xy-routing works up to good network condition and routing does not meet inactive router. In this routing routs the packets vertically when the router's left or right neighbor is inactive and routs the packets horizontally when the router's upper or lower t neighbor is inactive [6].

3. DyXY routing:

DyXY routing is depending on the network condition, the rout computation unit may select different paths at different times for the same source and destination pair[12].

4. OE routing algorithm:

OE routing is distributed adaptive routing algorithm which is base on odd even turn model [13]. In 2 dimensional mesh each node having identity by it's co-ordinates (X,Y), In this model column called even when X is even value and odd if it is odd value ,and turn of 90 degree involve for change direction, so EN,WS,WN,SE,SW,NE,NW this tern are possible .E,N,W,S , is east ,north, west, south respectively.

Two strict criteria for odd-even turn model [13].

1) At even column: No turns of East to North, East to South are allowed

2) At odd column : No turns of North to West, South to West are allowed.

IV. CONCLUSION

In these paper we studied various NoC router architecture, and also studied various NoC parameters which affects router design.

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