ISSN(Online): 2320-9801
ISSN (Print) : 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijircce.com

Vol. 7, Issue 1, January 2019

Design and Analysis of a Conventional Wallace Multiplier in 180nm CMOS Technology

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ABSTRACT: Multiplier is an arithmetic circuit that is extensively used in DSP, microprocessors and communication applications like, FFT, Digital Filters etc. Today entire world is demanding compact and small digital devices which should perform fast with low power consumption. Multiplier is the basic building block in almost all digital devices and it impacts the speed, power and area of a device significantly. Thus it is important to design an efficient multiplier which should perform fast with low power consumption. Optimizing actual delay, power and area of a multiplier is a major design issues, as area and speed are usually conflicting constraints.

I. INTRODUCTION

With expeditious development of VLSI applications such as DSP, image, video processing and microprocessors extensively use logic gates and arithmetic circuits. Because of powered by batteries, the supply voltage is often limited, and the life time of the battery is of great importance for these devices
In low-voltage environments, the transistor characteristics also degrade and some circuit techniques can no longer be used, thus the low-voltage design is different from the traditional circuit design technique. Gate Diffusion input (GDI) a new technique of designing low-power digital combinational circuit. This technique allows reduction in power consumption, transistor count, propagation delay and area of digital circuits.

MOTIVATION

The core of any kind of processor is its data path. Data path is the one of the crucial component that decides the key parameters such as the clock frequency, area and power dissipation of the design. Adders and multipliers are the main components in the data path and high performance systems such as FIR filters, microprocessors, digital signal processors, etc. A system's performance is generally determined by the performance of the multiplier because the multiplier is generally the slowest clement in the system. Furthermore, it is generally the most area consuming. Hence, optimizing the speed and area of the multiplier is a major design issue. However, area and speed are usually conflicting constraints so that improving speed results mostly in larger areas.

II. BASICS OF MULTIPLIERS

Multiplication is an operation that occurs frequently in digital signal processing and many other applications. However, multipliers occupy a much larger area and incur much longer delays than adders. Therefore it is imperative that special techniques be used to speed up the calculation of the product while maintaining a reasonable area.
The product is the result of multiplying the multiplicand to the multiplier. The multiplication operation is performed in two main steps. First is the partial product formation, which consists of AND-ing each bit of the multiplier with the multiplicand. Each successive partial product belongs one place to the left of the previous partial product. The second step is partial product accumulation, where the partial products are combined to form the result.

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Application of Multipliers

- Used in digital signal processing operations such as filtering, convolution and analysis of frequency.
- Image processing.
- Arithmetic units in Microprocessors.
- Used in graphics and computation system.
- Cryptosystems

Wallace/ Dadda Multiplier

The speed of multiplier is depends on the total time taken for summation of partial products. Scientist C. S. Wallace introduced an effective way of summing the partial product bits in parallel using a tree of Carry Save Adders which generally known as the "Wallace Tree" [39].

Wallace trees are irregular in the sense that the informal description does not specify a systematic method for the compressor interconnections. However, it is an efficient implementation of adding partial products in parallel.

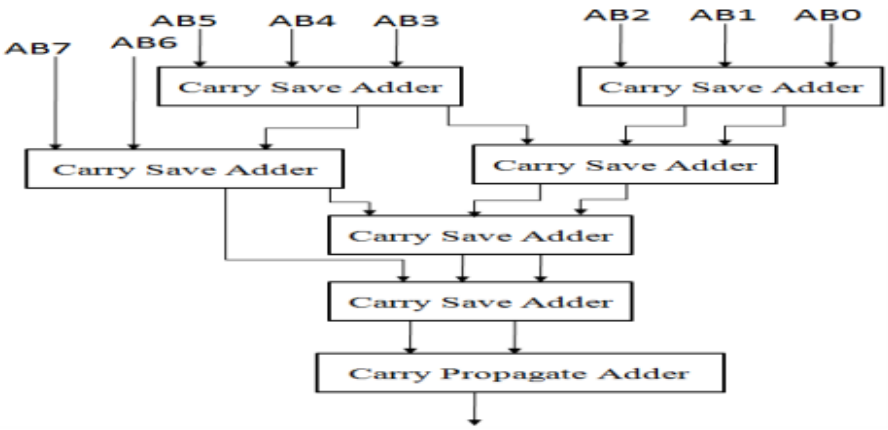

Fig 1: Wallace multiplier

2-BIT MULTIPLIER

In 2 × 2 bit multiplier, the multiplicand has 2 bits each and the result of multiplication is of 4 bits. Hardware realization of 2 x 2 multiplier is shown in fig 4.15.

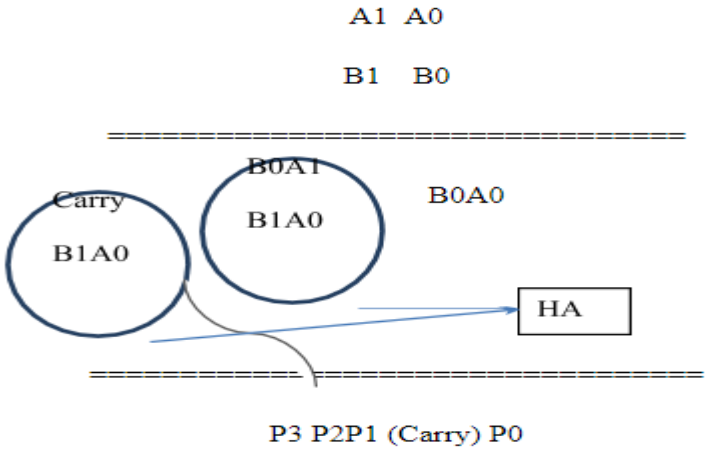

Fig 2: Hardware Implementation of 2-bit Multiplier

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Schematic diagram of 2-bit multiplier is shown in fig using Wallace tree method shown above. P0, P1, P3 and P4 are the partial products.

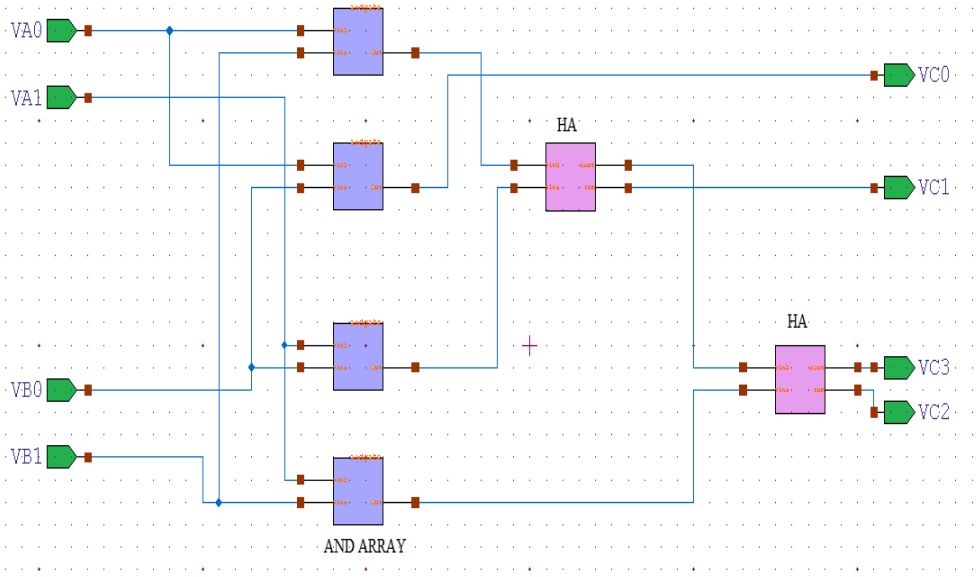

Fig 3: 2-Bit Multiplier

III. SIMULATION RESULT AND ANALYSIS

This shows Simulation results of all the building blocks. Functional verification of a design can be done by using simulation based verification. This verification ensures that the design is functionally correct when tested with a given set of inputs. Each method waveform is compared for Power Calculation, Delay Calculation and Area in terms of Transistor and the design has been implemented and simulated using Tanner Tool in 180nm technology with Operating voltage of approximately 1.8V

2-BIT MULTIPLIER

Simulated waveform of 2-bit GDI based multiplier is shown in fig 5.11.

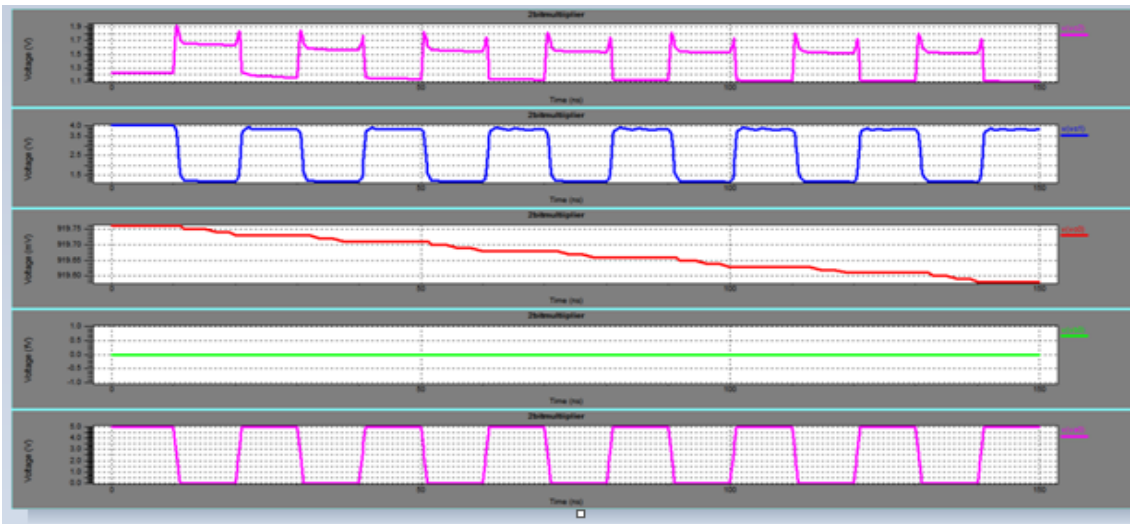

Fig 4 : Waveform of 2-bit GDI based Multiplier

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2-bit CMOS multiplier is also designed. Various parameters like delay and power dissipation is calculated for both CMOS & GDI based multiplier as shown in table 1 and 2 respectively.

Table 1
Delay and Power Dissipation of 2-bit CMOS multiplier

Vdd	Delay (ns)	Power dissipation (mW)
1.8	0.06	1.4965
1.6	0.07	1.3773
1.4	0.08	0.7645
1.2	0.085	0.4821
1.0	0.095	0.2568

Table 2
Delay and Power Dissipation of 2-bit GDI multiplier

Vdd	Delay (ns)	Power Dissipation (mW)
1.8	0.02	0.729
1.6	0.055	0.520
1.4	0.070	0.307
1.2	0.075	0.165
1.0	0.085	0.095

IV. CONCLUSION

Multiplier is one of the most important components of many digital signal processing, general purpose processing, image processing and other digital application. Multiplier performance can be measured by using performance factors like Power, Delay and area. In efforts to identify the most efficient multiplier, this research makes the following conclusions.

The GDI based wallace tree multiplier occupies smaller silicon area with higher resolution than the conventional wallace tree multiplier. Various parameters like delay and power dissipation of other circuits are also calculated with respect to different power supply

REFERENCES

1. Wallace, C. S., “A Suggestion for a Fast Multiplier”, IEEE Transactions on Computers, vol. 13, pp. 14-17, 1964.
2. Kumar, M., Hussain, M. A., and Paul, S. K., “Performance of a Two Input Nand Gate Using Subthreshold Leakage Control Techniques”, Journal of Electron Devices, Vol. 14, pp. 1161-1169, 2012.
3. Kumar, M., Hussain, M. A., and Singh, L. K., “Design of a Low Power High Speed ALU in 45nm Using GDI Technique and Its Performance Comparison”, Communications in Computer and Information Science, Springer Berlin Heidelberg, Vol. 142, pp. 458-463, 2011.
4. Gandhi, D. R., and Shah, N. N., “Comparative Analysis for Hardware Circuit Architecture of Wallace Tree Multiplier”, IEEE International Conference on Intelligent Systems and Signal Processing, Gujarat, pp. 1-6, 2013.
5. Swartzlander, E. E., and Waters, R. S., “A Reduced Complexity Wallace Multiplier Reduction”, IEEE Transactions on Computers, vol. 59, pp. 1134-1137, 2010.
6. Vinoth, C., Bhaaskaran, V. S. K., Brindha, B., Sakthikumaran, S., Kavinilavu, V., Bhaskar, B., Kanagasabapathy, M., and Sharath, B., “A Novel Low Power and High Speed Wallace Tree Multiplier for RISC Processor”, IEEE 3rd International Conference on Electronics Computer Technology, Kanyakumari, pp. 330 – 334, 2011.
7. Dubey, S., and Rao, M. J., “A High Speed and Area Efficient Booth Recoded Wallace Tree Multiplier for fast Arithmetic Circuits”, IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics & Electronics, Hyderabad, pp. 220 – 223, 2012.
8. Sureka, N., Porselvi, R., and Kumuthapriya, K., “An Efficient High Speed Wallace Tree Multiplier”, IEEE International Conference on Information Communication and Embedded system, Chennai, pp. 1023-1026, 2013.
9. Khan, S., Kakde, S., and Suryawanshi, Y., “VLSI Implementation of Reduced Complexity Wallace Multiplier Using Energy Efficient CMOS Full Adder”, IEEE International Conference on Computational Intelligence and Computing Research, Coimbatore, pp. 1-4, 2013.