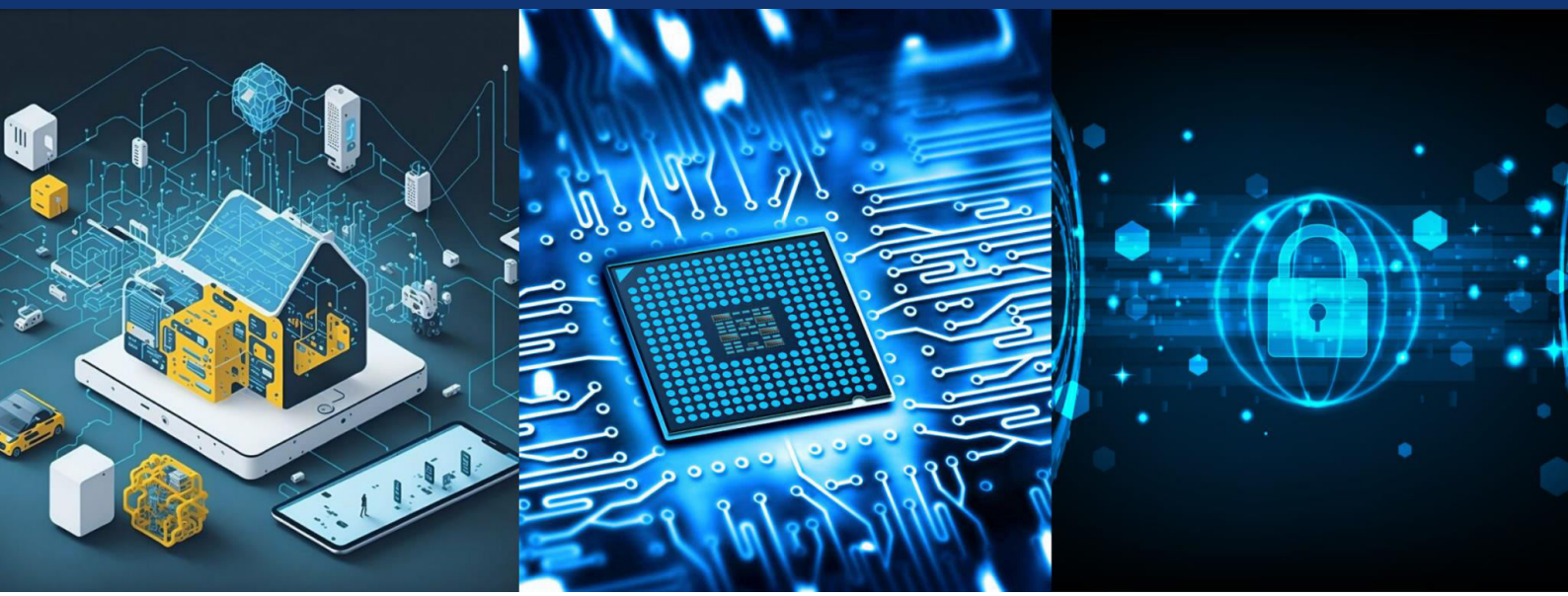
IJIRCCE

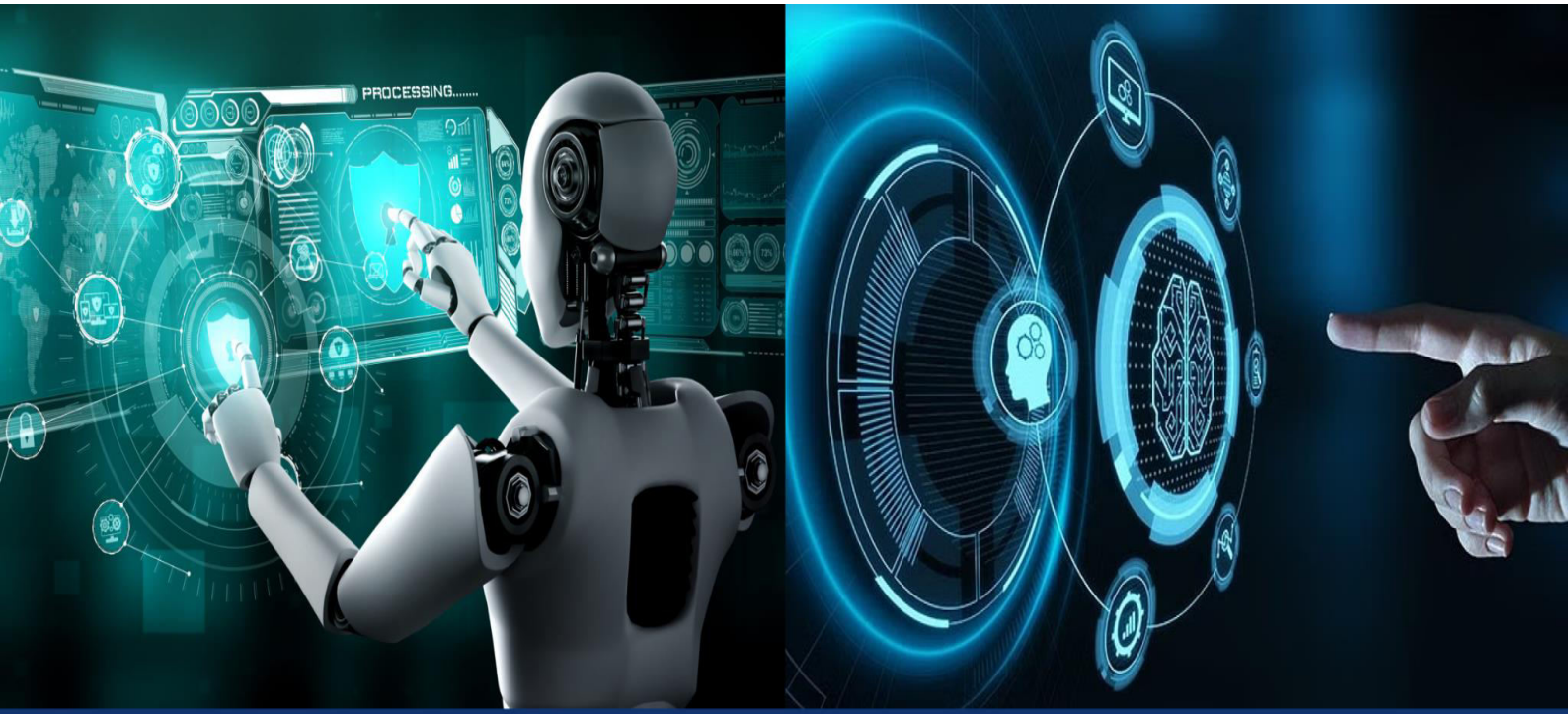
ISSN(O): 2320-9801

ISSN(P): 2320-9798



# International Journal of Innovative Research in Computer and Communication Engineering

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)




**Impact Factor: 8.771**

**Volume 13, Issue 5, May 2025**

© 2025 IJIRCCE | Volume 13, Issue 5, May 2025| DOI:10.15680/IJIRCCE.2025.1305039

www.ijircce.com | e-ISSN: 2320-9801, p-ISSN: 2320-9798| Impact Factor: 8.771| ESTD Year: 2013|

International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

# Design a CMOS Based Ring Oscillator Architecture for 5G Mobile Communication

**Sri. P. Vali Basha[1], M. Pavani[2], V. Shivaranga[3], B. Jayanth[4], P. Muniprakash[5]**

Assistant Professor, Dept. of ECE, N. B. K. R. Institute of Science and Technology, Vidyanagar, Tirupati District, Andhra Pradesh, India[1]

UG Students, Dept. of ECE, N. B. K. R. Institute of Science and Technology, Vidyanagar, Tirupati District, Andhra Pradesh, India[2-5]

**ABSTRACT:** Oscillator circuits are essential for generating accurate and stable clock signals, which are crucial for a wide range of applications, from simple wristwatches to complex satellite systems, especially in long-distance communications. These oscillators can be constructed using either passive or active components, each offering distinct advantages and limitations. In today's mobile communication landscape, the emphasis is on interoperability and energy efficiency, leading to the demand for compact, battery-operated devices. An ideal solution is offered by VLSI-based ring oscillators, which have a wide tuning range and are small and power-efficient.

The suggested design effectively controls both the voltage and supply by combining the advantages of a negative-skewed delay and a current-starved ring oscillator. It produces a primary frequency along with some harmonic distortion between the input and output signals. This design is well-suited for 5G applications, where frequency precision and low power usage are crucial, as the passive components are specifically selected to meet these requirements.

**KEYWORDS:** VLSI, 5G, CMOS, Ring Oscillator, Mobile Communication.

## I. INTRODUCTION

Radio frequency is fundamental to all wireless communication technologies, including mobile phones and automated gate systems. As these devices broadcast and receive signals, interference arises when multiple devices share the same frequencies. There is a growing demand for processors that operate at high frequencies while consuming low power. Wi-Fi, operating at 2.4 GHz and 5 GHz (corresponding to IEEE 802.11a and 802.11b), remains the leading technology in short-range wireless communication. To reduce digital noise in signals, Wi-Fi networks increasingly utilize the 5 GHz band for streaming media, and transferring music, photos, and videos. VCO plays a key role in the RF subsystem of wireless communication systems, where it is used to up-convert or down-convert signals with a local oscillator. Ideally, a VCO should have low phase noise, minimal power consumption, and a wide frequency range. Two main VCO designs exist: the ring oscillator and the LC oscillator. The ring oscillator, powered by a voltage-to-current converter, is more efficient than the relaxation oscillator, despite its broader tuning range. LC oscillators, though capable of precise phase noise performance, are large, space-consuming, and less flexible in tuning. Because of their compact size, digital compatibility, and portability, ring oscillators are typically preferred for use in modern systems. This study proposes an oscillator design with three stages, improving power efficiency, phase noise handling, and physical space utilization, while operating at a frequency of 5 GHz.

### Wi-Fi Communication System

Wi-Fi (Wireless Fidelity) technology enables wireless communication between devices via radio waves. It has become an essential part of modern life, providing internet access, device connectivity,and data transferin various environments such as homes, businesses, and public spaces. Here are the key aspects of a Wi-Fi communication system:

### Wi-Fi Standards:

Wi-Fi standards have evolved over time, with each generation offering better performance. Common standards include 802.11b, 802.11g, 802.11n, 802.11ac, and 802.11ax (Wi-Fi 6).

www.ijircce.com | e-ISSN: 2320-9801, p-ISSN: 2320-9798| Impact Factor: 8.771| ESTD Year: 2013|

International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

**Security:**
Wi-Fi networks can be secured using protocols like WEP, WPA, and WPA2/WPA3. Strong passwords, encryption, and regular updates are necessary for security.

**Range and Coverage:**
Wi-Fi range is influenced by factors such as frequency, interference, and obstacles. The 2.4 GHz band offers better range, while the 5 GHz band offers faster speeds.

**Applications:**
Wi-Fi is used in internet access, device connectivity, media streaming, gaming, and industrial applications such as machine monitoring.

**Future Developments:**
Wi-Fi continues to evolve, with new standards like Wi-Fi 6E (which includes the 6 GHz band) providing higher speeds and lower latency, and Wi-Fi 7 on the horizon.

**Ring Oscillator**
Digital circuits called ring oscillators are typically employed in integrated circuit architecture to provide periodic signals. It is made up of a feedback loop with an odd number of inverting stages or gates connected. Creating clock signals to synchronize digital systems is a common application for ring oscillators.

## II. LITERATURE REVIEW

**1. Sampe and Jahariah (2015):** Developed an ultra-low-power energy harvesting system using piezoelectric transducers and a power conditioning circuit with MPPT algorithm. Achieved 24 mW output at 90% efficiency from ambient sources as low as 500 mV.

**2. Yeo et al. (2015):** Compared CMOS rectifier topologies for micropower energy harvesters, focusing on low input voltage and frequency. Bootstrapped and fully cross-coupled designs achieved over 80% efficiency with input voltages as low as 20 mV.

**3. Hsu and Chen (2011):** Presented a low-power CMOS LC VCO with body-biasing and Q-enhancement for IEEE 802.11a applications. Operated between 4.92 GHz and 5.7 GHz with a phase noise of -118 dBc/Hz at 1 MHz offset.

**4. Kulkarni and Hosur (2013):** Designed a Current Starved Ring VCO for PLL applications using 180nm CMOS technology. Achieved a frequency range of 53 MHz to 2.348 GHz with power consumption of 848 µW and improved jitter performance.

**5. Khan and Raahemifar (2009):** Introduced a low-power current reused quadrature VCO tailored for biomedical applications. Emphasized low power consumption, reliability, and signal integrity for medical devices.

## III. EXISTING METHOD

Each CMOS component in the design operates as follows: Transistors M1 to M10 are responsible for forming the negative-skewed delay oscillators, while M11 to M16 serve as current-limited oscillators. M17 and M18 handle the biasing and control circuits. The design also incorporates five stages of inverters, M11 to M19, with current limiters placed at the first, third, and fifth stages to optimize power consumption. Transistors M20 and M21 function as current sources and biasing circuits, regulating the operational voltage of the entire topology.

The delay in the design is calculated by evaluating the delay of each individual architecture. The delay of the negative-skewed components is computed using specific equations, whereas the current-starved delay is determined separately. The total delay is then represented by combining these values, where 'τd' denotes the overall delay, 'τcs' stands for the current-starved delay, 'τns' is the initial two delay components exhibit negative skew, whereas the third component reflects the influence of the number of stages present in each design.

© 2025 IJIRCCE | Volume 13, Issue 5, May 2025| DOI:10.15680/IJIRCCE.2025.1305039

www.ijircce.com | e-ISSN: 2320-9801, p-ISSN: 2320-9798| Impact Factor: 8.771| ESTD Year: 2013|

International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

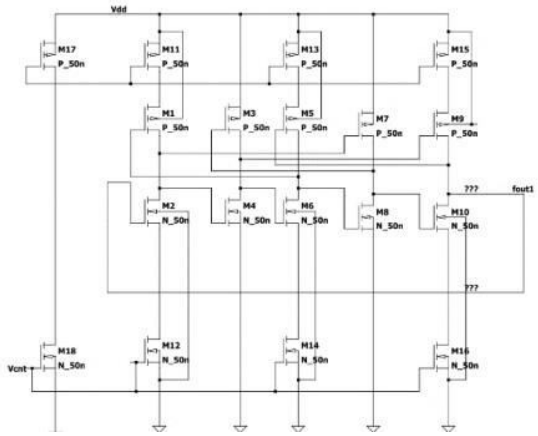



**Fig:1 Schematic of Ring oscillator**

The architecture was simulated using Cadence Virtuoso to examine waveform results, perform fast Fourier transform (FFT) analysis, assess harmonic distortion, and evaluate frequency components. Based on specific design parameters, the architecture was tested with the selected technology. Power consumption was adjusted according to the simulation results, and comparisons were made between the proposed architecture and existing designs in terms of harmonic distortion, power efficiency, and frequency performance.

## IV. PROPOSED METHOD

The SAPON (Stacked Arranged low Power ON transistor) technique is an innovative approach in low-power VLSI design that targets reducing leakage power. The proposed approach was also evaluated against standard techniques such as LECTOR and LCNT and STACK ONOFIC, showing that SAPON significantly outperforms these methods in terms of power consumption.

**SAPON Approach**

The SAPON technique primarily focuses on managing leakage power, a key contributor to power usage in VLSI circuits. Leakage power refers to the unwanted current that flows through transistors even when they are supposed to be in the 'off' state. To mitigate this issue, the SAPON technique introduces a pair of leakage-controlling transistors placed outside the main logic circuitry. These transistors act as resistive elements, effectively increasing the resistance between the supply voltage (Vdd) and ground, thereby reducing the leakage current.
Further details about SAPON include:

**Transistor Placement:** In the SAPON technique, the leakage control transistors are arranged in a stacked configuration outside the core logic path. This design choice allows for effective leakage suppression without interfering with the primary logic operation.

**Active Operation**: The gate terminals of the SAPON transistors are connected to both ground and the supply voltage. This ensures the transistors remain active during the entire operation cycle, which is essential for their role as leakage-control devices.

**Reducing Leakage Current**: By increasing the resistance between Vdd and ground, SAPON transistors reduce short-circuit leakage current during transitions and sub-threshold leakage current during the leveling phase. This is accomplished by creating a higher voltage drop across the transistors, thereby reducing the current flow.
Simulation results demonstrate that the SAPON technique effectively reduces power consumption across various logic gates, including inverters, NAND, NOR, and multiplexers. Compared to conventional methods like LECTOR, LCNT, and STACK ONOFIC, SAPON achieves approximately a 23% reduction in power usage.

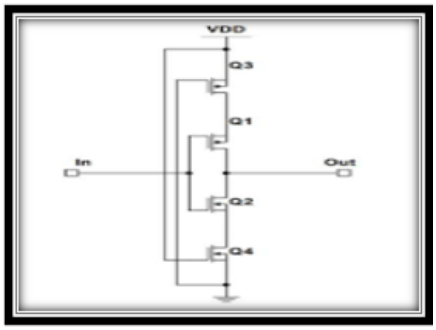
**Area Overhead**: Although the SAPON technique effectively reduces power consumption, its area overhead is comparable to that of other leakage control methods, meaning it does not notably increase the circuit's physical size.

© 2025 IJIRCCE | Volume 13, Issue 5, May 2025| DOI:10.15680/IJIRCCE.2025.1305039

www.ijircce.com | e-ISSN: 2320-9801, p-ISSN: 2320-9798| Impact Factor: 8.771| ESTD Year: 2013|

International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)




The SAPON technique shows great promise for low-power VLSI designs, especially for applications where power efficiency is crucial, such as in battery-powered devices.

In this chapter, we explore a novel design of SRAM using sleep transistors, which is an example of a power gating technique. Power gating is a highly effective method for reducing power consumption in modern low-power technologies.

The proposed architecture aims to combine insights from various designs to create a system that maximizes benefits while minimizing limitations, specifically for 5G applications. The design focuses on optimizing size, frequency, and power efficiency to meet the requirements of 5G devices. The architecture is inspired by both current-starved and negatively skewed oscillator designs.

Each CMOS component is designed as follows: Transistors M1 to M10 form the negative-skewed delay oscillators, M11 to M16 act as current-limited oscillators, and M17 and M18 manage the biasing and control circuits. The design also incorporates five stages of inverters (M11 to M19), with current limiters at the first, third, and fifth stages to optimize power usage. Transistors M20 and M21 serve as current sources and biasing circuits, controlling the operational voltage of the overall topology.

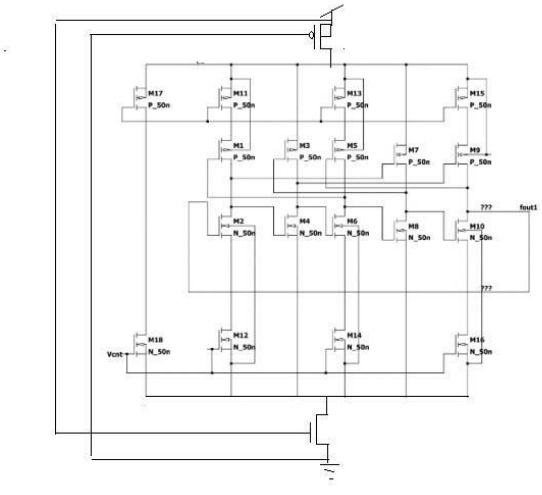


**Fig:3 Schematic of Sapon approach Ring oscillator**

The delay is calculated by evaluating each architecture's delay independently. The delay for the negative-skewed components is determined using specific equations, while the current-starved delay is calculated separately. The total delay is then expressed by combining these values.

The architecture was simulated using Cadence Virtuoso to analyze waveform results, perform fast Fourier transform (FFT), examine harmonic distortion, and evaluate frequency components. The architecture was tested with specific

© 2025 IJIRCCE | Volume 13, Issue 5, May 2025| DOI:10.15680/IJIRCCE.2025.1305039

www.ijircce.com | e-ISSN: 2320-9801, p-ISSN: 2320-9798| Impact Factor: 8.771| ESTD Year: 2013|

International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

design parameters on the chosen technology. Power requirements were adjusted based on the simulation results, and comparisons were made between the proposed design and existing architectures in terms of harmonic distortion, power consumption, and frequency performance

## V. RESULTS & ANALYSIS

A comprehensive evaluation of the Ring Oscillator architecture was conducted through simulation analysis in Tanner EDA's S-edit environment. Prior to initiating the simulation phase, thorough verification was performed to eliminate schematic and connectivity errors. The T-Spice simulation framework was configured through several critical parameters: technology file integration, simulation period definition, supply voltage specification, and implementation of calculation commands for power consumption and propagation delay assessment. Simulation execution was triggered via the simulation command interface.

Following successful simulation completion, a detailed waveform analysis was performed to characterize the Ring Oscillator structure's behaviour under various operating conditions. This examination encompassed multiple aspects including MOSFET utilization patterns, power consumption metrics, and timing characteristics. The waveform analysis provided crucial insights into the dynamic behaviour of the proposed architecture, facilitating a comprehensive evaluation of its functional characteristics and performance indicators.

The investigation into MOSFET-based designs offered valuable insights into the structural efficiency and optimal resource utilization of the flip-flop architecture. Power consumption was examined to evaluate the energy efficiency of the proposed design, while delay parameters were analyzed to assess the operational speed and responsiveness of the Ring Oscillator configuration.

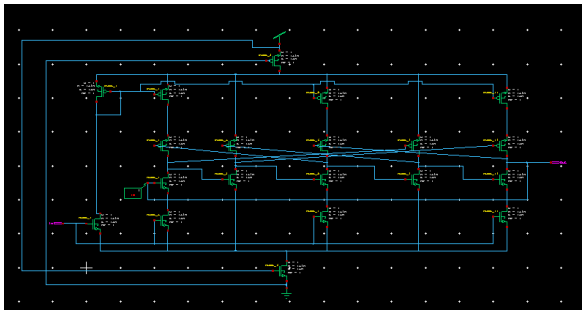


**Fig4: Schematic of Proposed method**

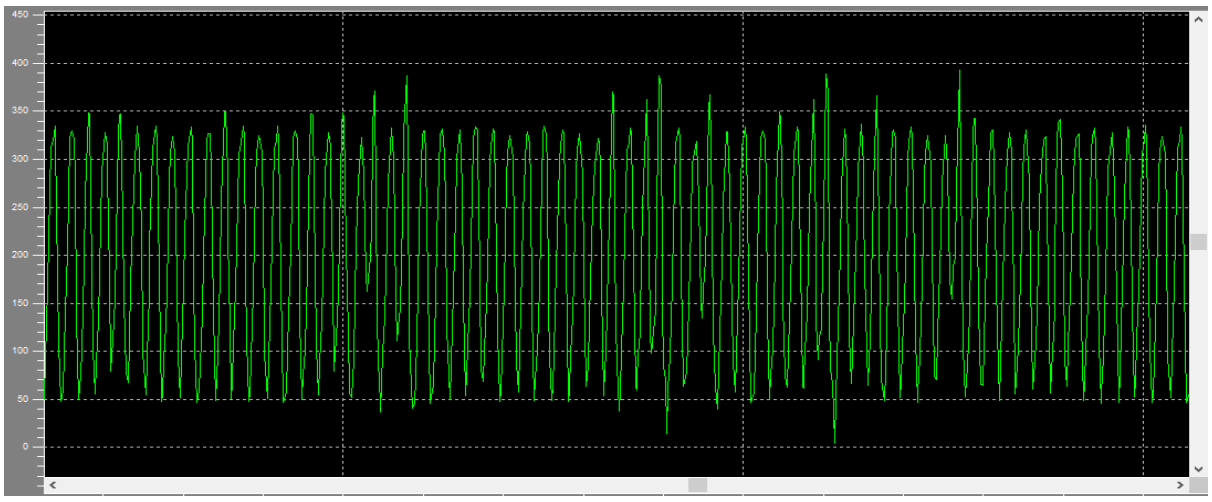



**Fig5: Output waveforms of Proposed method**

www.ijircce.com | e-ISSN: 2320-9801, p-ISSN: 2320-9798| Impact Factor: 8.771| ESTD Year: 2013|

International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE)

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)

**Comparison Table**

| | MOS count | Power consumption(w) | Frequency (GHz) |
|---|---|---|---|
| **Proposed** | 18 | 1.68x10^-4 | 28.24 |
| **Extension** | 20 | 6.43x10^-5 | 32.86 |

## VI. CONCLUSION

For 5G mobile communication, the transceiver needs a Voltage-Controlled Oscillator (VCO) with a broad tuning range, fast settling time, and minimal phase noise to ensure optimal performance. The advancements in 5G technologies, along with IoT applications, are driving innovations in areas such as smart homes, cities, automobiles, power grids, and healthcare. The current-starved oscillator design is efficient in reducing harmonic distortion but sacrifices frequency range and increases the required area. On the other hand, the negative-skew oscillator design enables higher frequencies, though it necessitates a higher control voltage, which in turn increases harmonic distortion.

The proposed architecture merges both designs, striking a balance between lower harmonic distortion and higher frequencies, making it suitable for 5G applications that require low-power operation and high-frequency performance. This combined approach enhances power efficiency and supports operation at lower voltages. By integrating current-starved and negative-skewed topologies, the architecture is optimized for 5G applications through a careful selection of passive components, ensuring optimal performance.

## REFERENCES

[1] Misra, D. K. (2004). Radio- Frequency and Microwave Communication Circuits. John Wiley & Sons, Hoboken, United States. doi:10.1002/0471653764.

[2] Rohde, U. L., Rubiola, E., & Whitaker, J. C. (2021). Microwave and Wireless Synthesizers. John Wiley & Sons, Hoboken, United States. doi:10.1002/9781119666127.

[3] Vendelin, G. D., Pavio, A. M., & Rohde, U. L. (2005). Microwave Circuit Design Using Linear and Nonlinear Techniques. John Wiley & Sons, Hoboken, United States. doi:10.1002/0471715832.

[4] Mandal, M. K., & Sarkar, B. C. (2010). Ring oscillators: Characteristics and applications. Indian Journal of Pure & Applied Physics, 48, 136–145.

[5] Rajesh, V., & Abdul Rajak, A. R. (2020). Channel estimation for image restoration using OFDM with various digital modulation schemes. Journal of Physics: Conference Series, 1706(1), 012076. doi:10.1088/1742-6596/1706/1/012076.

INTERNATIONAL STANDARD SERIAL NUMBER INDIA

INNO SPACE SJIF Scientific Journal Impact Factor

doi crossref

निस्केयर NISCAIR

# INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

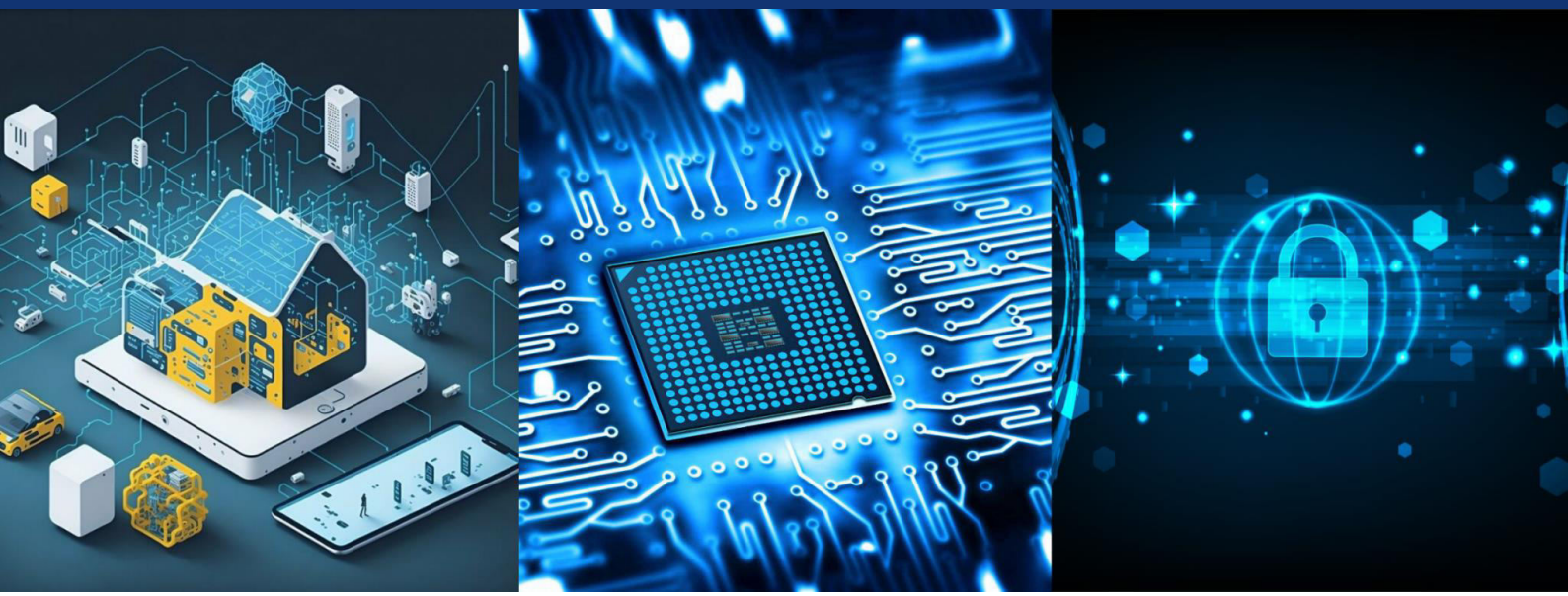
## IN COMPUTER & COMMUNICATION ENGINEERING

9940 572 462 6381 907 438 ijircce@gmail.com

www.ijircce.com

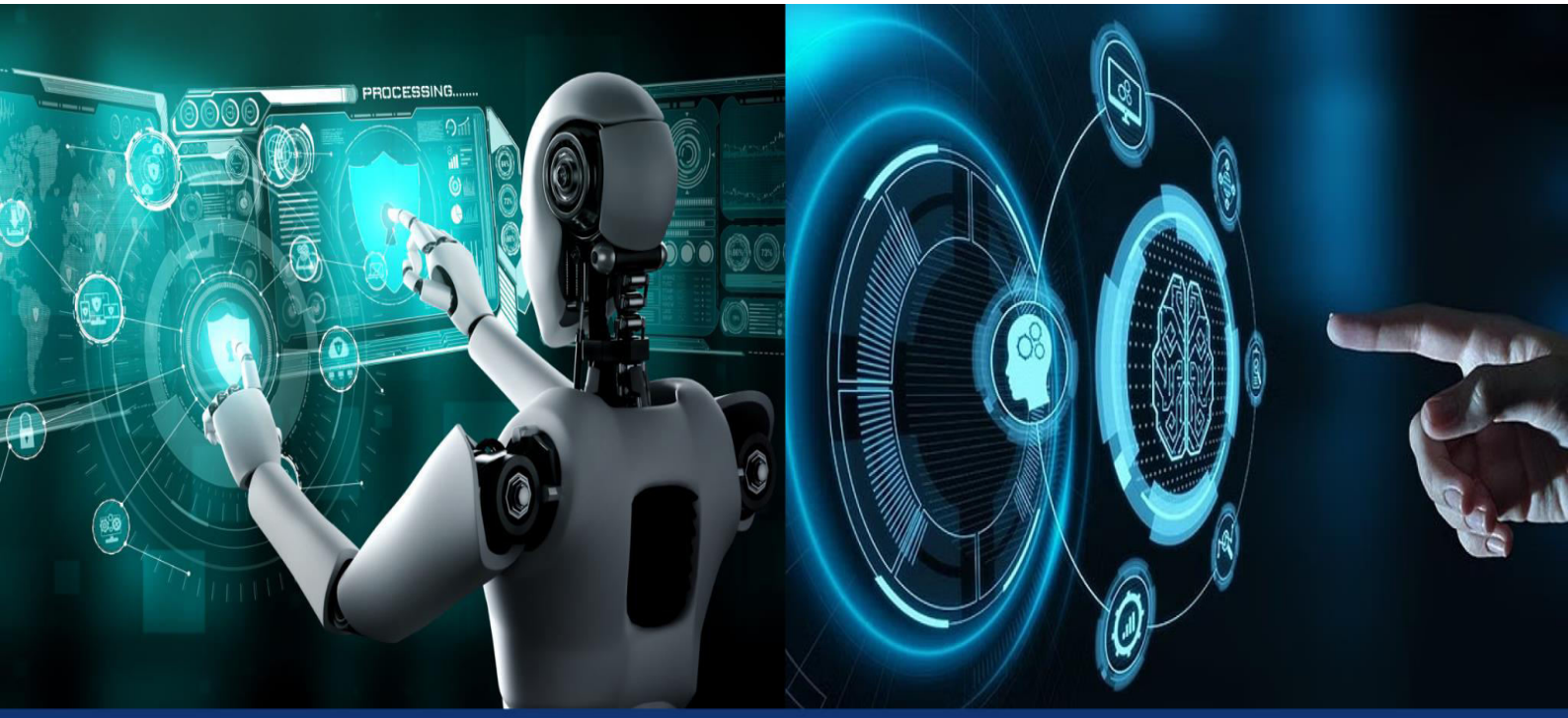
Scan to save the contact details

ISSN(O): 2320-9801
ISSN(P): 2320-9798



# International Journal of Innovative Research in Computer and Communication Engineering

(A Monthly, Peer Reviewed, Refereed, Scholarly Indexed, Open Access Journal)




**Impact Factor: 8.771** **Volume 13, Issue 5, May 2025**

INTERNATIONAL STANDARD SERIAL NUMBER INDIA

INNO SPACE SJIF Scientific Journal Impact Factor

doi crossref

निस्केयर NISCAIR

# INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

## IN COMPUTER & COMMUNICATION ENGINEERING

9940 572 462 6381 907 438 ijircce@gmail.com

www.ijircce.com

Scan to save the contact details