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A LOW POWER 8GS/S COMPARATOR FOR HIGH SPEED ANALOG TO DIGITAL CONVERSION

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ABSTRACT: In high-speed high-resolution Analog to digital converters, comparators have a key role in quality of performance. Comparator is the most analysing unit in an Analog to Digital Converter (ADC). To improve the performance of ADCs, the comparator which has high speed and consumes less power has to be used. Designing a comparator is more challenging when the supply voltage is smaller. To achieve high speed, large number of transistors are required to compensate the reduction of supply voltage, which also means that more die area and power is needed. In this project we designed a comparator which has high-speed, low-power consumption and works even with low supply voltages. This comparator design has less number of transistors and by this the delay time is reduced. Apart from technological modifications, developing new circuits which avoid stacking too many transistors between the supply rails are preferable for low-voltage operation, especially if they do not increase the circuit complexity. This comparator enhances the speed and performance even with a low power supply voltage. Additional circuitry is added to the conventional dynamic comparator to achieve our novel comparator. This design is done through the DSCH and Micro wind Electronic Design Automation

KEYWORDS: Comparator, DSCH, Automation.

I.INTRODUCTION

The need for ultra-low power, area efficient, and high speed Analog-to-digital converters is pushing toward the use of dynamic regenerative comparators to maximize speed and power efficiency. COMPARATOR is one of the fundamental building blocks in most Analog-to-digital converters (ADCs). Many high- speed ADCs, such as flash ADCs, require high-speed, low-power comparators with small chip area. High-speed comparators in ultra-deep sub-micrometer (UDSM) CMOS technologies suffer from low supply voltages especially when considering the fact that threshold voltages of the devices have not been scaled at the same pace as the supply voltages of the modern CMOS processes. Hence, designing high-speed comparators is more challenging when the supply voltage is smaller. In other words, in a given technology, to achieve high speed, larger transistors are required to compensate the reduction of supply voltage, which also means that more die area and power is needed. Besides, low-voltage operation results in limited common-mode input range, which is important in many high-speed ADC architectures, such as flash ADCs. Many techniques, such as supply boosting methods, techniques employing body-driven transistors, current-mode design and those using dual- oxide processes, which can handle higher supply voltages have been developed to meet the low-voltage design challenges.

Boosting and bootstrapping are two techniques based on augmenting the supply, reference, or clock voltage to address input-range and switching problems. These are effective techniques, but they introduce reliability issues especially in UDSM CMOS technologies. Apart from technological modifications, developing new

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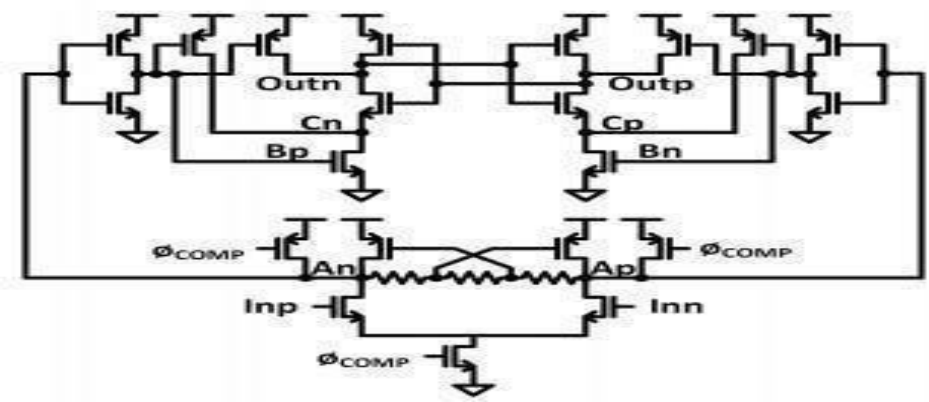
circuit structures which avoid stacking too many transistors between the supply rails is preferable for low-voltage operation, especially if they do not increase the circuit complexity. A additional circuitry is added to the conventional dynamic comparator to enhance the comparator speed in low supply voltages. Despite the effectiveness of this approach, the effect of component mismatch in the additional circuitry on the performance of the comparator should be considered. The structure of double-tail dynamic comparator first proposed in is based on designing a separate input and cross- coupled stage. This separation enables fast operation over a wide common-mode and supply voltage range. In this paper, a comprehensive analysis about the delay of dynamic comparators has been presented for various architectures. Furthermore, based on the double-tail structure proposed in a new dynamic comparator is presented, which does not require boosted voltage or stacking of too many transistors.

II.EXISTING CIRCUIT

The existing Comparator employs a high gain preamplifier that relaxes latch design, and reduces comparator's offset and input capacitance. The gain boosting technique in preamplifier employs three 10k resistors and increases pre-amplifier's gain. The comparator requires a single clock φCLK, which only needs to drive three transistors.

The power consumption is high and requires high input voltage. The number of transistors employed in the circuit is also quiet high in number.



III. PROPOSED CIRCUIT

Due to the better performance of double-tail architecture in low-voltage applications, the proposed comparator is designed based on the double-tail structure. The main idea of the proposed comparator is to increase ΔVfn/fp in order to increase the latch regeneration speed. For this purpose, two control transistors (Mc1 and Mc2) have been added to the first stage in parallel to M3/M4 transistors but in a cross-coupled manner.

The operation of the proposed comparator is as follows (see Fig 9). During

reset phase (CLK 0, both fn and fp nodes *M*tail *V*1DD and, hence *M*tail2 are off, avoiding static power), transistor *M*c1 and *M*c2 are cut off. *M*3 Intermediate and *M*4 pulls stage transistors, M_{R1} and M_{R2}, reset both latch outputs to ground.

During decision-making phase (CLK V_{DD}, M_{tail1}, and M_{tail2} are on), transistors M_3 and M_4 turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since fn and fp are about V_{DD}). Thus, fn and fp start to drop with different rates according to the input voltages. Suppose $V_{INP} > V_{INN}$, thus fn drops faster than fp, (since M_2 provides more current than M_1). As long as fn continues falling, the corresponding pMOS control transistor (M_{c1} in this case) starts to turn on, pulling fp node back to the V_{DD}; so, another control transistor (M_{c2}) remains off, allowing fn to be discharged completely.

In other words, unlike the conventional double tail comparator which has

high input transistor transconductance and input voltage difference, in the proposed structure as soon as the comparator detects that for instance node fn discharges faster, a pMOS transistor (M_{c1}) turns on, pulling the other node fp back to the V_{DD}. Therefore by the time passing, the difference between fn and fp ($\Delta V_{fn/fp}$) increases in an exponential manner, leading to the reduction of latch regeneration time. Despite the effectiveness of the proposed idea, one of the points which should be considered is that in this circuit, when one of the control transistors (e.g., M_{c1}) turns on, a current from V_{DD} is drawn to the ground via input and tail transistor (e.g., M_{c1}, $M1$, and M_{tail1}), resulting in static power

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consumption. To overcome this issue, two nMOS switches are used below the input transistors.

At the beginning of the decision-making phase, due to the fact that both

fn and fp nodes have been pre-charged to V_{DD}(during the reset phase), both switches are closed and fn and fp start to drop with different discharging rates. As soon as the comparator detects that one of the fn/fp nodes is discharging faster, control transistors will act in a way to increase their voltage difference. Suppose that fp is pulling up to the V_{DD} and fn should be discharged completely, hence the switch in the charging path of fp will be opened (in order to prevent any current drawn from V_{DD}) but the other switch connected to fn will be closed to allow the complete discharge of fn node. In other words, the operation of the control transistors with the switches emulates the operation of the latch.

IV. PERFORMANCE COMPARISON

Comparator structure	**Conventional Dynamic Comparator**	**Double-tail Dynamic Comparator**	**Proposed Dynamic Comparator**	
Technology CMOS	180 nm	180 nm	180 nm	
Supply voltage (V)	0.8 V	0.8 V	0.8 V	
Maximum sampling frequency	900 MHz	1.8 GHz	2.4 GHz	
Delay/log(ΔVin) (ps/dec.)	940	358	294	
Peak transient noise voltageat regeneration time(nV)	215 n	221 n	219 n	
Kickback noise voltage (at ΔVin = 10mV)	51.3 mV	5.3 mV	43 mV	With neutralization : 13 mV
Energy per conversion (J)	0.3 p	0.27 p	0.24 p	Without *Msw*1 and *Msw*2 : 0.265 p
Input-referred offset voltage (mV)	7.89 mV	7.91 mV	7.8 m	
Estimated area	16 μ × 16 μ	28 μ × 12 μ	28 μ × 14 μ	

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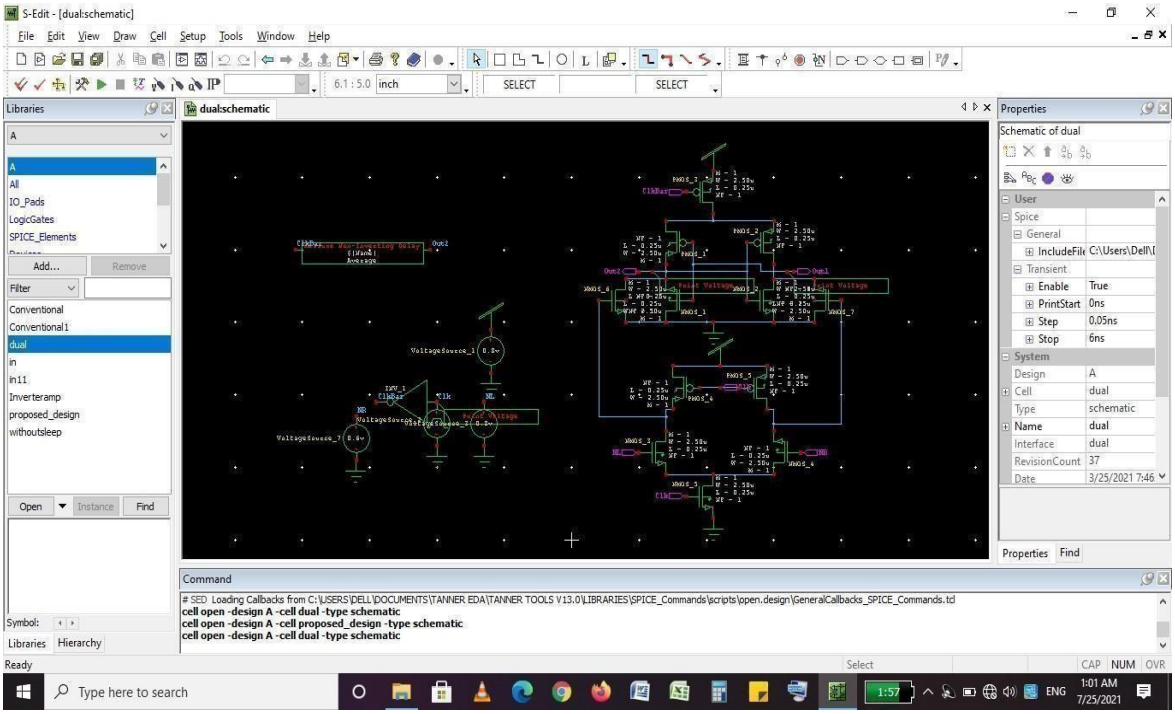
V . SCHEMATIC OF THE PROPOSED SYSTEM



VI. SIMULATION RESULTS

Tanner EDA provides a complete line of software solutions for the design, layout and verification of Analog and mixed-signal (A/MS) integrated circuits (ICs). Tanner's solution consists of tool for schematic entry, circuit simulation, waveform probing, full-custom layout editing, placement and routing, netlist extraction, LVS and DRC verification.

Today's semiconductors and electronic systems are complex that designing them would be impossible without electronic design automation (EDA). This primer provides a comprehensive overview of the electronic design process, and then describes how design teams use Cadence tools to create the best possible design in the least amount of the time.

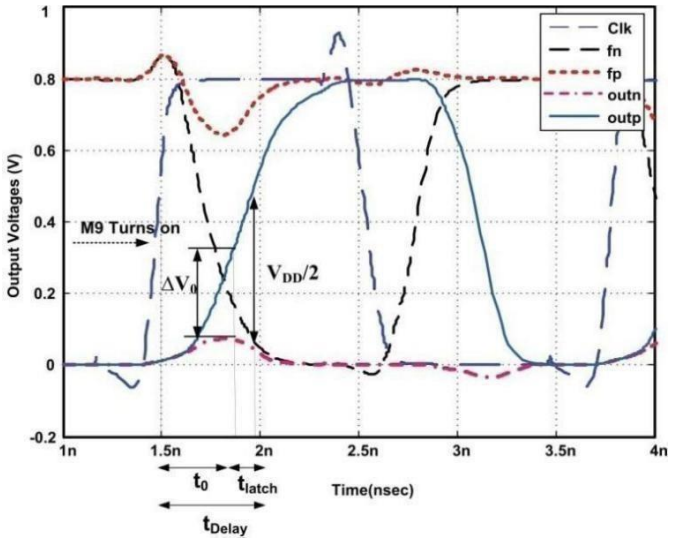


Fig.1. Simulation analysis of Proposed circuit

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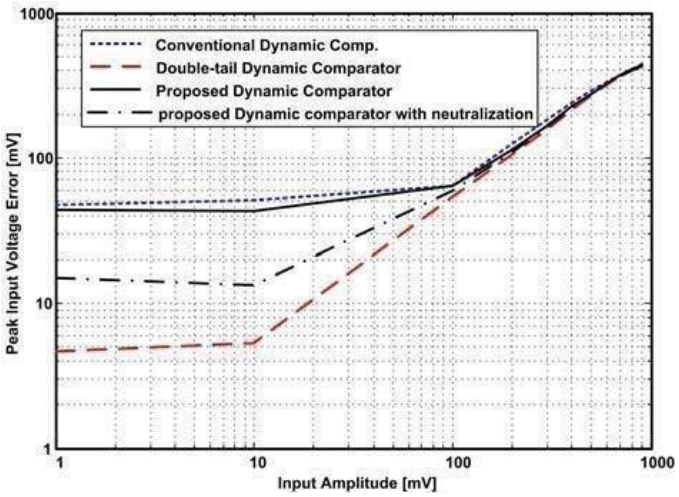

Fig. 2.peak input voltage due to kickback noise

VII. Conclusion and Future Work

In this paper, we presented a comprehensive delay analysis for clocked dynamic comparators. Two common structures of conventional dynamic comparator and conventional double-tail dynamic comparators were analysed. Also, based on analyses, a new dynamic comparator with low-voltage low-power capability was proposed in order to improve the performance of the comparator. Post-layout simulation results in 0.18-μm CMOS technology confirmed that the delay and energy per conversion of the proposed comparator is reduced to a great extent in comparison with the conventional dynamic comparator and double-tail comparator. A novel circuit topology was developed to reduce the recovery time, and hence increase the comparator speed, without increasing the power dissipation. The comparator circuit was designed for use in high-speed ADCs with sampling speeds up to 8-GS/s. It demonstrates higher bandwidth compared to existing architectures without the use of bandwidth enhancing inductors.

REFERENCES

1. B. Goll and H. Zimmermann, "A comparator with reduced delay time in 65-nm CMOS for supply voltages down to 0.65," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 11, pp. 810–814, Nov. 2009.
2. S. U. Ay, "A sub-1 volt 10-bit supply boosted SAR ADC design in standard CMOS," *Int. J. Analog Integr. Circuits Signal Process.*, vol. 66, no. 2, pp. 213– 221, Feb. 2011.
3. A. Mesgarani, M. N. Alam, F. Z. Nelson, and S. U. Ay, "Supply boosting technique for designing very low- voltage mixed-signal circuits in standard CMOS," in *Proc. IEEE Int. Midwest Symp. Circuits Syst. Dig. Tech. Papers*, Aug. 2010, pp. 893–896.
4. B. J. Blalock, "Body-driving as a Low-Voltage Analog Design Technique for CMOS technology," in *Proc. IEEE Southwest Symp. Mixed-Signal Design*, Feb. 2000, pp. 113–118.
5. M. Maymandi-Nejad and M. Sachdev, "1-bit quantiser with rail to rail input range for sub-1V $\Delta\Sigma$ modulators," *IEEE Electron. Lett.*, vol. 39, no. 12, pp. 894– 895, Jan. 2003
6. A. Nikoozadeh and B. Murmann, "An analysis of latched comaprator offset due to load capacitor mismatch," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 12, pp. 1398–1402, Dec. 2006.
7. S. Babayan-Mashhadi and R. Lotfi, "An offset cancellation technique for comparators using body-voltage trimming," *Int. J. Analog Integr. Circuits Signal Process.*, vol. 73, no. 3, pp. 673–682, Dec. 2012.
8. J. He, S. Zhan, D. Chen, and R. J. Geiger, "Analyses of static and dynamic random offset voltages in dynamic comparators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 5, pp. 911–919, May 2009.

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