Implementation of Phase Shifted Semi-Bridgeless PFC Converter

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Abstract: As most of the electronic appliances use DC power so improvement in AC–DC converter is always at large by the researchers. The factors of improvement of power quality are reduction in total harmonic distortion and improvement in power factor at input ac, and tight output dc regulation. In such context, the AC-DC boost converters have gained significant importance, especially when they are used in Continuous Conduction Mode (CCM). This work presents a bridgeless ACDC boost converter operating in CCM. The implementation of input current and output voltage controller is also discussed. Then a comparative analysis based on simulation results of bridgeless and bridge boost rectifier is presented. Bridgeless boost AC-DC converter has outperformed the conventional techniques due to lower conduction losses, lower THD of input current and improved input power factor.

KEYWORDS: Bridge boost ac-dc converter, Continuous Conduction Mode, Power Factor Correction (PFC), Bridgeless boost ac-dc converter, Total Harmonic Distortion (THD)

I. INTRODUCTION

The charging AC outlet predictably needs an plug in AC/DC charger with a power factor correction. For the PFC application a multiple of circuit topologies and con-trol methods have been developed. The single-phase active PFC techniques can be classi ed into two approaches: they are single-stage approach and the two-stage approach. The single-stage approach is right for low power level applications. It can only applicable for lead acid batteries charging because of frequency ripple problem. Therefore, the two-stage approach is the suitable for high storage battery chargers used for high power applications, where the power rating is relatively high, and lithiumion batteries are used as the main energy storage system. In the two-stage architecture, the rst stage is PFC recti cation where it recti es the input ac volt-age and transfers it to a dc link. At the same time, the PFC is also achieved. A phase shifted semi bridgeless PFC topology operated under continuous conduction mode as the two stage charger speci cally with the ac-dc PFC converter and dc-dc converter for battery charging with various duty cycles. A Plug-In hybrid electric vehicle (PHEV) is a hybrid vehicle with a storage system that can be recharged by connecting a plug to an external electric power source. The charging ac outlet inevitably needs an onboard acdc charger with power factor correction (PFC). An onboard charger could charge a depleted battery pack in PHEVs to 95% charge. A variety of circuit topologies and control methods has been developed for PHEV battery chargers. The two-stage approach with cascaded PFC acdc and dcdc con-verters is the common architecture of choice for PHEV battery chargers, where the power rating is relatively high, and lithium-ion batteries are used as the main energy storage system. The single-stage approach is generally only suitable for lead acid batteries due to a large low-frequency ripple in the output current. In the two-stagearchitecture, the PFC stage recti es the input ac voltage and transfers it into a regu-lated intermediate dc-link bus. At the same time, PFC is achieved. A boost-derived PFC topology operated in continuous conduction mode is used in this paper as the main candidate for the front-end acdc PFC converter for PHEV battery charging. The front-end candidate topologies in the boost-derived class include the interleaved boost converter, the bridgeless boost converter, the dual-boost converter, the semi-bridgeless boost converter, and the proposed phase-shifted semi-bridgeless (PSSB) boost converter.

Recently, much research e orts has been devoted to improving the performance of boostconverter in terms of high power density and systems energy e ciency.This project presents a power converter and its control circuit for high-frequency-fed ac to dc conversion. Based on the resonant technique, the input current is shaped to be sinusoidal and is forced to follow the high-frequency sinusoidal input voltage so as to achieve unity power factor. With the proper

selection of the characteristic impedance of the resonant tank, the converter is able to perform the function of a boost converter. The initial condition of the resonant tank is used to control the output voltage gain of the converter. Since all the switches are operated at the fundamental frequency of the input ac source, the switching loss of the converter is small. A control scheme is also proposed for the converter. The use and design of a Boost pre-regulator for the Power Factor Correction and the design, use and anal-ysis of boost Converter for power Factor Correction are described. Comparision of various AC-DC Converter topologies for Power Factor Correction is described. The basic purpose of a Power Factor Correction circuit is to make the line current follow the waveform of the line voltage so that the input to the power supply becomes purely resistive or behaves like a resistor and hence to improve the power factor. This project work makes the use of Boost Converter in the Power Factor Correc-tion circuit so as to improve the power factor. A comprehensive study on state of art of power factor corrected single-phase AC-DC converters confgurations, control strategies, selection of components and design considerations, performance evalu-ation, power quality considerations, selection criteria and potential applications, latest trends, and future developments. Simulation results as well as comparative performance are presented and discussed for most of the proposed topologies. Inter-leaved boost converters have been studied in recent years with the goal of improving power-converter performance in terms of size, efficiency, conducted electromagneticemission and also transient response. The gains of interleaving consist of high power potential, modularity and better reliability.

II.   PROPOSED PFC TECHNIQUE

Phase Shifted Semi-bridgless PFC Converter
The proposed topology exploits the advantages of the bridgeless and semi-bridgeless boost PFC topologies. In particular, it features reduced EMI, high e ciency at light loads, and low lines, which is critical to minimize the charger size, cost, charging time, and amount and cost of electricity drawn from the utility. The proposed converter steady-state operation is given in the following section.

Converter Steady-State Operation

To analyze the circuit operation, the input line cycle is separated into positive and negative half-cycles. In addition, the detailed circuit operation depends on the duty cycle. Positive half-cycle operation is provided for D > 0:5 and D < 0:5.

Positive Half-Cycle Operation

During the positive half-cycle, when the ac input voltage is positive, Q1 turns on and current ows through L1 and Q1 and continues through Q2 and then L2, returning to the line while storing energy in L1 and L2. When Q1 turns o , the energy stored in L1 and L2 is released as current ows through D1, through the load, and returns through the body diode of Q2 partially through Db back to the input.

Negative Half-Cycle Operation

During the negative half-cycle, when the ac input voltage is negative, Q2 turns on and current ows through L2 and Q2 and   continues   through   Q1   and   then   L

returning to the line while storing energy in L2 and L1. When Q2 turns o , the energy stored in L2 and L1 is released as current ows through D2, through the load, and returns split between the body diode of Q1 and Da back to the input.

Detailed Positive Half-Cycle Operation and Analysis

for D > 0:5

The detailed operation of the proposed converter depends on the duty cycle. During any half-cycle, the converter duty cycle is either greater than 0.5 (when the input voltage is smaller than half of the output voltage) or smaller than 0.5 (when the input voltage is greater than half of the output voltage). The three unique operating interval circuits of the proposed converter are provided in Figs for duty cycles larger than 0.5 during the positive half-cycle input.Waveforms of the proposed converter during positive half-cycle operation with D > 0:5 are shown in Fig. 4.4. To simplify the analysis, it is assumed that the current splits between the bridge diode, the body diode, and the MOSFET channel equally. The intervals of operation are explained here.
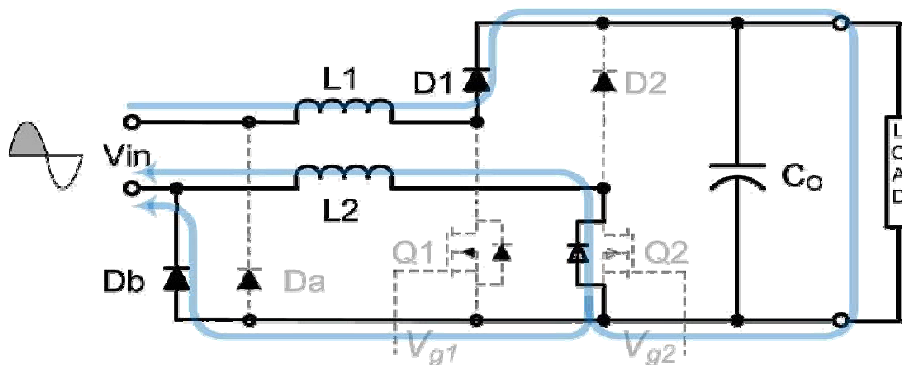

Figure 1. Intervals 1 and 3: Q1 and Q2 on.

Interval 1 [t_0 t_1]: At t_0, Q1/ Q2 are on, as shown in Fig.4.1. During this interval, the current in series inductances L1 and L2 increases linearly and stores the energy in these inductors. The energy stored in Co provides energy to the load. The return current is split among Db, Dq2, and Q2.

Interval 2 [t_1 t_2]: At t1, Q1 is on, and Q2 is o , as shown in Fig.4.2. During this interval, the current in series inductances L1 and L2 continues to increase linearly and store the energy in these inductors. The energy stored in Fig.4.1. PSSB boost converter steady-state waveforms for D > 0:5 provides the load energy. The return current is split only between Db and Dq2.
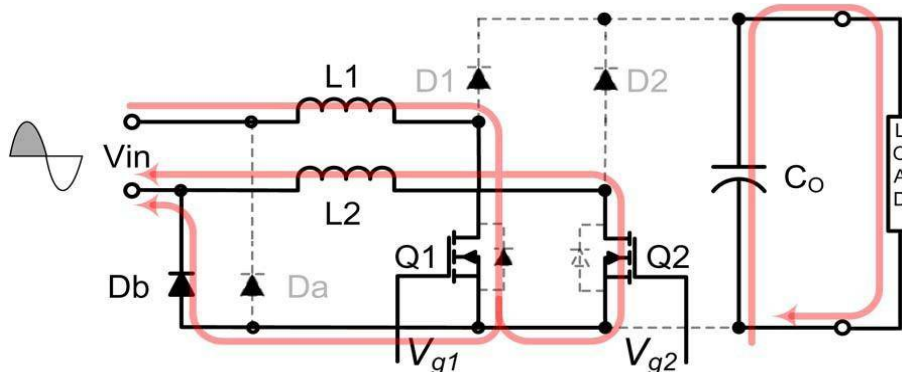

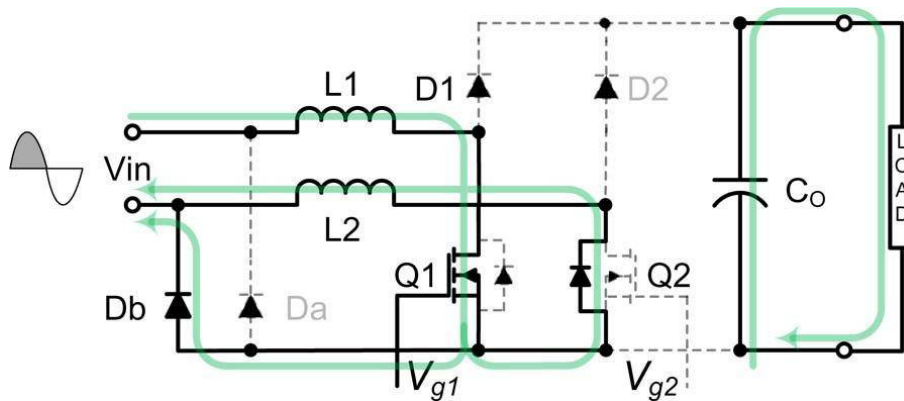Figure 2: Interval 2: Q1 on, body diode of Q2 conducting

Figure 3: Interval 4: Q1 oand Q2 on.

Interval 3 [t_2 t_3]: At t2, Q1/Q2 are on again, and interval 1 is repeated, as shown in Fig.4.1. During this interval, the current in series inductances L1 and L2 increases linearly and stores the energy in these inductors. The return current is again split among Db, Dq2, and Q2.

Interval 4 [t3-t4]: At t3, Q1 is o , and Q2 is on, as shown in Fig.4.3. During this interval, the energy stored in L1 and L2 is released to the output through L1, D1, partially Q2, Dq2, L2, and Db.

Detailed Positive Half-Cycle Operation and Analysis

for D < 0:5

The three unique operating interval circuits of the proposed converter are given in Figs. for duty cycles less than 0.5 during the positive half-cycle. The waveforms of the proposed converter during these conditions are shown in Fig.4.8 The intervals of operation are explained here.
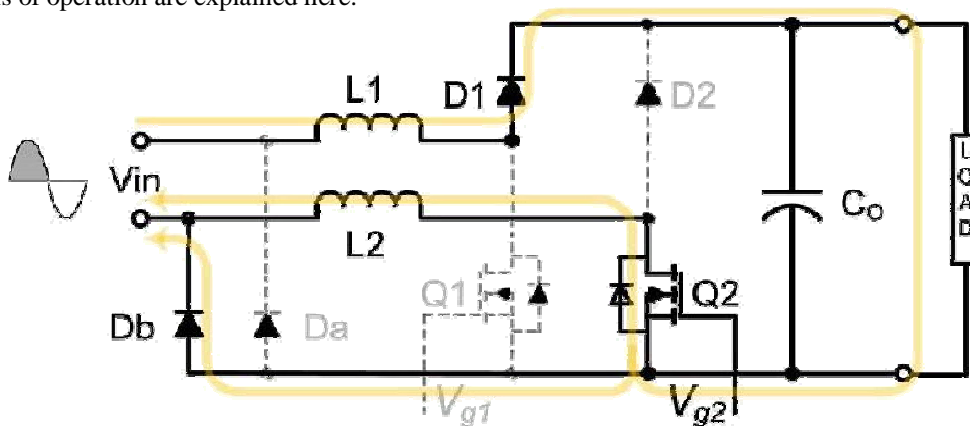

Figure 4: Intervals 1 and 3: Q1 and Q2 o , body diode of Q2 conducting.
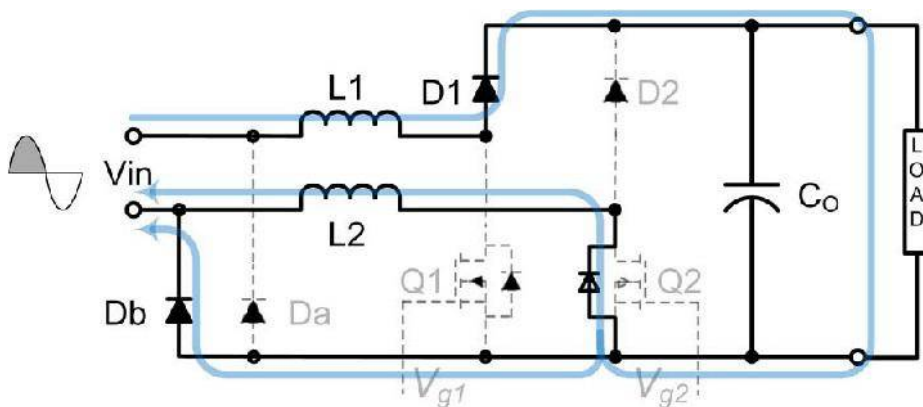
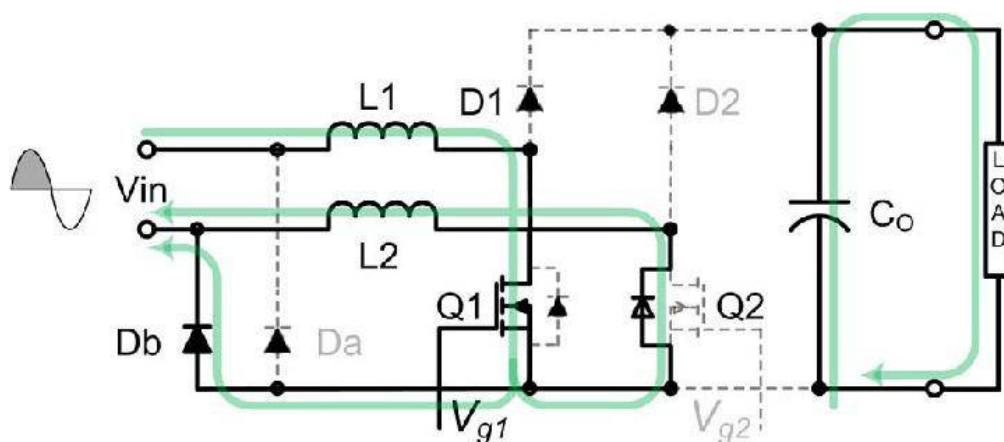Figure 5: Interval 2: Q1 on, body diode of Q2 conducting.

Figure 6: Interval 4: Q1 oand Q2 on.

Interval 1 [t_0 t_1]: At t_0, Q1/ Q2 are o , as shown in Fig.4.5. During this interval, the energy stored in L1 and L2 is released to the output through L1, D1, partially Dq2, L2, and Db.

Interval 2 [t_1 t_2]: At t1, Q1 is on, and Q2 is o , as shown in Fig.4.6 During this interval, the current in series inductances L1 and L2 continues to increase linearly and store the energy in these inductors. The energy stored in Co provides energy to the load. The return current is split only between Db and Dq2.

Interval 3 [t_2 t_3]: At t2, Q1/Q2 are o again, and interval 1 is repeated, as shown in Fig.4.5. During this interval, the current in series inductances L1 and L2 decreases linearly, and the energy in these inductors are released. The energy stored in L1 and L2 is released to the output through L1, D1, partially Dq2, L2, and Db.

Interval 4 [t_3 t_4]: At t3, Q1 is o , and Q2 is on, as shown in Fig.4.7 During this interval, the energy stored in L1 and L2 is released to the output through L1, D1, partially Q2, Dq2, L2, and Db. The operation of the converter during the negative input voltage half-cycle is similar to the operation of the converter during the positive input voltage half-cycle.

70 kHz switching frequency, 240 V input, and 3300 W load for benchmark conventional boost and interleaved boost converters and the proposed PSSB boost converter. The operation of the converter during the negative input voltage half-cycle is similar to the operation of the converter during the positive input voltage half-cycle.
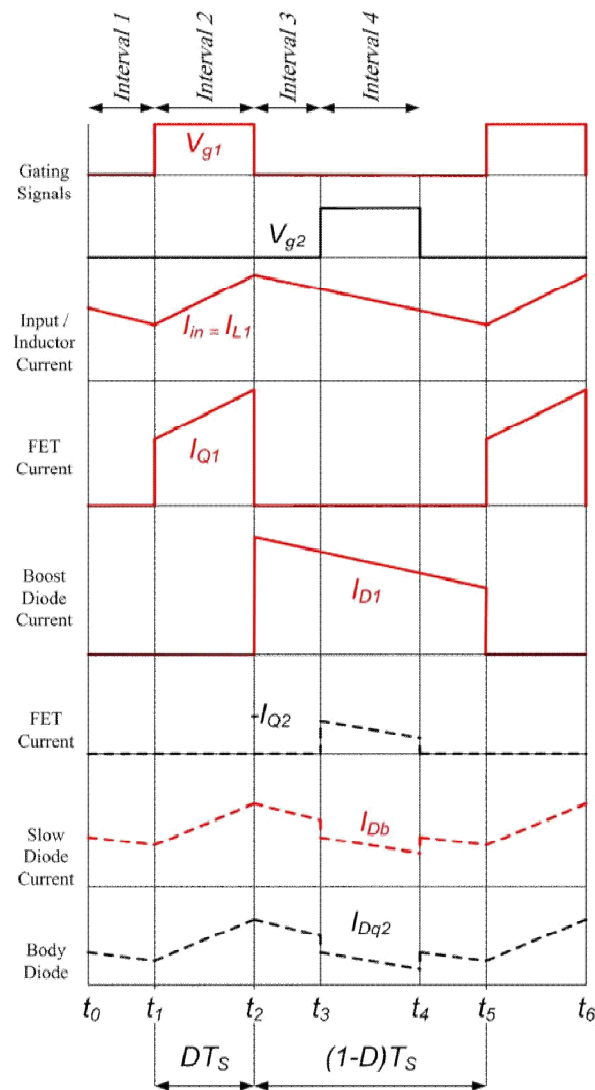

Figure 7: PSSB boost converter steady-state waveforms for D < 0:5.

Interval 3 [t_2 t_3]: At t2, Q1/Q2 are on again, and interval 1 is repeated, as shown in Fig.4.1. During this interval, the current in series inductances L1 and L2 increases linearly and stores the energy in these inductors. The return current is again split among Db, Dq2, and Q2.

Interval 4 [t3-t4]: At t3, Q1 is o , and Q2 is on, as shown in Fig.4.3. During this interval, the energy stored in L1 and L2 is released to the output through L1, D1, partially Q2, Dq2, L2, and Db.

Simulation for the Phase Shifted Semi bridge-less PFC Converter

The simulation prepared for the proposed topology in MATLAB is shown below

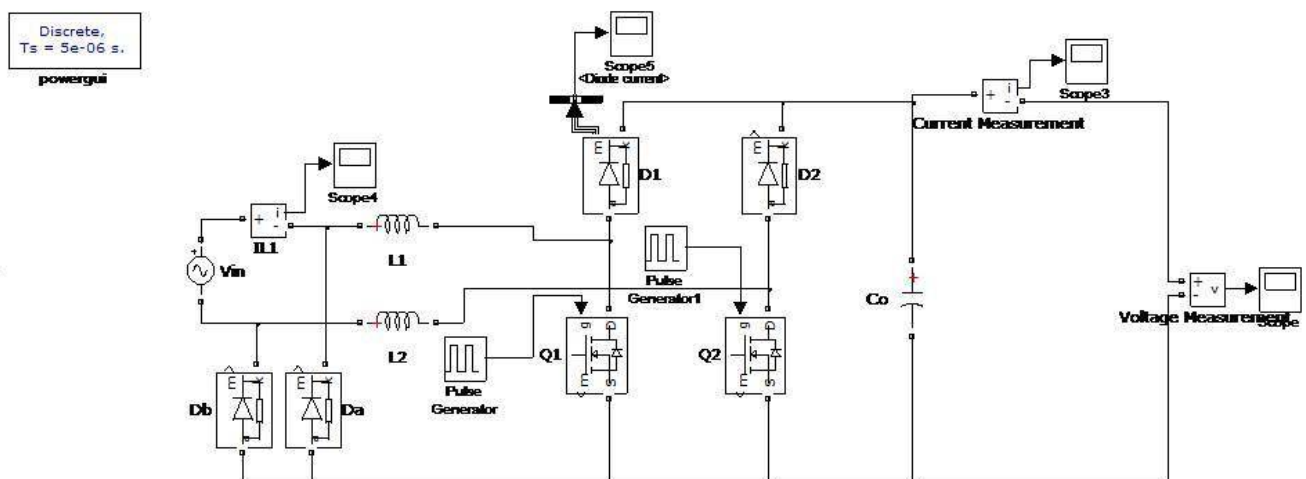It shows the proposed semi-bridgeless converter in open loop.

Figure 8: Simulation for The Phase Shifted Semi-bridgeless PFC Converter open loop

Advancement and modification after projectstage one.

Control topology for The Phase Shifted Semi Bridge-less PFC Converter

Schematic diagram for The Phase Shifted Semi Bridge-less PFC Converter

The block diagram for the proposed topology is shown below g. It shows the proposed semi-bridgeless converter control topology.
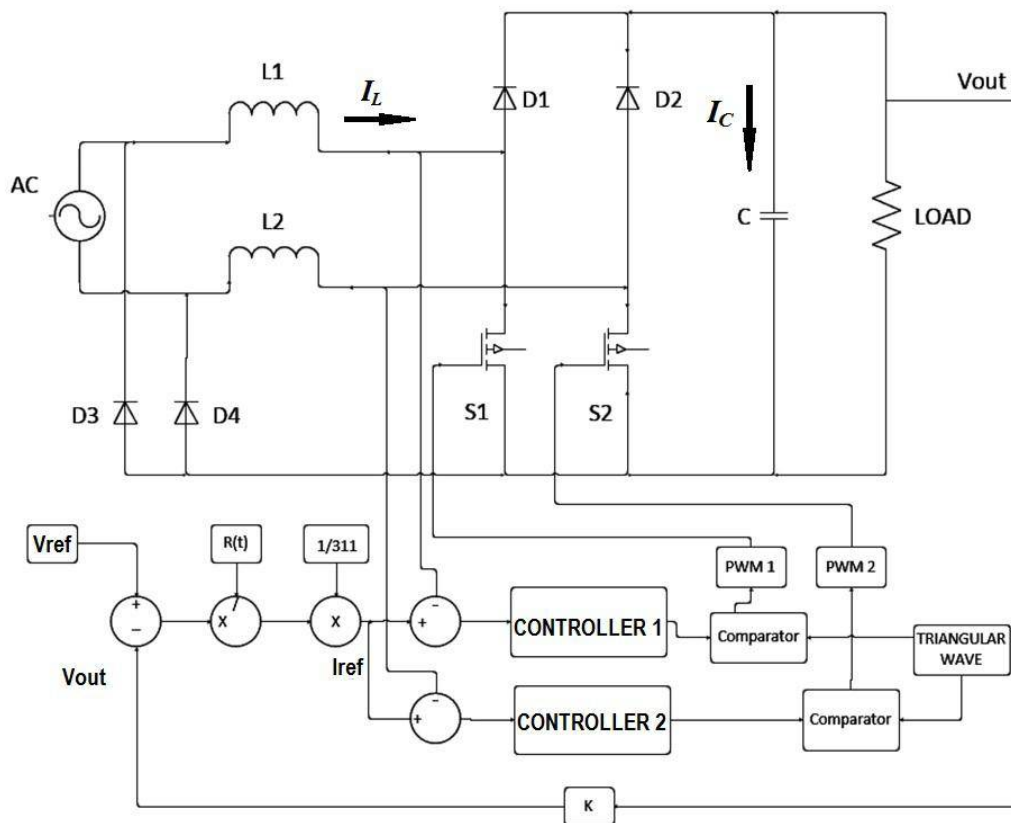
Figure 9: Schematic diagram for The Phase Shifted Semi bridgeless PFC Con-verter in closed loop.

CONTROL STRATEGY FOR PROPOSEDTOPOLOGY.

The control strategy of Boost PFC AC-DC Converter is designed in such a way that, rst it calculates the error between the reference and the output voltage and then this DC value is converted to the reference current that follows the input voltage by multiplying it with the recti ed sinusoidal wave and dividing it with the load resistance. Now this reference current is then subtracted from the actual inductor current to get an error, which is then fed to the controller to achieve our goal of tracking. Fig. 2 is the schematic diagram of Boost PFC with Diode Bridge and controller. In equation (1) PI controller is shown which is applied on the error obtained by subtraction of reference current iref from inductor current iL. In equation (2) the reference current iref waveform is generat ed using required output DC voltage, connected load and the sinusoidal waveform of AC voltage. Vref is the desired output voltage of the converter and Vo is the actual output volt age. The variable resistive load is denoted by R(t) and k1,k2 are the gains.

$$u = Kp(iref - iL) + Ki\int(iref - iL)dt$$

$$i\,ref = \frac{(Vref - k1Vo)}{}|\sin(\omega t)|\,k\,2\,R\,(t)$$

As output of the controller has to switch the power electronic switch of boost converter so we have to convert u into PWM. In this paper, xed frequency Sinu-soidal PWM (SPWM) is used.As this converter is designed for variable switching load so we have to observe the value of load. As the equation of controller totally depend upon the generation

of reference signal and reference signal depends upon connected load so value of load must be known. The load observer can be described as:

$$R(t) = \frac{V_{ref}}{I_o}$$

Io

Vref is reference dc voltage and Io is defined as:

$$I_o = (i_L - i_C)u$$

Simulation for the Phase Shifted Semi bridge-less PFC Converter

The simulation prepared for the proposed topology in MATLAB is shown below g..

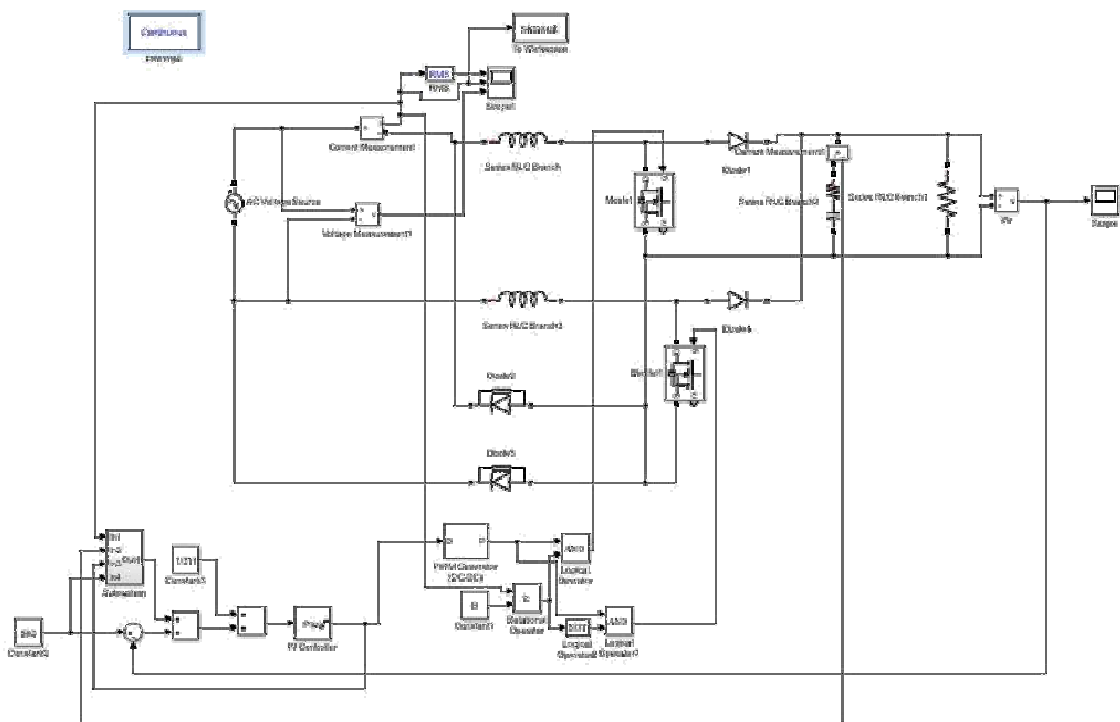It shows the proposed semi-bridgeless converter in closed loop.

Figure 10: Simulation for the Phase Shifted Semi-bridgeless PFC Converter

III. MERITS OF THE TECHNIQUE

The salient features of the method are given as follows

1.   In view of increasing applications, these AC-DC converters are being developed in single-stage to improve power quality, reduced number of components and high e ciency. Moreover, due to strict requirements of improved power quality at input AC mains several standards have been developed and are enforced on the consumers.

2.   However, power quality at AC mains can be improved using lters in existing installations but it increases cost, size, weight, and losses in the system. These prob-lems can be avoided using newly developed single-stage improved power qualityAC-DC converters.

3.   Moreover, this newbreed of single stage converters is being reported in new books, seminars, and many recent publications. Therefore, it is considered relevant to present a comprehensive state of art on the improved power quality AC-DC con-verters with HF transformer isolation for the bene ts of practice, application, and design engineers using them in wide varying applications ranging from few Watts to several kWs.

IV. CONCLUSION

The converter features high e ciency at light-load and low-line conditions, which is critical to minimize the charger size, cost, charging time, and amount and cost of electricity drawn from the utility. Experimental results will prove that the converter is able to achieve a high PF grater than 0.9 and a low input current distortion (THD less than 20 percent). A control scheme is also proposed for the converter. It can be realized by simple operational ampli ers and digital logic gates, and with the help of micro-controller. The distinctive features of this converter are favorable for future high-frequency ac power transfer system operating in the range from a few hundred kHz to the MHz range.

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