



An FPGA-Based Design of an Intelligent On-Chip Sensor Network Monitoring and Control

Tayyab Unnissa Begum¹, E. Shilpa², R. Surender Reddy³

Assistant Professor, Department of ECE, Lords Institute of Engineering and Technology, Telangana, India^{1,2,3}

ABSTRACT: This paper proposes different low-stage micro architectural designs and frameworks for actual-time monitoring and efficient control of on-chip sensor network for field programmable gate arrays (FPGAs). The most important targets are to design low cost, cheap, and incredibly correct monitoring and control mechanism utilizing self-sufficient sensor nodes and to dynamically reconfigure control of on-chip sensor networks via FPGAs. With the aid of accumulating dynamic and real-time monitoring parameters corresponding to voltage and temperature, the process turns into self-aware and is capable to beef up the utilization of FPGA resources and power consumption. The FPGA synthesis, place and route, and implementation have been performed for the proposed design. The results after synthesis and implementation show a significant low utilization of FPGA logic assets and efficient power consumption of all on-chip sensor add-ons compared with earlier techniques. The proposed design technique and framework will assist network engineers and system designers by providing flexible and efficient real-time monitoring and control design of large and complex on-chip sensor networks and remote-sensing applications.

KEYWORDS: on-chip sensor network, FPGA synthesis, Embedded FPGA

I. INTRODUCTION

The complexity imposed via on-chip sensor network monitoring and control increases with the scalability of the on-chip sensor network. Hence, there may be the need to have an intelligent and trustworthy low-stage design of smart monitoring and control methods making use of self-reliant sensor agents. Considering different runtime physical parameters need to be monitored, the need for correct and effective sensor conversation mechanisms is very important to ensure dependable monitoring and control of difficult on-chip sensor network environment. This method also entails the design of low power and high-speed circuits for effective and trustworthy network monitoring and control. The use of field programmable gate arrays (FPGAs) for self-sufficient sensor network monitoring and manipulate is an exciting research domain in which low FPGA logic utilization, low energy consumption, and accurate sensor readings are the fundamental metrics for analysis [1–5]. An autonomous sensor network is specific software for system monitoring, which consists of a couple of add-ons equivalent to a transducer, conditioning circuits, processing items, and data communication.

The foremost services of a sensor network are monitoring, collecting runtime ambient parameters, environmental adaptation, and making informed decisions concerning the located manipulate parameters [6–10]. As the flexibility and reliability of FPGAs broaden, self-sustaining sensor nodes can also be embedded in FPGA to measure different runtime parameters. However, designing a sensor network on FPGA is an extraordinarily complicated venture to reap in a short while on the grounds that designers are constrained to do beyond the FPGA company design specification. In a similar fashion, the degree of complexity as good as sophistication of design automation contained in the FPGA makes it elaborate for designers to tweak the FPGA circuitry to design and enforce sensor networks [4, 5]. The on-chip sensor network runtime parameters corresponding to voltage, current, and go speak noise are used in controlling and monitoring data from the on-chip sensor network environment. Thus, as the alerts are transmitted inside the good judgment blocks, they come across delays. This lengthen factor of the good judgment circuit will have to be minimized. As a result, using FPGA to implement sensor networks can be an effective answer for a riskless on-chip sensor network packet transmission and retransmission scheme due to the fact that common sense and imperative-route delays in

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 10, October 2016

FPGAs are minimal. Several approaches to beat these barriers comprise the use of feedback control method [5, 6, 11–14].

As defined by the IEEE 1451 standard, a smart transducer is an intelligent system that provides enhanced capability beyond sensing and provides a mechanism for control of the sensed information. This feature provides a means of combining transducers for different applications in a controlled network environment with a high level of efficiency and reliability. Furthermore, the IEEE 1451 architecture provides functionalities such as self-diagnosis, self-description, self-identification, self-calibration, data processing, location awareness, and time awareness. The various components of the IEEE 1451 smart transducer architecture are shown in Figure 1. The network capable application processor (NCAP) subsystem provides the functionality for application processing and network communication mechanism between the sensors and actuators. The TI module subsystem is composed of a transducer signal conditioning and data conversion, which consists of a number of sensors and actuators. The TI provides communication methods and algorithms for efficient transmission of sensed data. Finally, the NI provides a means of communication between the NCAP and the outside devices or networks [7–10].

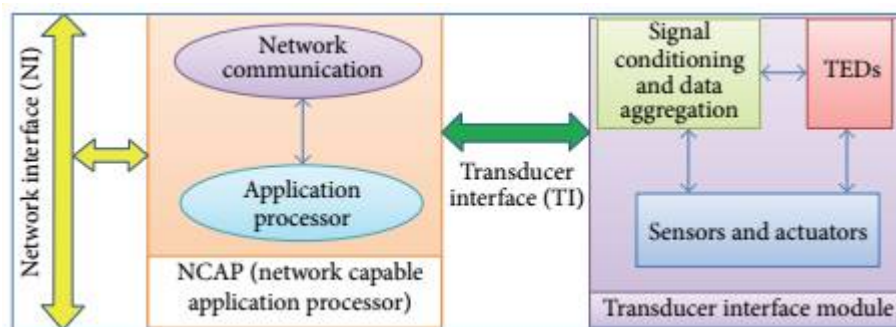


Figure 1: IEEE 1451 standard for smart TI [7]

II. RELATED WORK

Internet monitoring is one of the original techniques for far flung monitoring. Many researchers have worked in subject of web based remote monitoring. (Saito et al., 2000) developed home gateway method for interconnecting home network along with IEEE 1394 AV community and X10 vigor line home automation network with web. This supplied remote access services from internet for digital AV appliances like Digital Video digital, Digital VCR linked to IEEE 1394 community and home equipment like television, desk lamp, electric fan linked to X10 controller .

(Al-Khateeb et al., 2009) used X10 controller interfaced through serial port to PC server for control of devices. The Common Gateway Interface (CGI) is used to interface between the browser and the X10 protocol via http connection. The server executes CGI programs in order to satisfy a particular request from the browser, which expresses its request using the http.

(Peng Liu et al., 2007) developed model of web services based email extension for remote monitoring of embedded systems which integrates web services into emails. It uses a general purpose email messaging framework to connect devices and manipulators. This low cost model fits for systems with low connection bandwidth, small data transportation volume and non-real-time control, e.g., monitoring of home appliances and remote meter-reading.

(Tan and Soy, 2002) developed a system for controlling home electrical appliances over the Internet by using Bluetooth wireless technology to provide a link from the appliance to the Internet and Wireless Application Protocol (WAP) to provide a data link between the Internet and a mobile phone. However, technical details relating controller are not revealed.



International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 10, October 2016

(Nikolova et al., 2002) demonstrated that the control of home appliances can be extended beyond the home network to wireless mobile networks without any modification in the network specifications. This was accomplished by developing and implementing a HAVi (Home Audio Video Interoperability) - WAP UI gateway that intermediates between a wired home network and a wireless communication network using HAVi and WAP specifications, respectively. The gateway use both pull and push technologies, improves the network integration and provides opportunities for developing applications that combine mobile devices with home network devices.

(Yen-Shin Lai et al., 2002) developed an Internet-based monitoring and control of fuzzy controlled inverter for air conditioning system. The system consists of client/server, programmable logic controller, D/A modules, inverters, induction motors and the temperature sensing modules. The client accepts the command from the user and can also access the database created in server, using Internet Explorer (IE) Browser. The server performs function of fuzzy logic control, communication interface between server and PLC, and receiving command from client. Furthermore, the server also creates a database of the sensed temperature, speed of inverter-controlled motor drives, and reference command.

(Ximin et al., 2005) designed and implemented an Internet home automation system. The design uses an embedded controller based on C8051F005 microcontroller which is connected to a PCbased home Web server via RS232 serial port. The home appliances are connected to the input/output ports and the sensors are connected to the analog/digital converter channels of the embedded controller. The software of the system is based on the combination of Keil C, Java Server Pages, and JavaBeans, and dynamic DNS service (DDNS) client. Password protection is used to block the unauthorized user from accessing to the server.

(ColakIlhami et al., 2008) developed Internet controlled Heating Ventilation Air Conditioning (HVAC) system. The system can be controlled by three different units (web based remote control, remote control by hand-held device and keypad control mounted on AC). The hardware system of AC is controlled by PIC16F877 microcontroller. A DAQ board inserted into PCI bus of web server is used to control system over web. User is able to access system parameters over web by logging and setting parameters on forms available on main control page. User submits forms to web server having CGI program which performs requested tasks and reports status of system operation. The current operational parameters of the system are measured by microcontroller and displayed on LCD. Using web camera focused on LCD, these parameters are monitored online by client PC.

(Chen Chao et al., 2009) developed a remote wireless monitoring system for off grid Wind turbine based on the GPRS and the Internet. The remote monitoring system is made up of three parts: controlling terminal, central monitoring computer and communication network. Controlling terminal consists of microcontroller ARM7 LM3S1138, data acquisition module and GPRS communication module WAVECOM Q2406B connected to ARM7 system using serial port. GPRS module sends parameters relating wind turbine to central monitoring computer. The client can access central monitoring computer server through Internet and know parameters of different wind turbines.

(Kumari and Malleswaran, 2010) developed real time based equipment condition monitoring and controlling system using embedded web based technology which directly connects the equipment to network as a node. The embedded system consists of ARM7 based LPC 2148 microcontroller board, A/D, signal conditioning, sensors, and communications interface. The function of web based system is to collect the real time data information of the on-site equipment and remotely send the data in the form of user defined data transmission style. The remote Computer collects the data and running status through the network and provides the comparison on the historical data. If the parameter value is different from the original set value, the corrected signal is sent to the control unit. The embedded remote monitoring system completes the data Collection in the embedded platform and provides the data to remote host through the TCP/IP protocol from Web server. It creates condition to realize unattended management through carrying out remote data communication. The MCU S3C44B0, which utilize 32-bit ARM kernel, is adopted in intelligent monitoring terminal. μ Clinux operating system is chosen as the software core of embedded system. It offers self-contained TCP/IP network protocol module and provides strong support for embedded Internet technology.

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 10, October 2016

III. PROPOSED SYSTEM

The on-chip sensor network must consider and address the following fundamental issues in a controlled loop system. To address these issues, there is the need to have an efficient and reliable monitoring and control infrastructure that will provide all the needed design methodology and framework to achieve the stated goals and objectives. Figure 2 shows an intelligent monitoring and control system for on-chip sensor network using autonomous sensor agents. It shows the data transfer among different nodes in the system, that is, from the sensors to the controller and from the controller to the actuators.

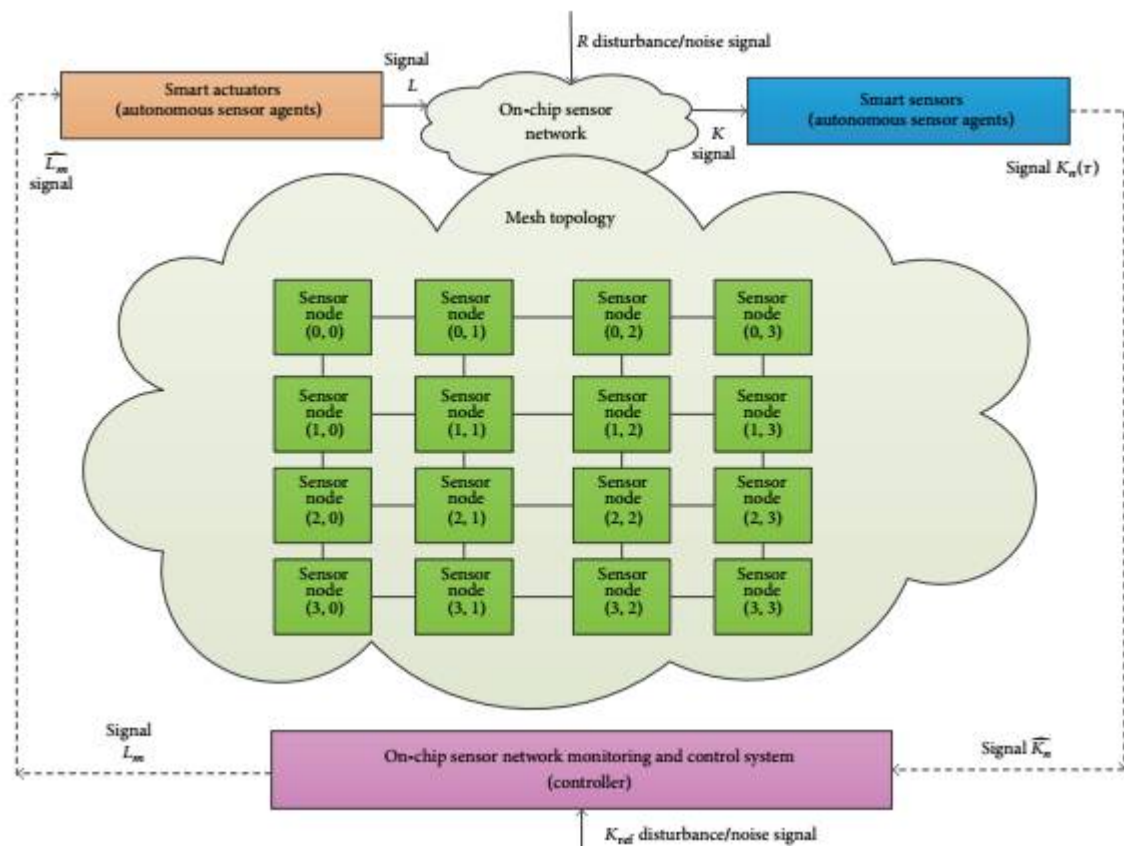


Figure 2: On-chip sensor network monitoring and control system using autonomous sensor agents.

Figure 2 shows single-headed arrow lines representing continuous time signals, whereas the dashed arrow lines represent the data transmission links at a given transmission time, for example, τh , for $h = 0, 1, 2, \dots$. During the transmission of the sensor data, the process produces a time delay that must be controlled and monitored. Similarly, time is another issue that needs to be considered: for example, at what time interval the communication is needed and required. The transmission of the sensor data is constrained to a small number of bit rates, which implies that the values of signals transmitted over the on-chip sensor network are constrained to a fixed bit length. Therefore, the monitoring and control system should ensure reliable and efficient communication at different time instances [36–38]. On the basis of these limitations, FPGA based design and implementation of an intelligent on-chip sensor network monitoring and control are essential. Hence, our proposed design methodology provides a better solution for on-chip sensor network monitoring and control using autonomous sensor agents.

This part grants the design methodology of the proposed on-chip sensor network monitoring and control method with dynamic reconfigurable capabilities. The proposed design detects runtime ambient parameters and communicates the

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 10, October 2016

sensed data to the monitoring and manipulate hardware unit. Fig.3 shows the architectural design of the proposed monitoring and manipulate process utilising self-sufficient sensor agents that dwell in the NI to experience and file more than a few parameter values to the hardware controller for onward evaluation and processing. The structure is a mesh community that is good fitted to on-chip sensor die structure. It includes 12 nodes (gateway) and IP cores. The NI presents a means of communication amongst the sensors and actuators, community nodes, and hardware reveal controllers. At each NI, three wise sensors are set up, namely, voltage, thermal, and temperature sensors. These sensors continuously sense and transmit the sensed data to the hardware controller that then techniques the data and supplies the necessary movements to maintain the approach in a soft and healthy condition. The sensors keep in touch the sensed data through a common protocol.

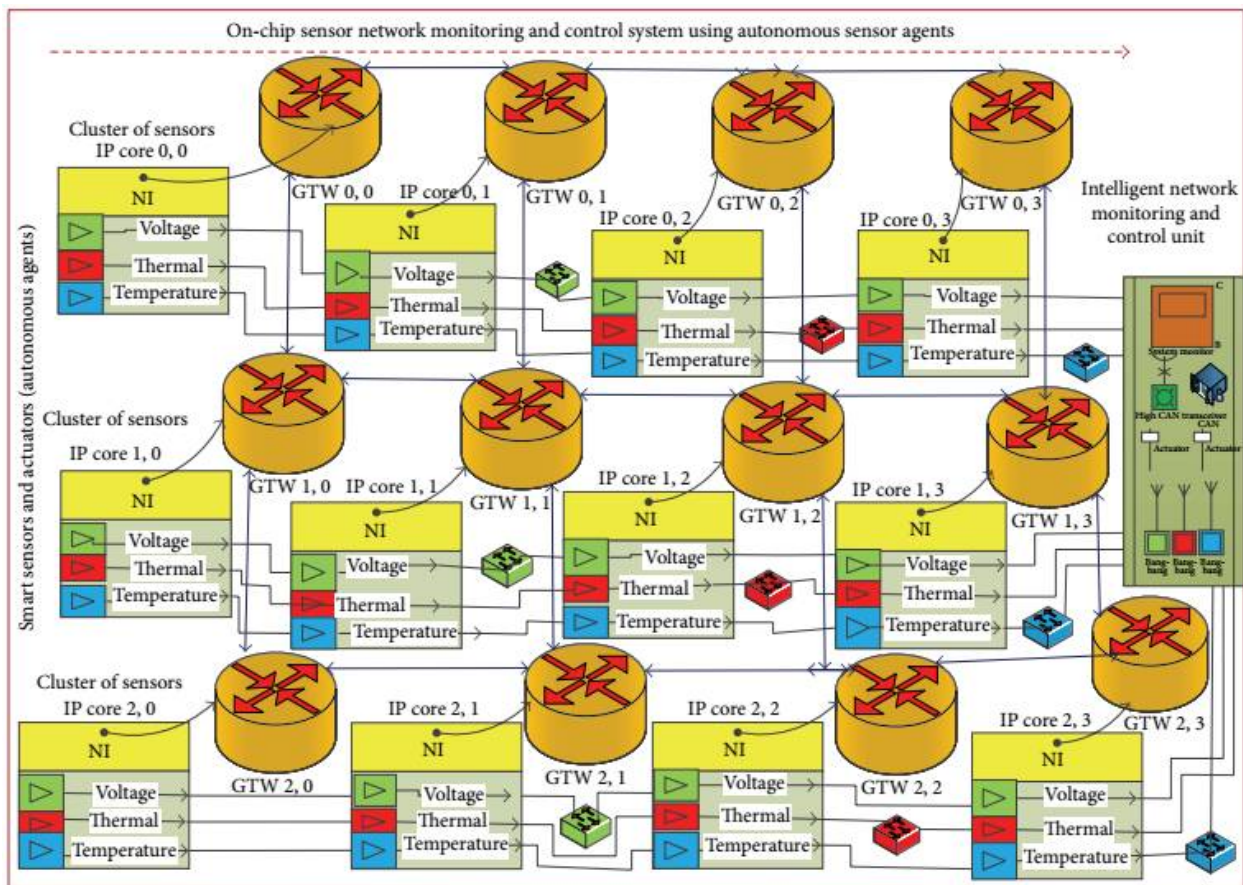


Figure 3: Proposed on-chip sensor network monitoring and control system using autonomous sensor agents on 4 x 3 mesh architecture

The temperature sensors measure the temperature variations to ensure that the system temperature does not exceed a certain threshold. The sensed data from the sensors are aggregated between four or more temperature sensors in different NIs. These temperature sensors form a cluster of sensors, and a cluster head (sub controller) among them is ready to collect and mix the sensed data from all sensors within the cluster and transmit them to the hardware monitoring and control approach for additional processing. The thermal sensors measure the quantity of heat dissipation as a result of the on-chip sensor cross talk noise and the data transmission and retransmission operations. For the thermal sensor operation, the process is much like that of the temperature sensors. The place four or more thermal sensors kind a cluster, and the cluster head (sub controller) transmits the aggregated sensed information to the on-chip display controller hardware. The voltage sensors measure the voltage variants on account of the present and resistance on the on-chip logic



International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 10, October 2016

and the analog circuits. These sensors determine any transient and variant in the voltage drop throughout different accessories within the on-chip sensor network. Right here, 4 or extra voltage sensors in different NIs can form a cluster, and their sensed voltage input data are then mixed for transmission to the monitoring and manipulate unit. This procedure will be certain gentle and safe monitoring and control of the whole on-chip sensor network.

IV. CONCLUSION

In this study paper, we now have proposed the design of efficient and excessive-speed circuit for real-time monitoring and manage of on-chip sensor network for FPGAs. We developed the autonomous sensor agents carried out in the FPGA based NI to be dynamically configured and to be in contact the dynamic ambient parameter alterations to the monitoring and manipulate hardware unit. The perfect goal of this study is to design low priced, low energy, and high accuracy actual-time monitoring mechanism making use of self-sufficient sensor agents as well as a dynamic reconfiguration manipulate of on-chip sensor community environment utilising FPGAs. We presented a unique design system and a case be taught to demonstrate the applicability of the proposed approach.

REFERENCES

- [1] C. Chu, Y. Ren, X. Liu, Y. Zheng, and W. Fang, "An efficiency multiplexing scheme and improved sampling method for multichannel data acquisition system," International Journal of Distributed Sensor Networks, vol. 2015, Article ID 626307, 9 pages, 2015.
- [2] M. D. R. Perera, R. G. N. Meegama, and M. K. Jayananda, "FPGA based single chip solution with 1-wire protocol for the design of smart sensor nodes," Journal of Sensors, vol. 2014, Article ID 125874, 11 pages, 2014.
- [3] J. Echanobe, I. del Campo, K. Basterretxea, M. V. Martinez, and F. Doctor, "An FPGA-based multiprocessor-architecture for intelligent environments," Microprocessors and Microsystems, vol. 38, no. 7, pp. 730–740, 2014.
- [4] C. G. Osuna, P. Ituero, and M. Lopez-Vallejo, "A self-timed 'multipurpose delay sensor for Field Programmable Gate Arrays (FPGAs)," Sensors, vol. 14, no. 1, pp. 129–143, 2014.
- [5] J. J. L. Franco, E. Boemo, E. Castillo, and L. Parrilla, "Ring oscillators as thermal sensors in FPGAs: experiments in low voltage," in Proceedings of the 6th Southern Programmable Logic Conference (SPL '10), pp. 133–137, Ipojula, Brizal, March 2010.
- [6] R. K. Umanath, Designing Next Generation Low Power Autonomous Sensor Nodes Using Systems-on-Chip based Solutions, Cypress Semiconductor, Published in EE Times Design, 2011.
- [7] E. Y. Song and K. Lee, "Understanding IEEE 1451-networked smart transducer interface standard—what is a smart transducer?" IEEE Instrumentation and Measurement Magazine, vol. 11, no. 2, pp. 11–17, 2008.
- [8] W. Elmenreich and S. Pizek, "Smart Transducers Principles Communications and Configurations," <http://www.vmars.tuwien.ac.at/~wilfried/papers/2003/rr-10-2003.pdf>.
- [9] H. Kopetz and T. Wien, "OMG smart transducer specification (II)," OMG Standard, 2003, <http://www.omg.org/news/meetings/workshops/RT2003Manual/Tutorials/T4SmartTransducersKopetzP2.pdf>.
- [10] Standard for a Smart Transducer Interface for Sensors and Actuators, "Common functions, communication protocols and Transducer Electronic Data Sheet (TEDs) formats," IEEE STD1451.0-2007, IEEE Instrumentation and Measurement Society, TC-9, the Institute of Electrical and Electronics Engineers, inc, New York, NY, USA, 2007.
- [11] V. Mattoli, A. Mondini, B. Mazzolai, G. Ferri, and P. Dario, "A universal intelligent system-on-chip based sensor interface," Sensors, vol. 10, no. 8, pp. 7716–7747, 2010.
- [12] J. H. Huijsing, F. R. Riedijk, and G. Van der Horn, "Developments in integrated smart sensors," Sensors and Actuators: A. Physical, vol. 43, no. 1–3, pp. 276–288, 1994.
- [13] G. Kornaros and D. Pnevmatikatos, "A survey and taxonomy of on-chip, monitoring of multi-core systems-on-chip," ACM Transactions on Design Automation of Electronic Systems, vol. 18, no. 2, article 17, 2013.
- [14] G. J. Garcia, C. A. Jara, J. Pomares, A. Alabdo, L. M. Poggi, and F. Torres, "A survey on FPGA-based sensor systems: towards intelligent and reconfigurable low-power sensors for computer vision, control and signal processing," Sensors, vol. 14, no. 4, pp. 6247–6278, 2014.

BIOGRAPHY



Tayyab Unnissa Begum presently, working as Assistant Professor, Department of ECE, Lords Institute of Engineering and Technology, Telangana, India. Her research interests are in area of low power VLSI, FPGA architectures.



ISSN(Online): 2320-9801
ISSN (Print) : 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 10, October 2016



E. Shilpa presently,working as Assistant Professor, Department of ECE, Lords Institute of Engineering and Technology, Telangana, India. Her research interests are in Microwave engineering, radar engineering and wireless mobile communications.



R. Surender Reddy presently,working as Assistant Professor, Department of ECE, Lords Institute of Engineering and Technology, Telangana, India. His research interests are in area of low power VLSI, DSP and FPGA architectures.