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A Review on Implementation of Virtual ARM Processor Using FPGA

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ABSTRACT: We know that the well known companies like Samsung, Nokia, Micromax develop their own processor ICs. It is very cost efficient to develop ICs in lacks and crores of amount as they require the with their own decided parameters, requirements. But if one wants to design a single IC , it is very cost effective. For single IC, it is not convenient to spend a lot of time for design purpose, manufacturing purpose, testing fault finding and repairing purpose. It increses the unit cost, time to market, manpower too. So the alternative is to design the software for it and dumping the code in userfriendly, low end device SPARTAN III. For that we are designing the ARM 7 soft core processor instead of other because it is easy to test the outputs of each functional block of ARM processor. Simulation results are observed for crosschecking the functionality of ARM processor. The functionality of block UART is crosschecked by sending the databits to the FPGA kit and displaying it through blinking the corresponding LEDs. An android application is executed to test functionality of entire ARM processor, the command is send through mobile device to ON/OFF relay**.**

KEYWORDS: FPGA, SpartanIII, UART, VLSI, VHDL.

I. INTRODUCTION

The New Effective technology that enables designers to utilize a FPGA that contains both memory &Logic Block elements. This new FPGA methodology is system on program chip (SOPC) design has advantages having feature like software flexibility, hardware flexibility, reconfigurality, development time& cost, peripheral equipment cost , It has better performance & production cost. Software ARM Processor is implemented specially designed to reduces power consumption & extended battery, operation to achieve high performance small code size. The FPGA based Design provides optical device utilization & adds design flexibility ,adaptabilitythat conserves less board space & system power, reduces time to market. Advantages of implementing the full featured soft core ARM processor with the various application implementation.

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II. PROPOSED WORK

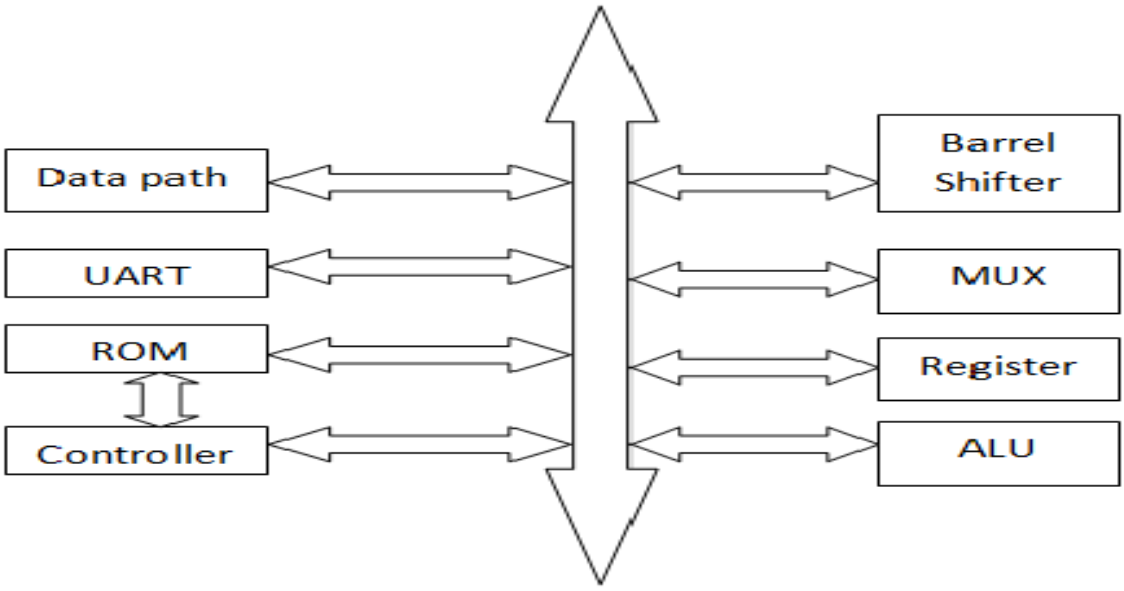

Figure.1 Block Diagram of Proposed System

Block diagram in fig1. Contens the Date path controller , Rom &communication modules are UART& SPI module. The block diagram comprises of

1) UART
2) ROM
3) Controller
4) Register file
5) Barrel shifter
6) ALU

1. UART:The UART or universal Asynchronous Receiver/ Transmitter is most important component in serial communication between computer &low speed peripheral devices like Keyboard ,Mouse Model & with terminal.
2. ROM:Hex code generated using ARM architecture used to test the implemented ARM processor is in the ROM.
3. Comtroller:Generates control signal to flow of data path for execute of instruction given in ROM controller play important role as it controller operation of system.
4. Register File:Register file consist of 10 negligible each of 32 bit length including program counter(PC) , control program status register(CPSR).
5. Barrel shifter :The data path uses barrel shifter to shift any data as per instruction with given amount of shift.
6. ALU:Arithmetic & Logical Unit is used to perform all with addition sub-straction, multiplication, division, logical shift, Right, left operation.

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C. Hardware Description

1) SPARTAN III:

Figure 2: SPARTAN III

Specifications:
1) FPGA: Spartan-3 XC6SLX9 in TQG144 package
2) Flash memory: 16 Mb SPI flash memory (M25P16)
3)100MHz CMOS oscillator
4) USB 2.0 interface for On-board flash programming
5) FPGA configuration via JTAG and USB
6) 8 LEDs and four switches for user defined purposes
7) 70 IOs for user defined purposes
8) On-board voltage regulators for single power rail operation.

2) JTAG Connector:

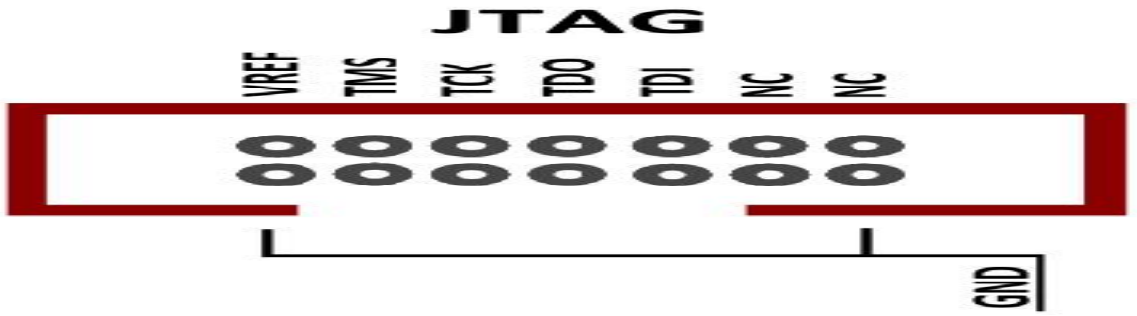

Figure 3:JTAG Connector

Joint Test Action Group (JTAG). It specifies the use of a dedicated debug port implementing a serial communications interface for low-overhead access without requiring direct external access to the system address and data buses.

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III. PROPOSED SYSTEM

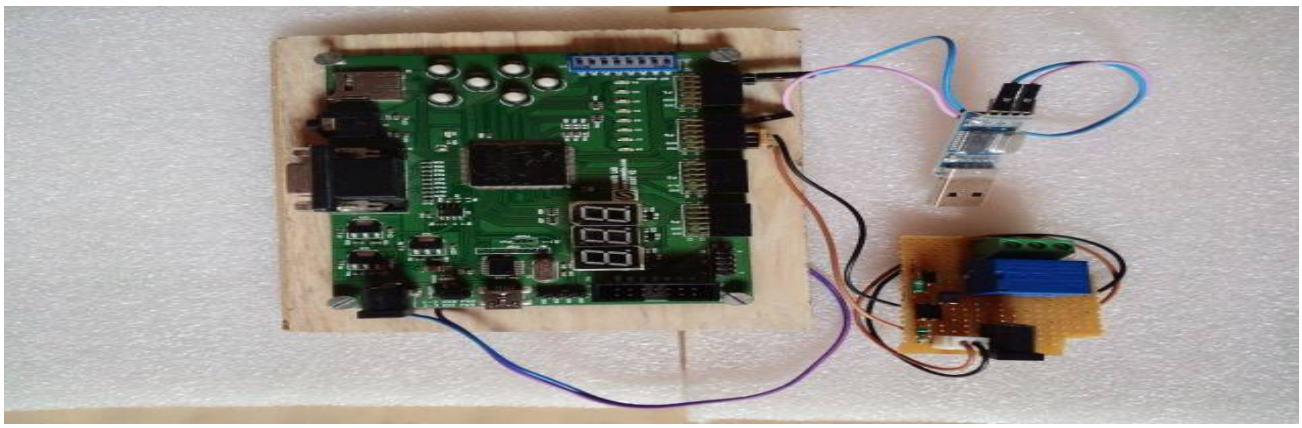

Figure 4: Proposed system

SIMULATION RESULTS

A. **Left barrel shifter**:For **Left barrel shifter**, the input and outputs are given bellow and are clearly shown in fig,

- Input data= 10100110
- Shift= 001
- Output data= 01001100

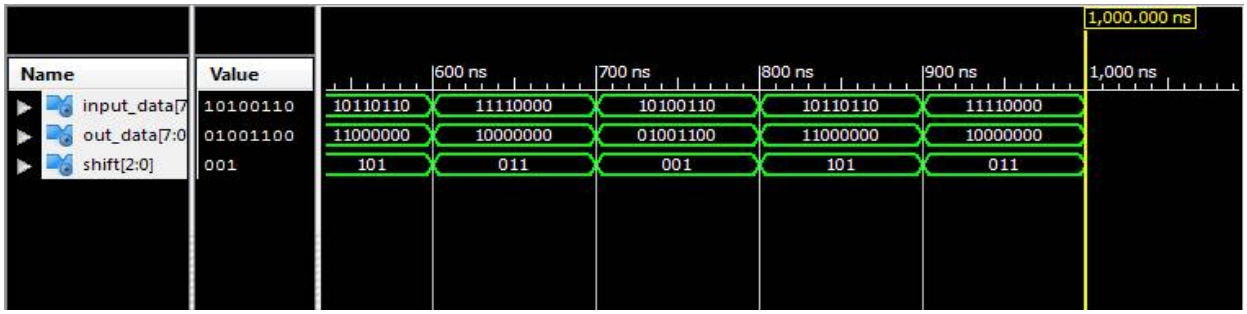

Figure 5:Left Barrel Shifter

B. **Right barrel shifter**:For **Right barrel shifter**, the input and outputs are given bellow and are clearly shown in fig,

- Input data= 11010001
- Shift= 010
- Output data= 001100100

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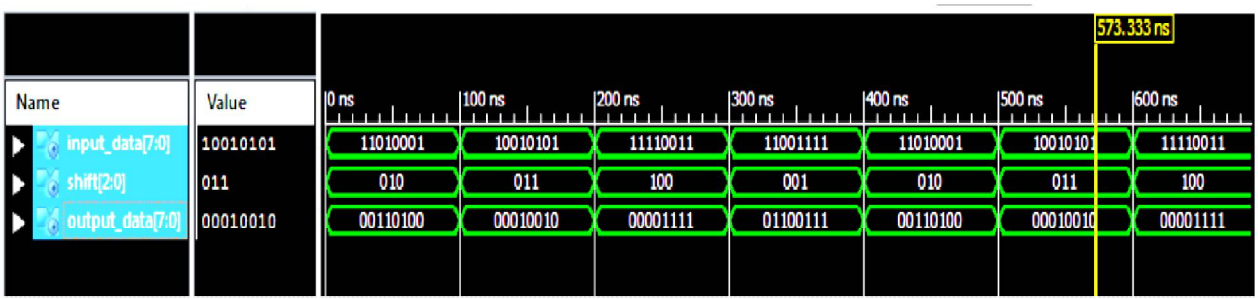

Figure 6:Right Barrel Shifter

C. **Left rotator:**For **left rotator**, the input and outputs are given bellow and are clearly shown in fig,

- Input data= 11010001
- Rotate= 010
- Output data= 01000111

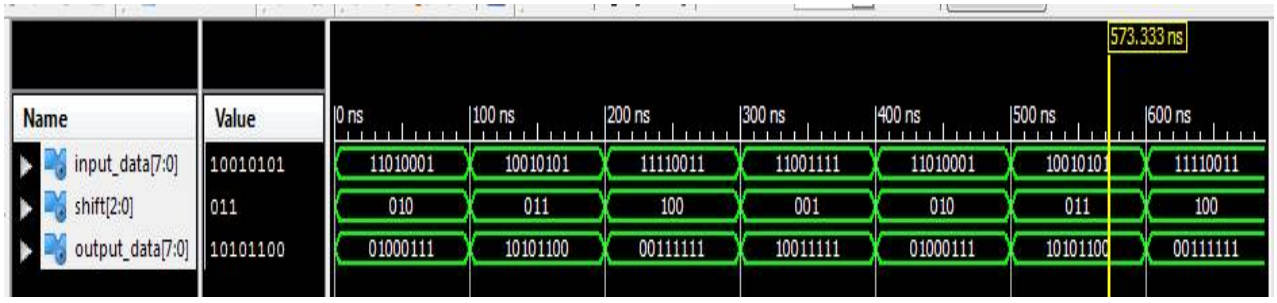

Figure 7:Left Rotator

D. **Right rotator:**For **Right rotator**, the input and outputs are given bellow and are clearly shown in fig,

- Input data= 11010001
- Rotate= 010
- Output data= 01110100

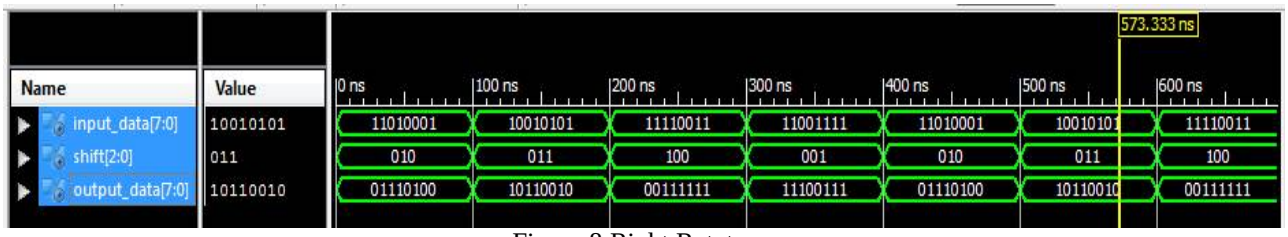

Figure 8:Right Rotator

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E. Synthesis Report:

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	7	704	0%
Number of Slice Flip Flops	3	1408	0%
Number of 4 input LUTs	12	1408	0%
Number of bonded IOBs	22	108	20%

Figure 9: Synthesis Report

IV. APPLICATIONS

1. DSP:For simulation and execution of digital signal in ISE Design Suite14.7. Any digital signal can be simulated using this suite.
2. ASIC prototyping: For executing specific application using ARM processor. It reduces the memory space consumed than that consumed by any other processor and writing code for specific application with suitable memory.
3. Aerospace: Main aim while designing any system is implement design with reduced hardware which can be achieved by FPGA.
4. Industry system monitoring: Virtual ARM processor can be used further for industrial system monitoring, analyzing and future record purpose.
5. It can be used in applications like Medical imaging, Cryptography, Speed recognition, etc.

V. CONCLUSION

In this venture we have built up an android application to associate with Bluetooth module and given the instructions to start the relay, ON/OFF LEDs.A shrewd correspondence system is made with an end goal to achieve complete hardware customization and reduced memory consumption with less i/o pins.The high end FPGA device can be used for Better efficiency verification ARM platform can be Executed with ARM 9, ARM 11 Processor.

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