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FPGA Implementation of Gradient Based Edge Detection Algorithms

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ABSTRACT: Edges are one of the most significant features for image processing and many computer vision applications. Edge detection is one of the classical studies since it is perquisite thing prior to perform any image processing operation. It has provoked interest among research fraternity since several years. Real time image processing applications demand hardware implementation of Edge detection algorithms. In this paper, various gradient based edge detection algorithms such as Robert, Prewitt, Sobel, Canny are implemented on Spartan-3E FPGA. Using Xilinx System Generator (XSG) tool all these edge detection algorithms are designed in MATLAB/Simulink. By eliminating HDL coding, programming file (*.bit file) is generated using hardware co-simulation technique. Designed algorithms are efficiently compiled, synthesized and implemented on Field Programmable Gate Array (FPGA).

KEYWORDS: Image Processing, Edge Detection, XSG, Hardware Co-simulation, Spartan-3E FPGA

I. INTRODUCTION

Over the past decade, the field of image analysis research has undergone a rapid evolution. Image processing now-a-days has various applications in the fields of medical imaging,weather meteorology, computer vision etc. The main objective of image processing is to improve the quality of the images for human interpretationand analysis. Edge detection is always the first step in many image processing algorithms, because it significantly reduces the amount of data and filters out uselessinformation. Edge detection serves as a pre-processing step for many image processing algorithms such as image enhancement, image segmentation, object tracking, object recognitionand image/video coding.Digital image consists of set of pixels with certain value of intensity. Edge can be characterized by sudden change in this intensity levels. Edge defines the object boundaries within the image and occurs when discontinuities present in the pixel values. Inorder to identify these edges from an image various edge detection algorithms are proposed. In this paper, gradient based edge detection techniques such as Robert, Prewitt, Sobel and Canny are discussed.

II. RELATED WORK

Edge detection is a fundamental tool in the field of image processing. Edge indicates sudden change in the intensity level of image pixels [1]. By detecting edges in an image, one can preserve its features and eliminate useless information. In the recent years, especially in the field of Computer Vision, edge detection has been emerged out as a key technique for image processing. Many researches have been going on for the past few years in the field of machine vision. In literature, there are various edge detection algorithms used for this purpose. On the broader scale edge detection techniques can be categorised as Gradient based edge detection and Laplacian based edge detection [2]. Generally, gradient based edge detection techniques are used in many image processing applications. These include various classical operators (such as Robert, Prewitt, Sobel) and Canny algorithm.In this paper, all these gradient based edge detection algorithms are implemented on FPGA hardware by utilizing hardware software co-simulation [3]. The main objective isto implement imageprocessing algorithms applicable to Edge Detection system in a Xilinx FPGA using System Generator for DSP, with a focus on achieving overall high performance, low cost and short development time [4]. FPGAs are generally programmed using hardware description language (HDL) which uses a low level, hardware-oriented programming model to fully exploit their potential performance. Unfortunately, writing thousands of code lines for image processing is impractical and time consuming. So, a tool called Xilinx System Generator (XSG) with graphical interfacing MATLAB-Simulink is used to produce software environment for hardware description [5]. This combination

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of MATLAB-Simulink and Xilinx system generator offers an ideal virtual prototyping environment to quickly test the system. Moreover, the designer does not need to know the details of the hardware description language or have an in-depth knowledge of the board that hosts the FPGA [6], which improves efficiency of learning the use of such complex design systems [7]. After making prototype of design on FPGA, further logic can be implemented further to ASIC. Thus, hardware requirement can be fulfilled and design can be used for real-time applications of image processing.

III. EDGE DETECTION

Edge detection is the process of localizing pixel intensity transitions. The most well-known technique for edge detection is gradient-based. The gradient method looks the edges by finding maximum and minimum in the first derivative of the image. The basic edge detection operator is a matrix area gradient operation that determines the level of variance between different pixels. The edge detection operator is calculated by forming a matrix centred on a pixel chosen as the centre of the matrix area. If the value of this matrix area is above a given threshold, then the middle pixel is classified as an edge.

*A. Robert operator:*The Robert cross operator is used in image processing and computer vision for edge detection. As a differential operator, the idea behind the Robert cross operator is to approximate the gradient of an image through discrete differentiation which is achieved by computing the sum of the squares of the differences between diagonally adjacent pixels.The kernels or masks (as shown in Fig. 1) can be applied separately to the input image, to produce separate measurements of the gradient component in each orientation (Gx and Gy). These can be combined together to find the absolute magnitude of the gradient at each point. An approximate magnitude is computed using:

$$G = |Gx| + |Gy|$$

P_1	P_2
P_3	P_4

(a)

1	0
0	-1

(b)

0	1
-1	0

(c)

Fig. 1: (a) Image Pixels (b) Horizontal Mask (c) Vertical Mask

*B. Prewitt operator:*Prewitt operator provides two masks for detecting edges in horizontal and vertical direction.Mathematically, the gradient of a two-variable function (here, the image intensity function) is at each image point a 2D vector with the components given by the derivatives in the horizontal and vertical directions.

P_1	P_2	P_3
P_4	P_5	P_6
P_7	P_8	P_9

(a)

-1	0	1
-1	0	1
-1	0	1

1	1	1
0	0	0
-1	-1	-1

(b)

-1	0	1
-2	0	2
-1	0	1

1	2	1
0	0	0
-1	-2	-1

(c)

Fig. 2: (a) Input Pixels (b) Prewitt Masks(c) Sobel Masks

*C. Sobel operator:*The Sobel operator is very similar to Prewitt operator except higher weights are assigned to the pixels close to the candidate pixel. These kernels are designed to respond maximally to edges running vertically and horizontally relative to the pixel grid, one kernel for each of the two perpendicular orientations. The kernels can be applied separately to the input image, to produce separate measurements of the gradient component in each orientation.

*D. Canny Algorithm:*The Canny edge detection algorithm is known to many as the optimal edge detector. Canny's intentions were to enhance the many edge detectors already out at the time he started his work. In his paper [8], he followed a list of criteria to improve classical methods of edge detection.1) Low Error Rate: It is important that edges occurring in images should not be missed and there should be no responses to non-edge pixels.2) Localization of Edges: The second criterion is that the edge points should be well localized. In other words, the distance between the edge pixels as found by the detector and the actual edge is to be at a minimum.3) Only One Response to Single Edge: This was

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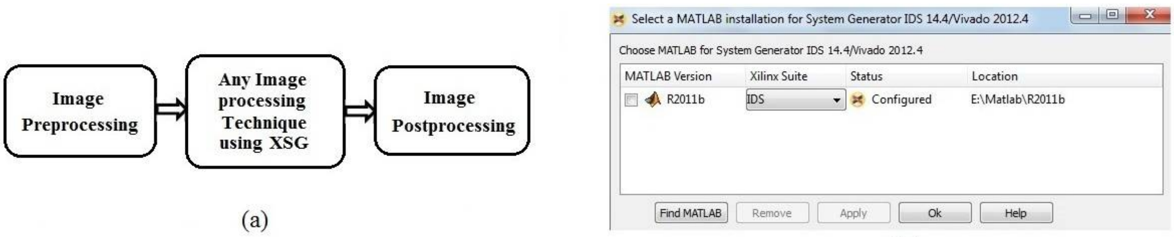
implemented because the first two were not substantial enough to completely eliminate the possibility of multiple responses to an edge.

Based on these criteria, the canny edge detector first smoothened the image to eliminate noise. It then finds the image gradient to highlight regions with high spatial derivatives. The algorithm then tracks along these regions and suppresses any pixel that is not at the maximum (non-maximum suppression). The gradient array is further reduced by hysteresis. Hysteresis is used to track along the remaining pixels that have not been suppressed. Hysteresis uses two thresholds and if the magnitude is below the first threshold, it is set to zero. If the magnitude is above the high threshold, it is made an edge. And if the magnitude is between the two thresholds, then it is set to zero unless there is a path from this pixel to a pixel with a gradient above high threshold.

IV. SYSTEM DEVELOPMENT

A. System Requirement and Design Flow:

In this paper, hardware software co-simulation concept is utilized in order to carry out Edge detection. MATLAB/Simulink along with System generator [9]provides common environment where simultaneously software and hardware results are observed. System generator is configured as shown in Fig. 3(b).System design is mainly divided into three parts as shown in Fig. 3(a) which are explained as follows:



(a) (b)

Fig. 3: (a)System Design Model (b) Configuring MATLAB with System Generator

1. Image Pre-processing Blocks:As an image is two dimensional (2D) array size with R×C where R, C represent the rows and columns of an image respectively. For image processing, image must be converted to one dimensional (1D) vector. Image pre-processing blocks are used to convert 2D image data to 1D arraywhich converts this frame to scalar output samplesat a higher sampling rate.

2. Xilinx System Generator Blocks:All Xilinx blocks are connected between Gateway In and Gateway Out and any image processing technique is applied between those two.Since, Xilinx blocks process on fixed point but the real world signal process on floating point so to convert fixed point to floating point, Gateway In and Gateway Out blocks act as translators. System generator token provides various options for compilation such as Bit-stream, HDL Net-list, NGC Net-list, Hardware Co-simulation, Timing and Power analysis etc.

3. Image Post-processing Blocks:The image post processing blocks are used to convert serial 1D data to the 2D image data. It includes a buffer block which converts scalar samples to frame output at lower sampling rate, followed by convert 1D to 2D, transpose blocks and data type convertor.

Fig. 4(a) shows system generator flow. After configuring MATLAB with system generator, required algorithm is designed using various Xilinx blocks in Simulink environment. Designed algorithm is then compiled using different options. In this paper, hardware co-simulation compilation is utilized for the hardware implementation on Spartan-3E FPGA. Fig. 4(b) indicates described procedure.

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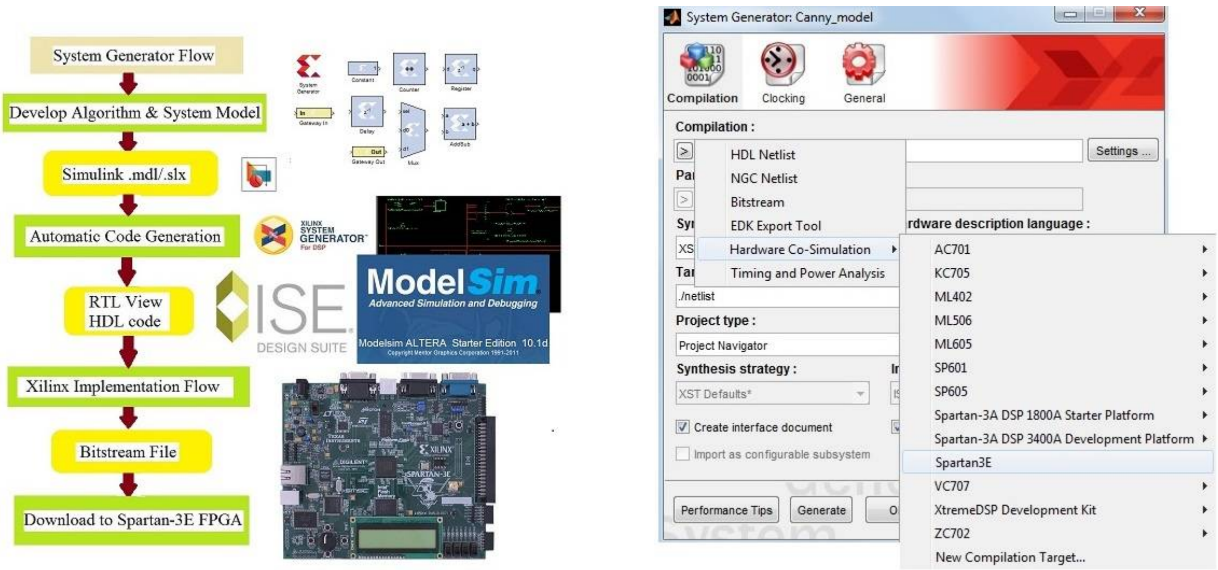


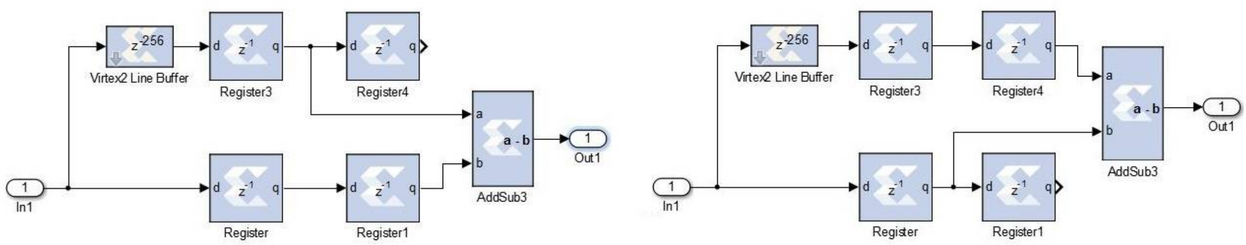
(a) (b)

Fig. 4: (a)System Generator Flow (b) Hardware Co-Simulation Window

B. System Implementation:

1. Robert Gradient Filters:Gradient of image is computed by moving masks for Robert edge detection over an image. Local gradients are used for computed at every point by convolving mask coefficients with pixel. Suppose, p1, p2, p3, p4 are image pixels and Mx, Myare masks for horizontal and vertical gradient filter respectively. Then, formulae used for gradient calculation are given by:

$$|Gx| = |p1 - p4| \quad \text{and} \quad |Gy| = |p2 - p3|$$



(a) (b)

Fig. 5: (a)Robert Horizontal Gradient Filter (b) Robert Vertical Gradient Filter

2. Prewitt Gradient Filters: Gradient of image is computed by moving masks for Prewitt edge detection over an image. Suppose, p1, p2, p3,….p9 are image pixels and Mx, My are masks for horizontal and vertical gradient filter respectively. Then, formulae used for gradient calculation are given by:

$$|Gx| = |(p3 + p6 + p9) - (p1 + p4 + p7)| \text{and} \quad |Gy| = |(p7 + p8 + p9) - (p1 + p2 + p3)|$$

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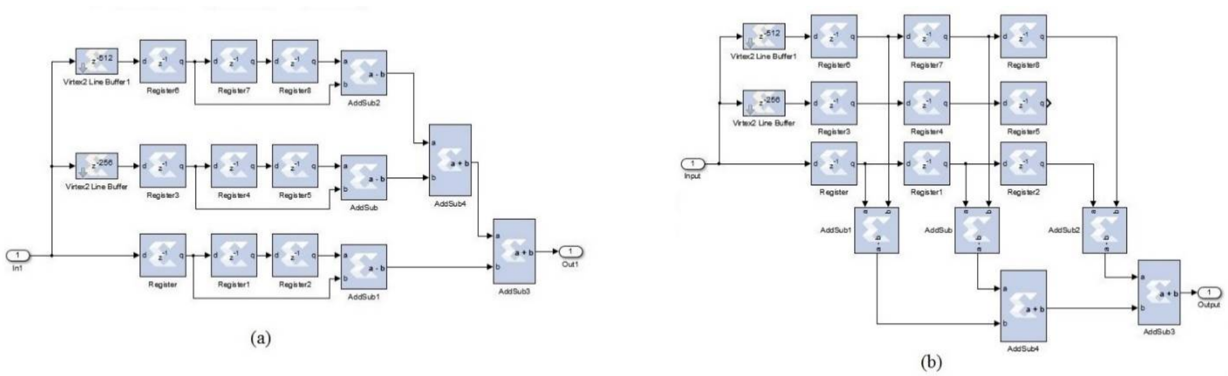

Fig. 6: (a)Prewitt Horizontal Gradient Filter (b) Prewitt Vertical Gradient Filter

3. Sobel Gradient Filters:Gradient of image is computed by moving masks for Sobel edge detection over an image. Suppose, p1, p2, p3,….p9 are image pixels and Mx, My are masks for horizontal and vertical gradient filter respectively. Then, formulae used for gradient calculation are given by:

$$|Gx| = |(p3 + 2*p6 + p9) - (p1 + 2*p4 + p7)| \quad \text{and} \quad |Gy| = |(p7 + 2*p8 + p9) - (p1 + 2*p2 + p3)|$$

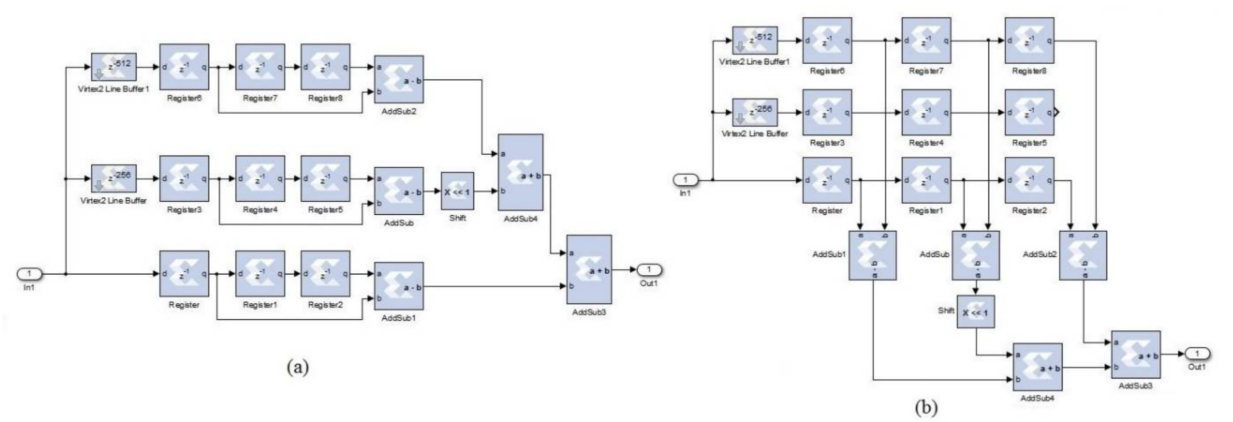

Fig. 7: (a)Sobel Horizontal Gradient Filter (b) Sobel Vertical Gradient Filter

4. Canny Algorithm Model:Fig. 8(a) shows JTAG model for designed Canny Algorithm. It has three outputs which are different steps in Canny such as smoothing, gradient calculation and NMS with hysteresis thresholding. It is obtained by choosing compilation type as Hardware Co-Simulation and then by selecting development board as shown in Fig. 4(b).

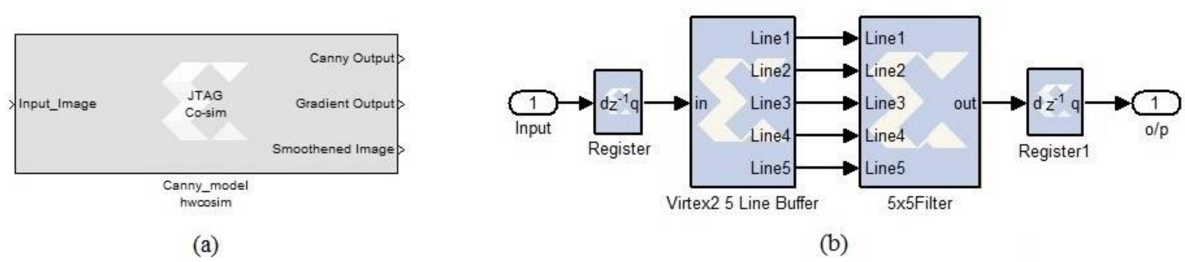

Fig. 8: (a)Canny JTAG Model (b) Gaussian Smoothing using 5×5 Filter

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First step in Canny algorithm model is Gaussian smoothing using 5×5 filter.It makes Canny immune to noise. Image smoothing is carried out using inbuilt 5×5 filter block. This block along with Virtex2 5 Line Buffer provides various image processing applications along with Gaussian Smoothing as shown in Fig. 8(b). Second step consists of Gradient Calculation using Sobel Operator. In this step both horizontal and vertical gradient filters as shown is Fig. 7(a) and Fig. 7(b)are used to find out gradient magnitude of input gray image. Sobel operator is used because of its better performance than other two classical operators i.e., Robert and Prewitt. Next step is of Non-Maximum Suppression (NMS). Smoothing image causes loss in some edges which makes gradient output very thick. Thus,NMS block in the Cannyalgorithm provides Edge thinning. It can be designed using various xilinx blocks. Centre pixel is compared to all the 8 neighbourhood pixels and considered as edge only if it is local maximum. Otherwise, it is suppressed to value 0 (i.e., No Edge). Fourth and final step in Canny algorithm model is of Hysteresis Thresholding.When single threshold is used while processing image containing noise, Streaking is be observed in the output edge map. This disadvantage is eliminated in Hysteresis thresholding. Using basic Xilinx blocks such as mux, comparator, constants etc. this block is designed and both high & low thresholds are assigned to it.

V. EXPERIMENTAL RESULTS

JTAG Co-simulation based approach is used for hardware implementation of different edge detection techniques. In this approach bit stream file generated after preliminary processed of hardware implementation such as synthesis, place and route is dumped into the FPGA hardware. Here, Spartan-3E Starter Kit [10] with device xc3s500e-5fg320 is used for this purpose.Fig. 9(a) shows edge output for all classical operators.

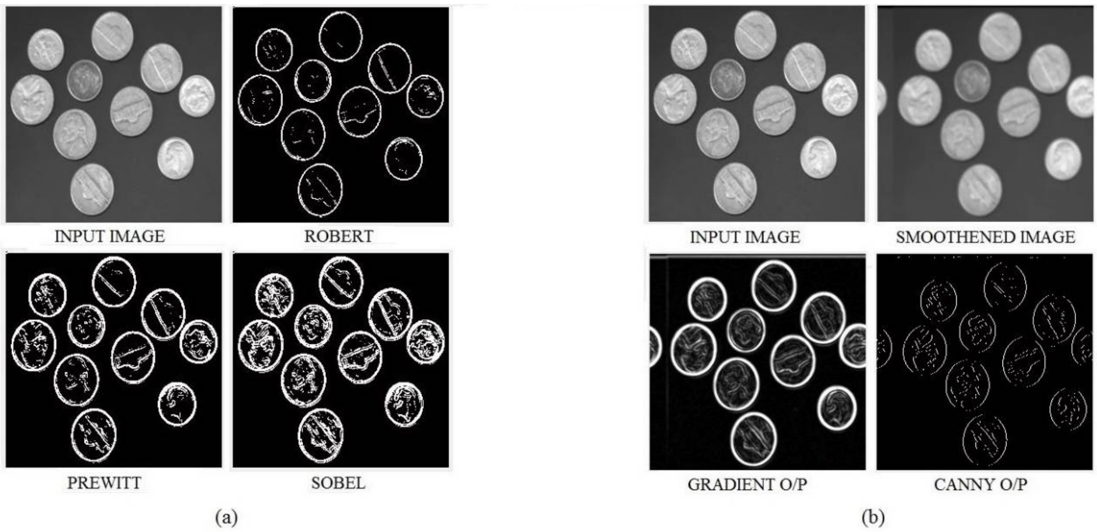

Fig. 9: (a)Edge Output for Robert, Prewitt & Sobel Operators (b) Output for various steps of Canny algorithm

By observation, it is seen that Sobel gives maximum edges whereas Robert provides minimum edges. Gradient based classical operators have very low latency and high throughput and are used in real time. These operators are used in several applications where accuracy is not a major issue such as surveillance, monitoring, barcode reader etc. But, in some applications especially, in the field of biomedical or machine vision, accuracy plays an important role. Thus, Canny algorithm is implemented for such applications. Fig. 9(b) shows resultsfor different steps of Canny algorithm such as smoothing, gradient calculation and Non-Maximum Suppression& hysteresis thresholding.

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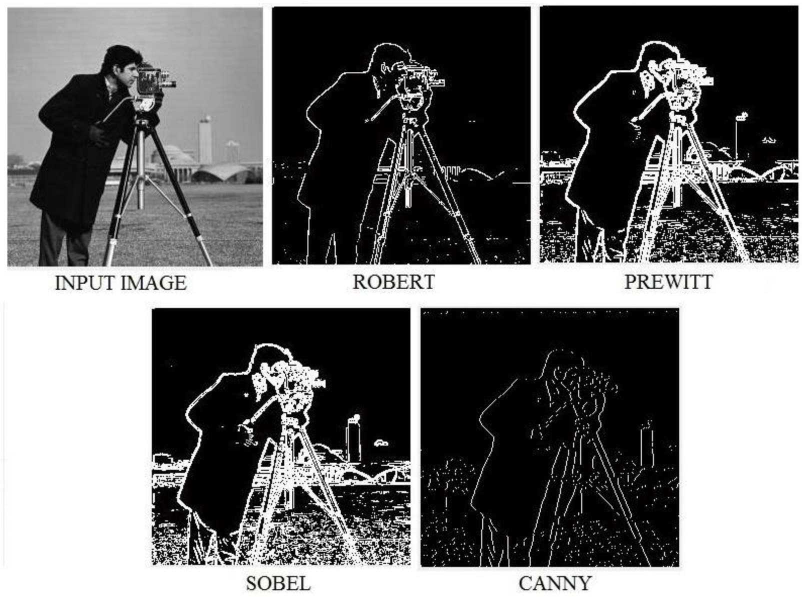

Fig. 10: Comparative analysis of Gradient Based Edge Detection Techniques

Fig. 10 provides a comparative analysis between all implemented edge detection algorithms. It is observed that Canny provides superior performance than Robert, Prewitt and Sobel. It gives thin edges and also it is immune to noise. On the other hand, all classical operators are affected due to noise. Between classical operators, Sobel provides better performance than remaining two. But, Robert is fastest of them all.

VI. PERFORMANCE ANALYSIS

System generator token provides various options for compilation as shown in Fig. 4 (b). Using Timing and Power Analysis compilation, performance analysis is done. Table I shows a comparative analysis of all gradient based edge detection techniques with respect to resource utilization. Resource utilization provides complexity of designed algorithm.It implies that Robert is the simplest and Canny is the most complex of all discussed algorithms.

Table I: Resource Utilization of Edge Detection Techniques

Sr.No.	Logic Utilization	Robert	Prewitt	Sobel	Canny
1.	Slice Flipflops	64	150	148	1039
2.	4 input LUTs	70	163	159	704
3.	Occupied Slices	65	152	167	996
4.	Total number of 4 input LUTs	87	189	186	799
5.	Number used as Logic	70	163	159	559
6.	Number used as a route-thru	17	26	27	95

Table II provides a comparative analysis for all gradient based edge detection techniques with respect to various parameters such as power, minimum period and maximum frequency. Xilinx Power Analyzer is a tool given in ISE Design suit to perform power analysis. Maximum frequency offered by Canny is least as compared to classical operators which limits its frequency of operation. Whereas, Robert has maximum frequency of operation.

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Table II: Comparative Analysis of Edge Detection Techniques

Technique	Total Power [watts]	Min. Period [ns]	Max. Frequency [MHz]
Robert	0.116	4.48	223.36
Prewitt	0.126	5.11	195.58
Sobel	0.127	5.01	199.60
Canny	0.125	13.92	71.83

VII. CONCLUSION

Real time image processing applications require hardware implementation of Edge detection algorithms. In this paper, classical edge detector operators (i.e., Robert, Prewitt and Sobel) and Canny edge detection algorithm are implemented on Spartan-3E FPGA. Obtained results prove that Canny is the best edge detection algorithm followed by Sobel, Prewitt and Robert. Depending on the application requirement we can use any of these algorithms in real time scenario. Also, JTAG hardware co-simulation approach using Xilinx System Generator is found to be easy and efficient approach for hardware implementation over FPGA platform.

REFERENCES

1. R. C. Gonzalez, R. E. Woods, Digital Image Processing, 3rd edition, Prentice Hall, pp.187-190, 2007.
2. R. Maini, H. Aggarwal. “Study and comparison of various image edge detection techniques,” International Journal of Image Processing. Vol.3, pp.1-12, Feb 2009.
3. K.K. Ahmed, A. Fuad, S. M. Rizvi, “Hardware software co-simulation ofCanny edge detection algorithm,”International Journal of Computer Applications, 122(19),pp.7-12, July 2015.
4. Y. Said, T. Saidani, F. Smach and M. Atri, “Real Time Hardware Co-simulation of Edge Detection for Video Processing System,” IEEE, pp.852-857, 2012.
5. G. B. Reddy, K. Anusudha, “Implementation of image edge detection on FPGA using XSG,” International Conference on Circuit, Power and Computing Technologies (ICCPCT), pp.1-5, 2016.
6. Kiran M., K.M. War, L.M. Kuan, L.K. Meng, L.W. Kin, “Implementing image processing algorithms using ‘Hardware in the loop’ approach for Xilinx FPGA,” Proceedings of the International Conference on Electronic Design,Dec. 1-3, IEEE Xplore Press, Penang, pp.1-6,2008.
7. M.Ownby, W.H. Mahmoud, “A design methodology for implementing DSP with Xilinx System Generator for Matlab,” IEEE International Symposium on System Theory, pp.404-408, March 2002.
8. J.Canny, “A computational approach to edge detection,” IEEE transaction on pattern analysis and machine intelligence, vol. 8, no.6, pp.679- 698,Nov 1986.
9. Xilinx System Generator User's Guide.
10. Spartan-3E Starter kit Board User’s Guide,www.xilinx.com

BIOGRAPHY

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