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900nW, 0.8V, 600$ppm/℃$,CMOS Voltage Reference Circuit using High and Low Threshold MOSFETs

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ABSTRACT: This paper based on the principle of temperature compensation of threshold voltage of MOS. It generates constant voltage 375mV with supply voltage range 0.8V - 1.2V. It is implemented in 0.18 UMC CMOS process. The device consists of MOSFET circuits operated in the saturation and sub-threshold region and uses no resistors. It can work at 0.8V supply voltage with dc current consumption of 1.2 µA at absolute temperature. The measured temperature coefficient in temperature range -40 - 80℃ was 600ppm/℃ .The measured line Sensitivity was$0.55\%/V$. The (PSRR) was -21 dB at 100Hz and -11 dB at 10MHz respectively.

KEYWORDS: sub-threshold, low-power, low voltage, power-supply rejection ratio, temperature coefficient, threshold voltage.

I. INTRODUCTION

In VLSI design field voltage reference circuit is basic building block for other devices, which required a constant supply voltage for operation. If we seen the history of voltage reference circuits, it was firstly design by WIDLAR (1971). He was designed band gap voltage reference circuit based on vertical bipolar transistor. This circuit used in CMOS LSIs [1], band gap reference circuits required large value of resistor for implementation, which occupied large area of die, so there is problem in design of area efficient LSIs with less power consumption and lower supply voltage. To remove this problem lot of voltage reference circuits were designed, most of the circuits based on the sub-threshold Operation of MOSFETs, where the supply gate voltage of MOS below the threshold voltage, in the range of 1 V or less than .In this concept circuits consume less power in few micro watt range with small power supply voltage. But in the sub-threshold region of operation of MOS, the device is more sensitive regarding to temperature variation and process variation, here most important thing is dispersion of threshold voltage with the variation of operating temperature. This is challenge for us to compensate the variability of threshold voltage with temperature variation. For solution of this problem, I combined the concept of sub threshold operation of MOSFETs and saturation operation of MOSFETs. Some transistors of the circuit operates in sub-threshold region and some in saturation with the use of different type of MOSFETs, High threshold MOSFETs and Low threshold MOSFETs in same circuit by proper selection of physical Parameter of MOS, like channel length (L), channel width (W), than only transistors work properly in desire region. The implementation of this circuit achieves a better compensation of temperature dependency of threshold voltage and process variation. This voltage reference circuit also better in aspect of supply voltage dependency of reference output voltage from previous reported work because the line sensitivity of this circuit was$0.55\%/V$. It consume 900 n W Dc power with supply voltage 0.8V at room temperature. In detailed we explained the related work in section II, Working principle in section III, result and Discussion in section IV, conclusion in V.

II. RELATED WORK

In the field of reference circuits lot of work done on voltage reference circuit with different circuit topology and working concept at different level of compensation technique for optimisation of circuit performance. They are better in related to power consumption, supply voltage, but they have poor performance regarding to temperature dependency

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Of mobility, threshold voltage dispersion with temperature variation, process variation and body effect. Here I focused on the work done in IEEE journal (2011) by Luca and their group members, because in this paper they work on the principle of sub threshold operation of MOS, so here less power consumption with small supply voltage. This is good in aspect of power-aware LSIs. The poor performance in relation with temperature coefficient and line sensitivity because in sub-threshold region operating temperature variation play important role, effect the mobility, threshold voltage of MOS. So there is possibility in the previous work to improve the temperature coefficient and line sensitivity. I was focused (TC), (LS).

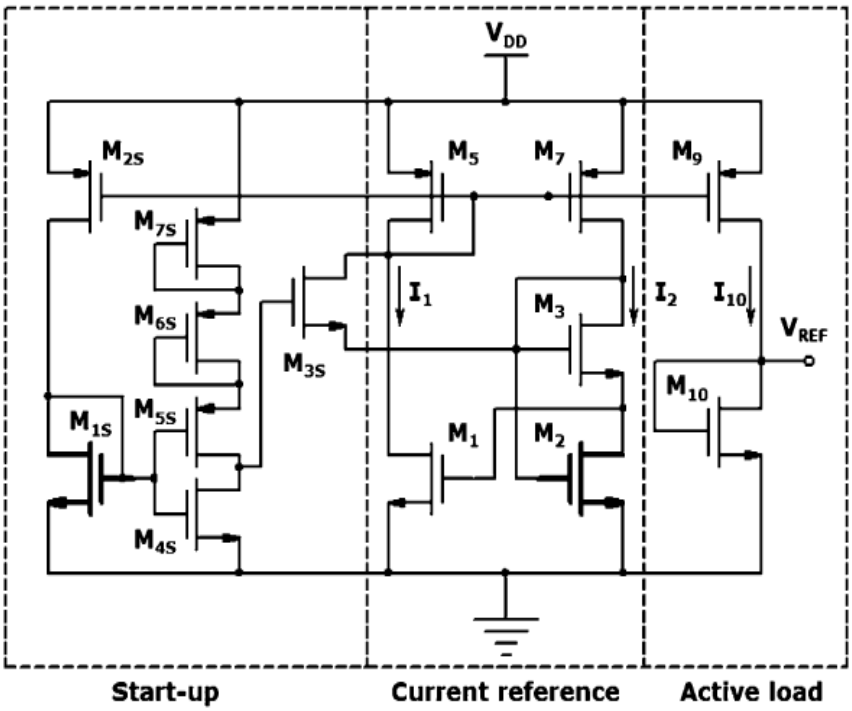

Fig.1. voltage reference circuit reported in ref [1]

Drawback of this circuit is more dependency on temperature variation and supply voltage variation. To avoid this I implement a new circuit shows in proposed methodology.

III. PROPOSED METHODOLOGY

I. OPERATING PRINCIPAL

The functionality of proposed circuit is based on two region of operation of MOS; first region is sub-threshold region and second is saturation region due to this combination of region of operation circuit will work properly with supply voltage less than 1 V. In this work circuit will operate at 0.8 V supply voltage at room temperature. In this circuit all the MOSs of load circuit will work in saturation region, so output voltage given by

$$V_{REF} = V_{th10} + \sqrt{\frac{2I_0}{K_{10}}} \qquad (1)$$

Where I_0 is the operating current of M_{10} .Equation (1) shows the temperature dependency of the reference output voltage. In this equation two temperatures dependent terms, first is Vth_{10} due to temperature dependency of threshold voltage and second is due to temperature dependent of mobility and operating current. Since K_{10} is linearly dependent on mobility and operating current also linearly dependent to mobility that will help to remove the effect of the

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temperature variation on mobility so that output reference voltage temperature independent. By the linear approximation, the threshold voltage linearly decays with temperature of an n MOS transistor shown in equation below.

$$V_{th}(T) = V_{th}(T_0) - K_{t1}(T - T_0) \qquad (2)$$

Here T is the room temperature and K_{t1} is calculated at absolute temperature T_0. So that in order to acquire the temperature independency with a absolute cancellation of the linear dependency of mobility at any temperature, than most important thing is that a operating current linearly dependent $I_0 \propto \mu(T)T^2$ to the temperature squared and mobility that is, so there is a solution to achieve a operating current which based on MOS transistors working in sub-threshold and the saturation region.

IV. CIRCUIT DESCRIPTION

The designed voltage reference circuit is shown in figure 1. The circuit consist three parts first is start-up M_{1s} toM_{3s} . The function of this circuit is to remove the zero biasing condition and provide proper current for next part of the circuit In this part all the MOS operating in saturation region where ($V_{ds} \gg V_{gs}$). The circuit made by transistor numbered from M_1 to M_8 produce a current I_0 which does not depend on supply voltage V_{DD}. Now this current is flow into M_{10} diode connected transistor. The dependence of I_0 on the temperature is manipulated by the temperature dependence of the gate-source voltage of M_{10}. So that circuit produce temperature insensitive reference voltage.

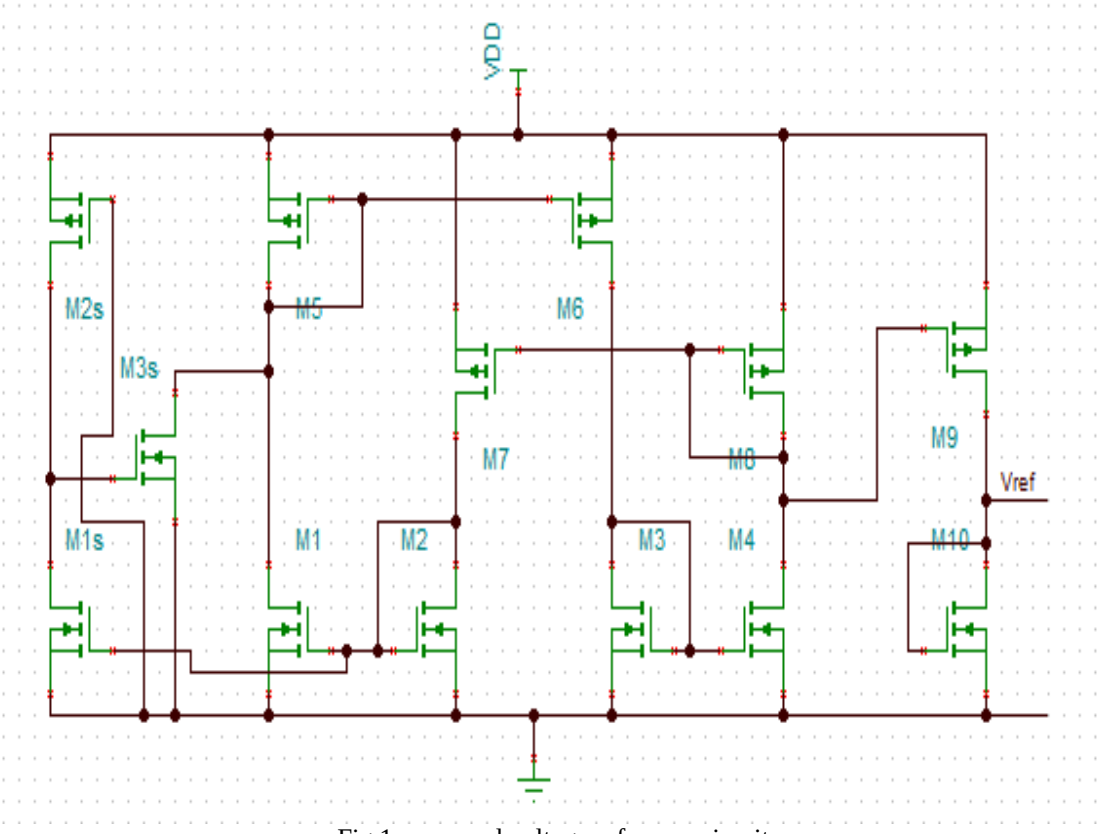

Fig.1. proposed voltage reference circuit.

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V. CURRENT GENERATOR CIRCUIT

This is the second part of the circuit which is the Heart of the current generator circuit it contain the transistors M_1-M_2, which evaluate the value of the current I_0. The MOS M_5 and M_6 inject same current I_1 in M_1 and M_3 and transistor M_7 and M_8 inject same current I_0 in M_2 and M_4. MOS M_1 and M_3 is high threshold MOSFETs and others MOSFETs are low threshold MOSFETs. By the application of two different threshold voltages allow us to work M_4 and M_2 in the saturation region and, at the same time M_3 and M_1 work in Sub-threshold region. Such condition is found by putting the gate-source voltages of M_4, M_3 and M_2, M_1 in between 0.5V and 0.7 V. The (V-I) characteristics of an n MOS transistor that work in the sub threshold regions and saturation given by (3) and (4), respectively.

$$I_d = \mu C_{ox} \; V_T^2 \frac{W1}{L1} e^{\frac{Vgs-Vth}{mVT}} \left[1 - e^{-\frac{Vds}{VT}}\right] \qquad (3)$$

$$I_d = \frac{\mu C_{OX}}{2} \frac{W1}{L1} \left(V_{gs} - V_{th}\right)^2 (1 + \lambda V_{DS}) \qquad (4)$$

Here m is the sub-threshold slope parameter and V_T is the threshold voltage. The gate-source voltages of M_2 and M_1 (M_4 and M_3) are same and can be calculated from (1) and (2) by taking M_4 and M_2 in strong inversion region with drain current I_0 and M_3 and M_1 in sub-threshold with a drain current I_1. Now by enforcing$V_{GS4} = V_{GS3}$ and $V_{GS2} = V_{GS1}$. We calculated I_0

$$I_0 = \frac{\mu C_{ox} \frac{W}{L}}{2(N-1)^2} \; m^2 \; V_T^2 \; ln^2\left(\frac{\frac{W_3}{L_3}}{\frac{W_1}{L_1}}\right) \qquad (5)$$

Where we have defined $N = \sqrt{\frac{\frac{W_4}{L_4}}{\frac{W_2}{L_2}}}$

Here we not consider channel length modulation in calculation that's why (λ=0) and have put the second term in equation (2) to unity. The body effect not affect the operation of the circuit because the source terminal of all NMOS transistors were grounded $V_{th4} = V_{th1}$ and $Vth_3 = V_{th1}$.

VI. ACTIVE LOAD

The third part of the circuit is the active load. It helps to produce reference output voltage by using the current I_0 which is generated by the second part of the circuit. It flows in to active load which consists of a diode-connected NMOS transistor M_{10}. In Order to produce a temperature manipulated reference voltage .M_{10} works in the saturation region and then by using (4) and (5), we can calculate the reference output voltage $V_{REF:}$

$$V_{REF} = V_{th10} + \frac{mV_T}{N-1} \sqrt{\frac{\frac{W_4}{l_4}}{\frac{W_{10}}{L_{10}}}} \; \ln\left(\frac{\frac{W_3}{L_3}}{\frac{W_1}{W_1}}\right) \qquad (6)$$

VII. SIMULATION RESULTS AND DISCUSSION

The simulation of the circuit was done in cadence EDA tool in 180 nm CMOS process by using spectre for schematic analysis and virtuoso for layout analysis at room temperature. For circuit simulation we use the ADE window for different type analysis of the circuit, like DC, AC, Trans, parametric, corner, Monte- Carlo etc. For that circuit I was performed DC analysis for calculation of reference output voltage. AC analysis for calculation of power supply

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rejection ratio, Noise analysis for calculation of noise density, parametric analysis for showing the effect of different parameters variation on circuit performance.

All Simulated result shows below in which fig.2 shows the Reference output voltage (V_{REF}) as a function of supply voltage (V_{DD}) at absolute temperature. The supply voltage was 0.8V and output reference voltage is 375 mV. The reference output Voltage dependency on temperature for different values of the supply voltage is shown in fig.3 the measured temperature coefficient at V_{DD}=0.8 V is $600 ppm/℃$ .The current flow from the V_{DD} as a function of the supply voltage with different temperature values is shown in fig.4. The PSRR was -21dB at 100 Hz and -11dB at 10MHz at operating voltage 0.8 V shown in fig.5.

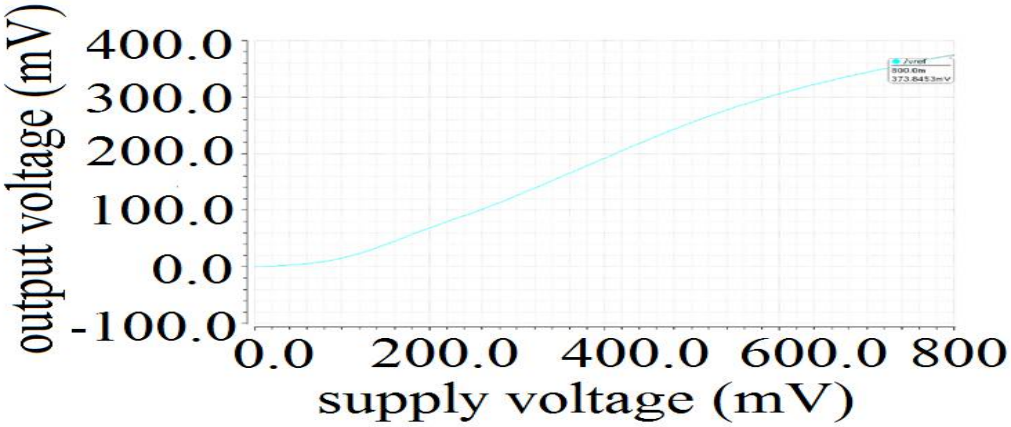

Fig.2. Output refrence voltage as a function supply voltage at room temperature.

This figure shows the reference output voltage change with supply voltage initially but after a certain voltage it is independent on the supply voltage here it get saturated after 0.8 V,which is the property of reference voltage circuit.The measured line sensitivity was $0.55\%/V$ at room temperature in supply voltage range 1.2 – 1.8 V.

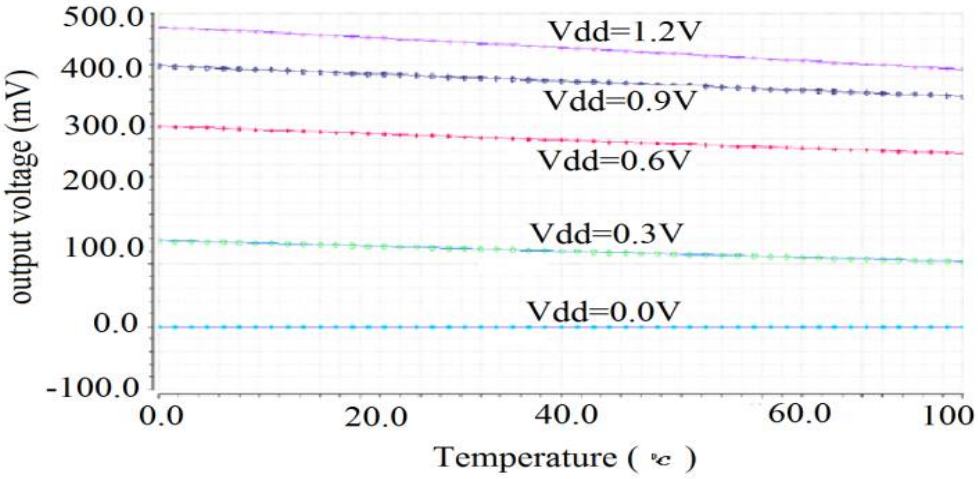

Fig.3. output reference voltage as a function of temperature for different value of supply voltage.

This figure shows the how to output voltage change with change temperature in wide range $0 to 100℃$ .The significance of this graph is that the output voltage should not be changed with the change in temperature at any value

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of supply voltage .In above figure we shows the output voltage at different value of supply voltage. At 0.3 V and 0.6 V the ouput voltage almost independent on temperature. But for the higher value of supply voltage small change in output with temperature .The measured temperaure coefficient was $600ppm/℃$.

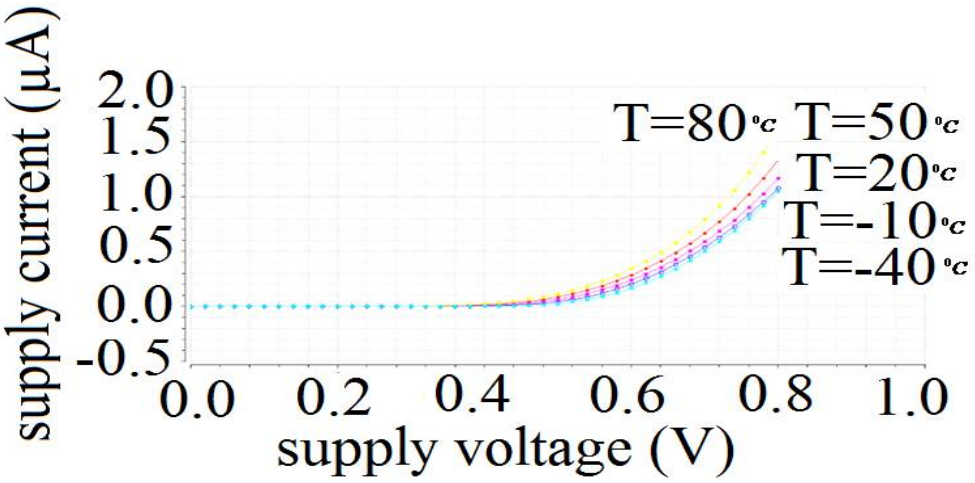

Fig.4. Current drawn from the supply Voltage as a function of supply voltage at different value of the temperature.

This graph shows the supply current drawn from supply voltage as the variation of supply voltage at different value of operating temperature as shown above the supply current increased with temperature and decrease with temperature that means supply current linearly change with temperature. The measured supply current was 1.2 μA at 0.8 V supply voltage at room temperature.

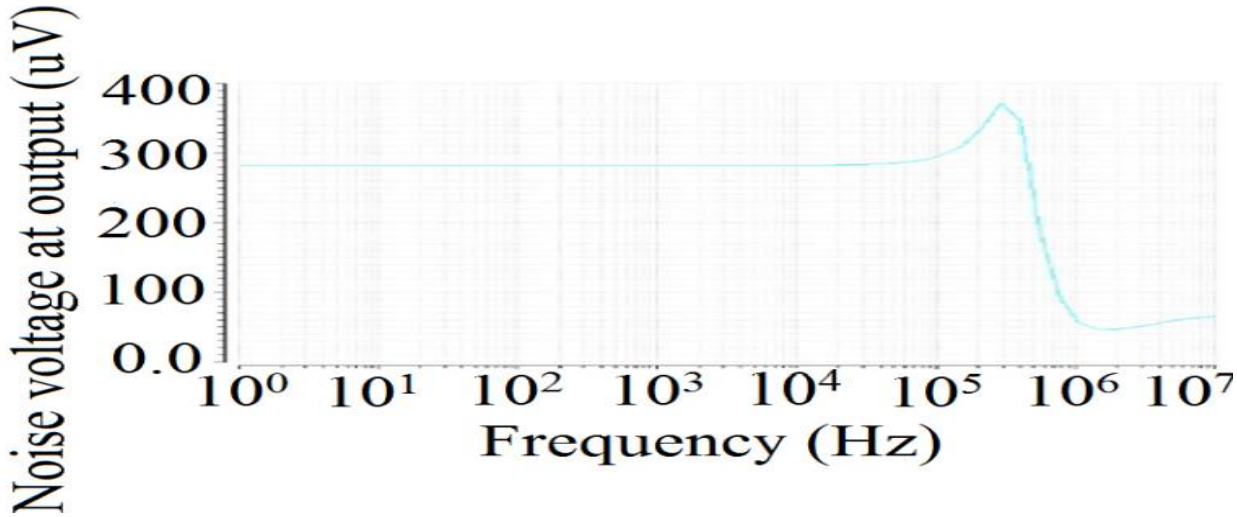

Fig.5. Effect of frequency variation on output voltage.

This plot shows the effect of noise on the generated reference output voltage as a function of frequency at room temperature. The proposed circuit less sensitive to noise variation since measured PSRR was -21dB at100 Hz and -11dB at 10 MHz.

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TABLE 1

Comparison of Reported low-power CMOS voltage reference circuits

	This work	[12]	[13]	[10]	[11]
Process (µm)	0.18	0.18	0.18	0.35	0.35
V_{DD}(V)	0.8-1.2	.45-2	0.85-2.5	0.9-4	1.4-3
Supply current(µA)	1.2	.007	N.A.	.04	.2143
V_{REF}	375mV	263.5mV	221mV	670mV	745mV
TC $ppm/℃$	600	142	194	10	7
Line Sensitivity$(\%/V)$	0.55	0.44	0.905	0.27	.002
PSRR @100Hz @10MHz	-21dB -11dB	-45dB -12.12dB	N.A.	-47dB -40dB	-45dB
Power(µW)	0.9	.0026	3.3	-	.3
Area(mm^2)	0.0022	0.0430	0.0238	0.0450	0.0550

This table shows the comparison of different voltage reference circuit at different level of measured parameters in different technology reported in the literatures in previous years.

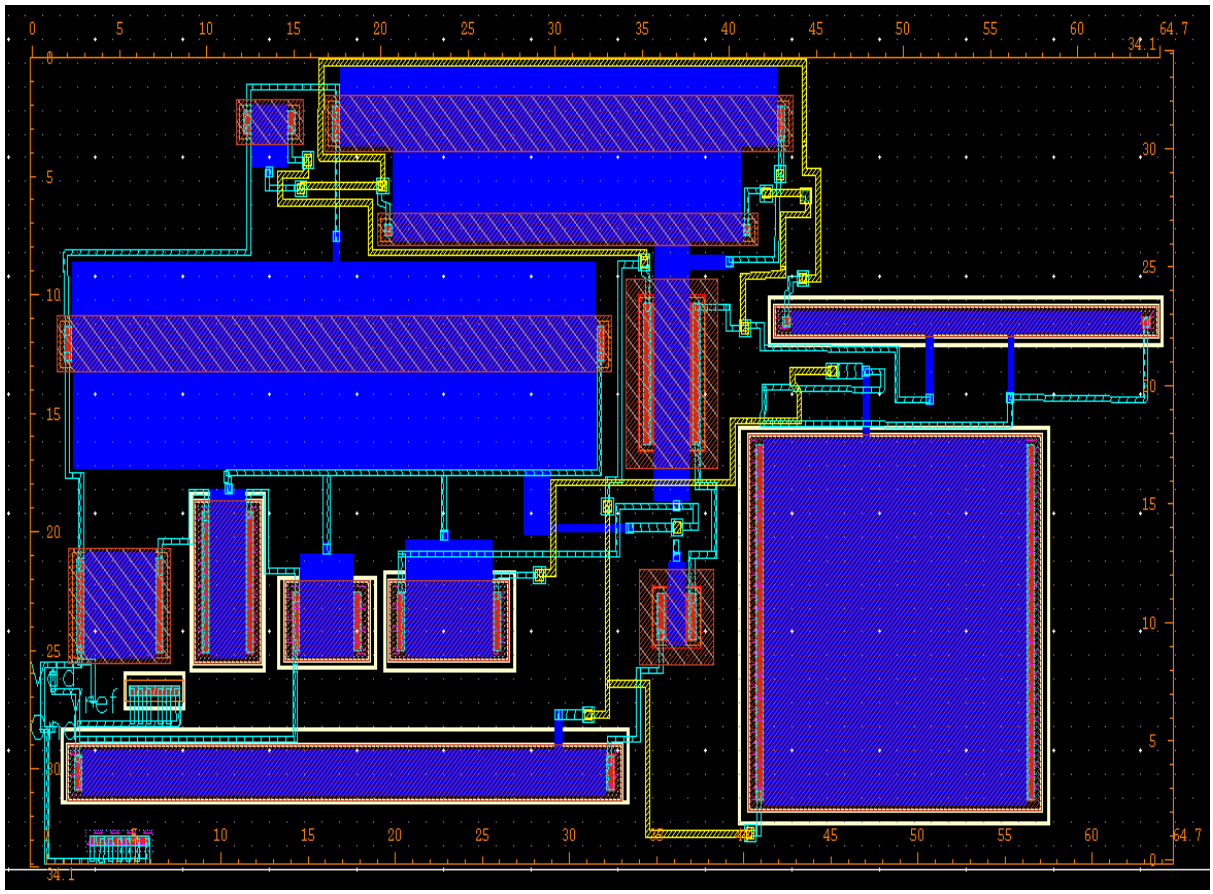

Fig.6. Chip photo of proposed voltage reference circuit

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Fig.6. shows the layout of the proposed voltage reference circuit. The occupied chip area is only $0.0022mm^2$. Less than the other reported work in literature and reduced the number of transistor in the core of the circuit, current reference and active load circuit.

V .CONCLUSION AND FUTURE WORK

A Nano- power CMOS voltage reference circuit is simulated in the 180 nm technology in Spectre simulation tool of cadence. The circuit work with two different threshold voltages of MOSFETs which allow a remarkable reduction in the minimum supply voltage and power consumption .The circuit was generated 375m V reference output voltage at supply voltage 0.8 V. Temperature coefficient was 600 $ppm/℃$ .The power consumption was 900 n W at 0.8 V supply. It is the reason for the circuit used in low power application like in sensors, wearable medical devices. In future work we will use trimming technique for better performance and optimization.

REFERENCES

[1] B.S. Song, P.R. Gray, "A precision curvature-compensated CMOS band gap reference," *IEEE Journal of Solid State Circuits*, vol. DC-18, pp.634-643, December 1983.
[2] K.N. Leung, P.K.T. Mok, "A sub-1 V 15 ppm/°C CMOS Band gap Voltage Reference without requiring Low Threshold Voltage Device,"*IEEE Journal of Solid State Circuits*, vol. 37, pp. 526-530, April 2002
[3] R.A. Blauschild, P.A. Tucci, R.S. Muller, R.G. Meyer, "A new NMOS Temperature Stable Voltage Reference," *IEEE Journal of Solid State Circuits*, vol. SC-13, pp. 767-774, December 1978.
[4] H. Tanaka, Y. Nakagome, J. Etoh, E. Yamasaki, M. Aoki, K. Miyazawa"Sub-1 µ A Dynamic Reference Voltage Generator for battery-operated Drams," *IEEE Journal of Solid State Circuits*, vol. 29, pp. 448-453,April 1994.
[5] M.C. Tobey, D.J. Gialiani, P.B. As kin, "Flat-Band Voltage Reference", U.S. Patent 3 975 648, August 1976.
[6] H.J. Oguey, B. Gerber, "MOS Voltage Reference based on polysilicogate work function difference," *IEEEJournal of Solid State Circuit*, vol.SC-15, pp. 264-269, June 1980.
[7] K.N. Leung, P.K.T. Mok, K.C. Kwok, "CMOS Voltage Reference," US Patent 6 441 680, August 2002.
[8] K.N. Leung, P.K.T. Mok, "A CMOS Voltage Reference Based on Weighted VGS for CMOS Low-Dropout Linear Regulators," *IEEEJournal of Solid State Circuits*, vol. 38, pp. 146-150, January 2003.
[9] H. Banda et al., "A CMOS Band gap Reference Circuit with Sub-1VOperation," *IEEE Journal of Solid State Circuits*, vol. 34, pp. 670-674, May 1999.
[10] G. De Vita and G. Iannaccone, "A sub-1-V, 10 ppm/ C, nano power voltage reference generator," *IEEE J. Solid-State Circuits*, vol. 42, no.7, pp. 1536–1542, Jul. 2007.
[11] K. Ueno, T. Hirose, T. Asia, and Y. Amemiya, "A 300 nW, 15 ppm/ C, 20 ppm/V CMOS voltage reference circuit consisting of sub threshold MOSFETs," *IEEE J. Solid-State Circuits*, vol. 44, no. 7, pp. 2047–2054, Jul. 2009.
[12] L. Magnelli, F. Crupi, P. Corsonello, C. Pace, and G. Iannaccone, "A 2.6 nW, 0.45 V temperature-compensated subthreshold CMOS voltage reference," *IEEE J. Solid-State Circuits*, vol. 46, no. 2, pp. 465–474,Feb. 2011.
[13] P.-H. Huang, H. Lin, and Y.-T. Lin, "A simple subthreshold CMOS voltage reference circuit with channel-length modulation compensation," *IEEE Trans. Circuits Syst. II, Expr. Briefs*, pp. 882–885, 2006.