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Manchester Decoder and Clock Recovery Module Using Xilinx

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ABSTRACT: This paper describes the development and testing of the Manchester decoder and clock recovery module for FPGA prototype. At the core of module operation is the measurement of time between consecutive edges of a Manchester encoded signal, which is performed using two counters clocked by an available clock. The measured time is used to compute the Manchester half-cycle duration, which is in turn used to recover the clock signals. The developed module receives a Manchester encoded signal and generates three signals: two clock signals – one of the same frequency as the input Manchester signal, the other one of a doubled frequency, and a sequence of decoded data bits. The module has been written in VHDL programming language, simulated in Xilinx ISE simulator.

KEYWORDS: Manchester decoder, FPGA, HDL, VHDL programming.

I. INTRODUCTION

Assuming that the incoming radio signal is already demodulated and represented in digital form (such as signal encoded using Manchester code), the clock recovery module can be purely digital. In this case, decoding is done together with clock recovery and the clock signal is used to properly receive decoded data bits by some other module. As for the FPGA-based prototype of the tag, decoding and clock recovery functions can be performed by an HDL module. The rest of this paper describes the developed Manchester decoder and clock recovery module, written in VHDL programming language, its verification by simulations.

Manchester coding is one of the most common data coding methods used today. Similar to BiPhase, Manchester coding provides a means of adding the data rate clock to the message to be used on the receiving end. Also Manchester provides the added benefit of always yielding an average DC level of 50%. This has positive implications in the demodulator's circuit design as well as managing transmitted RF spectrum after modulation. This means that in modulation types where the power output is a function of the message such as AM, the average power is constant and independent of the data stream being encoded. Manchester coding states that there will always be a transition of the message signal at the mid-point of the data bit frame. What occurs at the bit edges depends on the state of the previous bit frame and does not always produce a transition.

In the paper [2], the function of Manchester Decoder is realized using Combinational and Sequential circuits. Combinational circuit includes logic gates for Reset and enable control actions along with the ex-or operation for the Clock recovery. The sequential circuit includes latches and flip flops for the transition detection function for Data recovery. This is designed without any input clock signal so that it can work at any data frequency.

II. MANCHESTER DECODER AND CLOCK RECOVERY MODULE

A. *Proposed work:*

The module mydecoder.vhd has been designed to receive a Manchester encoded signal, to give out two clock signals – one of the same frequencies as the Manchester signal (SYNC), the other one of a doubled frequency (DBL_BSB), and to provide decoded data bits serially. Also the module uses another two input signals: the clock signal CLK and reset signal RST. Schematic representation of the module is shown in Figure 1.

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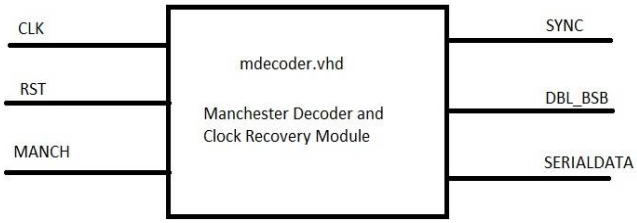

Figure.1: Schematic representation of Manchester decoder and clock recovery module

B. *Description of the Proposed work:*

Each data bit in a Manchester encoded signal is represented by a transition, which should happen during a certain time interval (cycle), as shown in figure 2. Ideally, the cycle duration is constant and the transition happens exactly in the middle of the cycle. The recovered clock period should be equal to the cycle of the Manchester signal. Transitions (edges) of the Manchester signal can be significant, i.e. representing some data bit, or they can happen at the boundary between consecutive cycles. Significant edges take place in the middle of every cycle, while "boundary edges" do not happen between those consecutive cycles, which have different data bits (e.g. 0 and then 1 or vice versa). This means that the time between each two consecutive edges of the Manchester signal can be equal to either its one or two half-cycles.

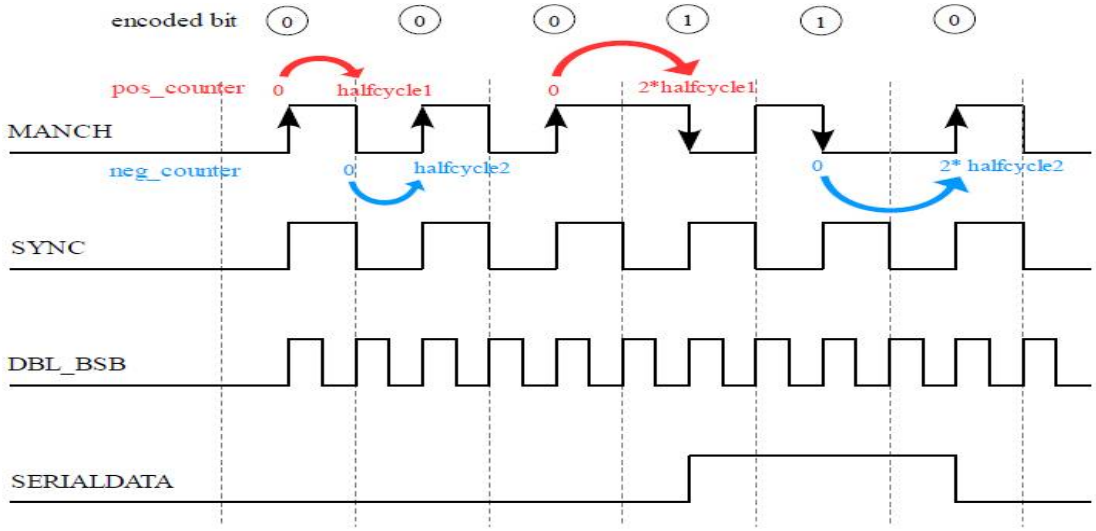

Figure.2: Ideal wave forms applied to and generated by the Manchester decoder and clock recovery module

The counter pos_counter is reset on a positive edge, the counter neg_counter – on a negative edge of the Manchester signal. Thus, whenever a positive edge happens, the value of neg_counter indicates the time elapsed from the last negative edge, i.e. the time interval between the two resent edges. This value is stored as the half-cycle duration halfcycle1 if it lies within [halfcycle2 – jitter; halfcycle2 + jitter], where halfcycle2 is the half-cycle duration computed previously (i.e. on the last negative edge) and jitter equals to some jitter value. If the neg_counter value is within [2*(halfcycle2 – jitter); 2*(halfcycle2 + jitter)], it is divided by two and the result is stored as the half-cycle duration halfcycle1. Similarly, the half-cycle duration halfcycle2 is computed on a negative edge, using the value of pos_counter. If the half-cycle duration is not known before the decoding process, it must be computed using the two first edges of the incoming Manchester signal. In this case the first two data bits must be the same (either two zeros or

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ones) in order to correctly compute the half-cycle duration. Alternatively, if it is known in advance that the first two bits are different, the time interval between the first two edges equals to two half-cycles, and the half-cycle duration can be derived by dividing that time interval by two. The described clock recovery module assumes that the first two data bits are the same. A special process controls both counters (increases and resets them), and two other processes compute the half-cycle duration: one on positive edges, another – on negative edges. The jitter value is assumed to be equal to one eighth of the half-cycle duration and it is also recomputed on every edge.

Clock recovery is based on the fact that the recovered clock signal should be inverted on any Manchester edge. Also it should be inverted at the boundary between adjacent Manchester cycles when an edge is not present (this happens when two consecutive data bits are different). This inversion is performed in a process that tracks the values of the two counters mentioned above. When any of the counters equals to zero, which happens just after some Manchester edge, the recovered clock signal sync_signal, and the doubled frequency signal doubled_baseband are inverted. When there is no Manchester edge, the process checks whether the last observed edge was positive (this is true when pos_counter < neg_counter). If so, the process checks whether the pos_counter value is equal to halfcycle1 + jitter. If it is true, this means that no Manchester edge was detected and one half-cycle interval has already passed since the last positive edge. This corresponds to the boundary between adjacent Manchester periods and both sync_signal and doubled_baseband must be inverted. Besides, when pos_counter counts one or three quarters of Manchester period, the doubled_baseband should be inverted. When there is no Manchester edge and the last observed edge was negative, the clock signals are recovered in an analogous way.

Decoding is based on the fact that each positive edge of sync_signal (recovered clock) happens just after a significant Manchester edge (i.e. after a transition representing some data bit). This takes place already in the second half of the Manchester period and the respective data bit equals to the inverted value of the Manchester signal at that moment, if G. E. Thomas convention is used (pos.transition corresponds to zero, neg. – to one). A special process assigns that value to current_bit signal (connected to SERIALDATA output of the module) on a positive edge of sync_signal. The other module (which uses decoded data) can receive the bit on the following negative edge of sync_signal (which is connected to SYNC output of the module). Notice that the first received edge of an incoming Manchester signal is taken as a significant one. The presented module uses G. E.Thomas convention, but this can be easily changed to IEEE 802.3 convention (where neg. transition corresponds to zero, pos. – to one) by assigning Manchester signal value to current_bit on positive edges of sync_signal in the aforementioned process.

III. SIMULATION RESULTS

The module operation was verified using Xilinx ISE simulator. A test bench waveform was created, which is shown in figure 3. First, a positive pulse appears on RST input of the module, and then MANCH input is supplied with a square pulse signal representing the Manchester encoded data bit sequence "00110101010000000111". The result of the corresponding behavioural simulation is shown in figure 3.

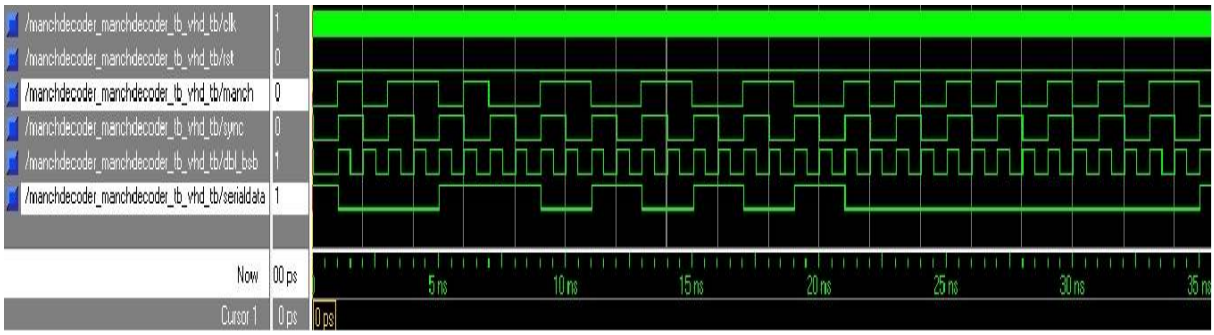

Figure.3: Simulation of module waveform in Xilinx Test Bench

The recovered clock signal is generated correctly on the SYNC output starting from the very first Manchester edge (which is assumed to be a significant edge), despite of the fact that the half-cycle duration is not yet known (it is computed when at least two edges have already happened). This is because the recovered clock signal is inverted on

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any Manchester edge and the two first data bits are the same (which is necessary to correctly initialize the half-cycle value). The doubled baseband frequency signal, generated on the DBL_BSB output, is valid starting from the first half of the first Manchester period, since it requires the knowledge of half-cycle duration. The valid decoded data bits appear on the SERIALDATA output starting from the first Manchester edge. Notice that the positive pulses of SYNC and DBL_BSB signals are wider than normal when two adjacent bits differ. This is because the signal values are inverted later due to the absence of a Manchester edge, as it is explained above.

IV. CONCLUSION

A simple VHDL module, which performs Manchester decoding and clock recovery, has been developed. The main function of the module is to receive a Manchester encoded signal, decode it and extract clock signal from it. The module generates two clock signals – one of the same frequency as the input Manchester signal, the other one of a doubled frequency. Also, the module provides decoded data bits in series on one of its outputs. Each of the data bits can be received by some other module on the falling edges of the generated clock signal. The module, whose operation has been simulated in Xilinx ISE Simulator.

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BIOGRAPHY

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