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# Design of Power & Area optimized 6T Latch for Shift Registers Using Pulsed Latches

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**ABSTRACT:** This paper proposes low power 6T latch for shift registers using pulsed latches. The area and power consumption are reduced by replacing flip-flops with pulsed latches. This method solves the timing problem between pulsed latches through the use of multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The latest portable advanced devices require low power and area efficient designs. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. A n-bit shift register using pulsed latches is designed. The simulation results show that the proposed shift register design with less transistor count is better choice for low power and area efficient applications.

**KEYWORDS:** Area-efficient, Flip-flop, Pulsed clock, Pulsed latch, Shift register.

## I. INTRODUCTION

Latches and Flip flops are the basic storage elements used extensively in all kinds of digital designs. As the feature size of CMOS technology process scaled down according to Moore's Law, designers are able to integrate many numbers of transistors onto the same die. The more transistors there will be more switching and more power dissipated in the form of heat or radiation. Heat is one of the phenomenon packaging challenges in this epoch, it is one of the main challenges of low power design methodologies and practices. Another driver of low power research is the reliability of the integrated circuit. A shift register is the basic building block in a VLSI circuit. Shift registers are commonly used in many applications, such as digital filters [1], communication receivers [2], and image processing ICs [3]–[5]. Recently, as the size of the image data continues to increase due to the high demand for high quality image data, the word length of the shifter register increases to process large image data in image processing ICs. An image-extraction and vector generation VLSI chip uses a 4K-bit shift register [3]. A 10-bit 208 channel output LCD column driver IC uses a 2K-bit shift register [4]. This paper proposes a low-power and area-efficient shift register using pulsed latches. The shift register solves the timing problem using multiple nonoverlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches.

## II. RELATED WORK

Flip-flops and latches (collectively referred to as timing elements) are heavily studied circuits, as they have a large impact on both cycle time and energy consumption in modern synchronous systems. Previous work has focused on the energy-delay product of timing elements (TEs), but real designs include many TEs that are not on the critical path and this timing slack can be exploited by using slower, lower energy TEs. Instead of simultaneously optimizing for delay and energy, critical TEs should be optimized to reduce delay and noncritical TEs should be optimized to reduce energy. For example, it used different structures for critical and noncritical flip-flops in the context of a logic synthesis design flow. The transmission gate pulsed latch (TGPL) [7], hybrid latch flip-flop (HLFF) [8], conditional push-pull pulsed latch (CP3L) [9], Power-PC-style flip-flop (PPCFF) [10], Strong ARM flip-flop (SAFF) [11], data mapping flip-flop (DMFF) [12], conditional precharge sense amplifier flip-flop (CPSAFF) [13], conditional capture flipflop (CCFF) [14],

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adaptive-coupling flip-flop (ACFF) [15] are compared with the SSASPL [6] which has minimum number of transistors.

Previous work often measured energy consumption using a limited set of data patterns with the clock switching every cycle. But real designs have a wide variation in clock and data activity across different TE instances. For example, low-power microprocessors make extensive use of clock gating resulting in many TEs whose energy consumption is dominated by input data transitions rather than clock transitions. Other TEs, in contrast, have negligible data input activity but are clocked every cycle.

## III. PROPOSED DESIGN

### A. *Proposed Shift Register*

A master-slave flip-flop using two latches in Fig. 1(a) can be replaced by a pulsed latch consisting of a latch and a pulsed clock signal in Fig. 1(b)[6]. All pulsed latches share the pulse generation circuit for the pulsed clock signal. As a result, the area and power consumption of the pulsed latch become almost half of those of the master-slave flip-flop. The pulsed latch is an attractive solution for small area and low power consumption.

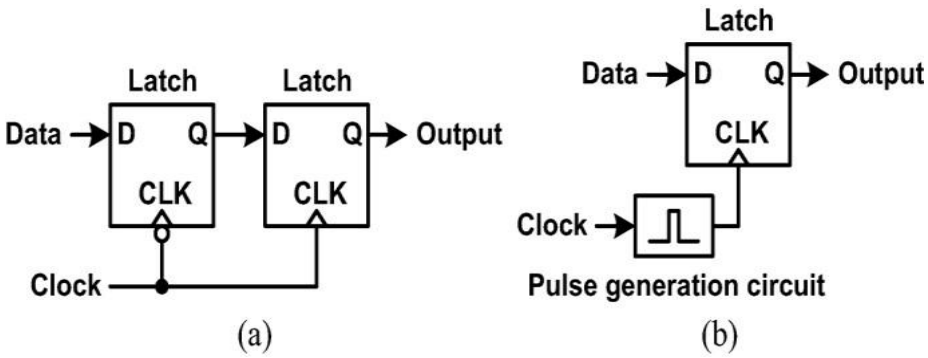


Fig.1 (a) Master-slave flip-flop. (b) Pulsed latch.

### B. *Problem with pulsed latch and solution*

The pulsed latch cannot be used in shift registers due to the timing problem, as shown in Fig. 2. The shift register in Fig. 2(a) consists of several latches and a pulsed clock signal (CLK_pulse). The operation waveforms in Fig. 2(b) show the timing problem in the shifter register. The output signal of the first latch (Q1) changes correctly because the input signal of the first latch (IN) is constant during the clock pulse width (TPULSE). But the second latch has an uncertain output signal (Q2) because its input signal (Q1) changes during the clock pulse width. latches. All latches have no timing problem occurs between the latches and constant input signals during the Therefore, there are two solutions to solve this problem.one solution for the timing problem is to add delay circuits between clock pulse in the result. However, the delay circuits cause large area and power overheads.

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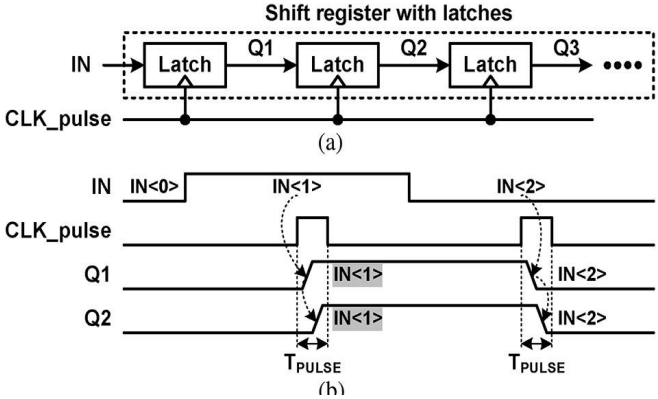


Fig 2: Shift register with latches and a pulsed clock signal. (a) Schematic. (b) Waveforms.

Another solution is to use multiple non-overlap delayed pulsed clock signals, as shown in Fig. 3(a). The delayed pulsed clock signals are generated when a pulsed clock signal goes through delay circuits. Each latch uses a pulsed clock signal which is delayed from the pulsed clock signal used in its next latch. Therefore, each latch updates the data after its next latch updates the data. As a result, each latch has a constant input during its clock pulse and no timing problem occurs between latches. However, this solution also requires many delay circuits. As a result, each latch has a constant input during its clock pulse and no timing problem occurs between latches. However, this solution also requires many delay circuits'

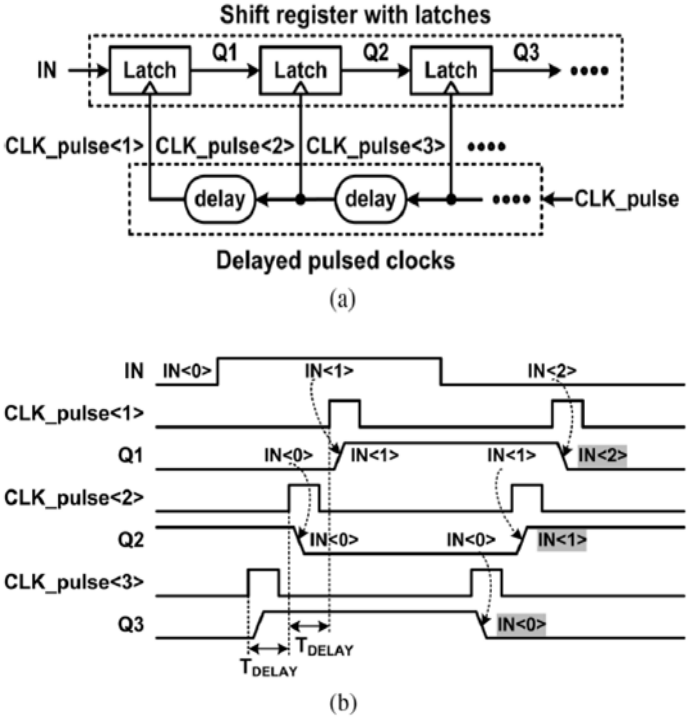


Fig 3: Shift register with latches and delayed pulsed clock signals. (a) Schematic. (b) Waveforms.

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C. *Description of the Proposed system*

An example the proposed shift register shows in fig 4 . The proposed shift register is divided into M sub shifter registers to reduce the number of delayed pulsed clock signals. A 4-bit sub shifter register consists of five latches and it performs shift operations with five nonoverlap delayed pulsed clock signals(CLK_pulse<1:4>and CLK_pulse<T>). In the 4-bit sub shift register #1, four latches store 4- bit data (Q1-Q4) and the last latch stores 1-bit temporary data (T1) which will be stored in the first latch (Q5) of the 4-bit sub shift register #2.

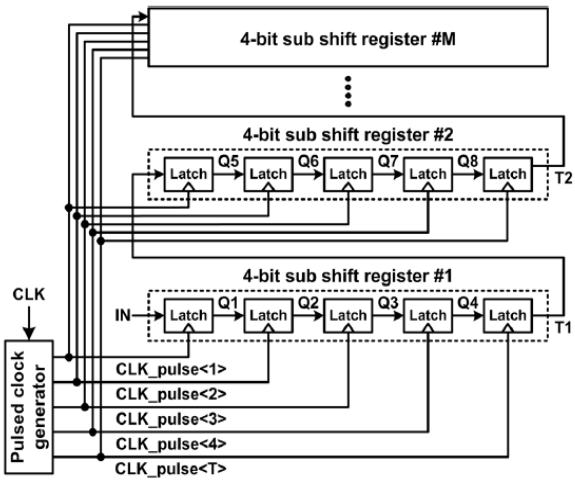


Fig 4: Schematic of Proposed shift register.

The proposed shift register reduces the number of delayed pulsed clock signals significantly, but it increases the number of latches because of the additional temporary storage latches. Each pulsed clock signal is generated in a clock-pulse circuit consisting a delay circuit and an AND gate. When an N-bit shift register is divided into K-bit sub shift registers, the number of clock-pulse circuits is K+1 and the number of latches is N+N/K. A sub shift register consisting of K+1 latches requires K+1 pulsed clock signals. The number of sub shift registers (M) becomes N/K , each sub shift register has a temporary storage latch. Therefore, N/K latches are added for the temporary storage latches. The conventional delayed pulsed clock circuits in Fig. 3 can be used to save the AND gates in the delayed pulsed clock generator .In the conventional delayed pulsed clock circuits, the clock pulse width must be larger than the summation of the rising and falling times in all inverters in the delay circuits to keep the shape of the pulsed clock.

The proposed shift register uses latches instead of flip flops to reduce the area and power consumption. The schematic of SSASPL (static differential sense amp shared pulse latch) in Fig. 5, which is the smallest latch, is selected. The original SSASPL with 9 transistors [6] is modified to the SSASPL with 7 transistors in Fig. 5 by removing an inverter to generate the complementary data input (Db) from the data input (D). In the proposed shift register, the differential data inputs (D and Db) of the latch come from the differential data outputs (Q and Qb) of the previous latch. The SSASPL uses the smallest number of transistors (7 transistors) and it consumes the lowest clock power because it has a single transistor driven by the pulsed clock signal.

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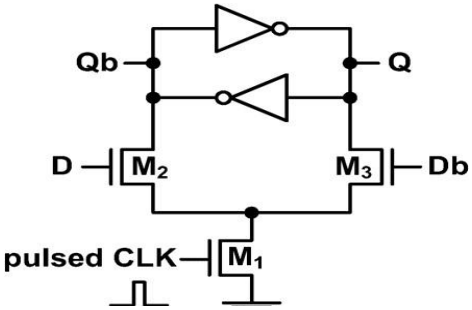


Fig 5: Schematic of the SSASPL [6].

The basic idea behind the proposed design is to replace transmission gate logic by pass transistor logic in conventional 8T design. The proposed 6 transistor design implements pass transistor logic for the transmission of data through it. The drain of first transistor PMOS_1 are connected to the data input and this data will be available at the drain terminal only when the clock will be low (Fig.6.) Since PMOS transistors are weak zero transistors, so small threshold loss is observed when data is zero. The output of this transistor is connected to the input of the first inverter. This inverter then inverts this data and also compensates the threshold loss, but not completely and thus less than the desired output loss is observed at the output. The next inverter again inverts the data and produces the output 'Q'. This output is feedback to the transistor NMOS_1.But overall performance of the device is almost unaffected because of the presence of the inverters.

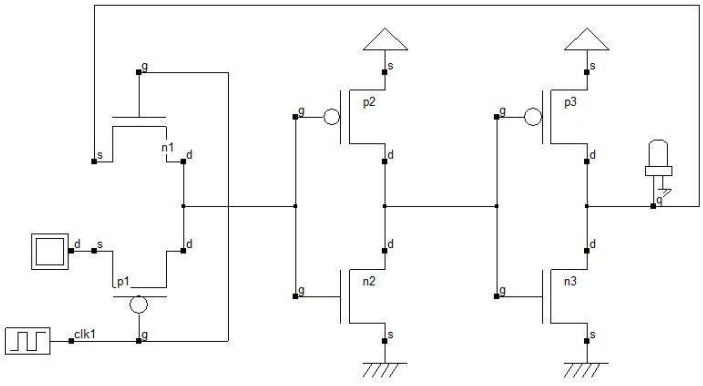


Fig 6: Proposed 6 Transistor Latch

## IV. SIMULATION RESULTS

All the simulations are performed on Microwind3.5 and DSCH3.5. The main focus of this work is to meet all challenges faced in designing of shift register circuit with pulsed latches and proposed latch. The shift register reduces area and power consumption by replacing flip-flops with pulsed latches and proposed latch. The timing problem between pulsed latches is solved using multiple non-overlap delayed pulsed clock signals instead of a single pulsed clock signal. A small number of the pulsed clock signals is used by grouping the latches to several sub shifter registers and using additional temporary storage latches.The latch consumes power for data transition and clock loading The proposed 6transistor design implements pass transistor logic for the transmission of data through it. The timing diagram of 6T pulsed latch is shown in fig 8.Whenever, clock is negative, the output changes with respect to data but remains constant as clock goes positive. .

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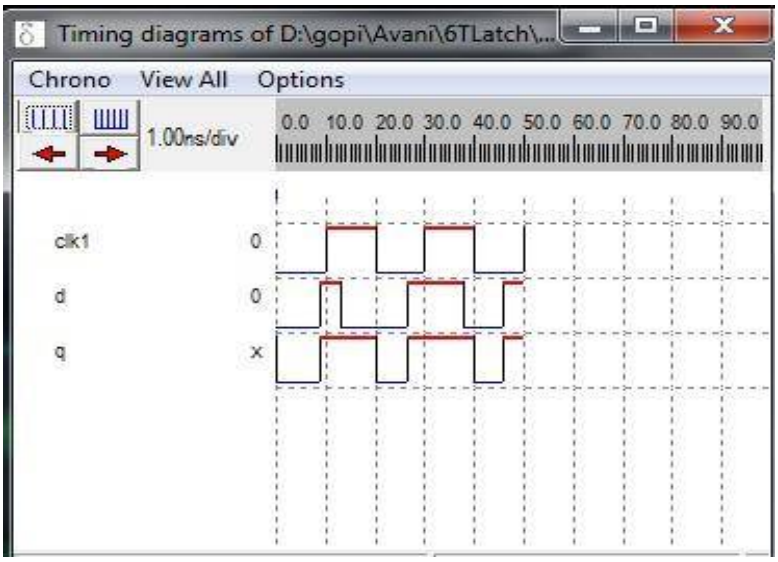


Fig 7: Timing diagram of 6T pulsed Latch

In Fig 8, we can observe the simulation waveform of pulse latch using 6T. It acts as a negative level triggered flip flop thus whenever clock is high, data is not passing through the transistor PMOS_1 but output is again feedback through the circuit and output remains same.The proposed shift register by using 6T latch achieves a small area and low power consumption compared to the conventional shift register

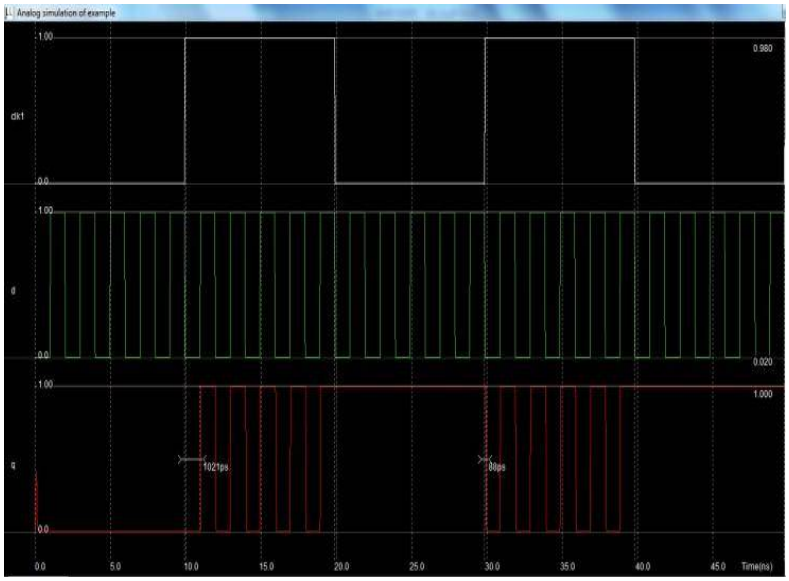

Fig 8: Simulation of 6T pulsed Latch

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## V. CONCLUSION AND FUTURE WORK

The simulation results of the conventional and proposed design found that the proposed 6-transistor latch is better for low pow. Since the transistor count is less, thus the proposed design is also area efficient. This paper proposed a low power and area-efficient shift register using pulsed latches. The shift register reduces area and power consumption by replacing flip-flops with pulsed latches. The timing problem between pulsed latches is solved using multiple non-overlap delayed pulsed clock signals instead of a single pulsed clock signal. A small number of the pulsed clock signals is used by grouping the latches to several sub shifter registers and using additional temporary storage latches. A 128-bit shift register was fabricated using a 65nm µm CMOS process with VDD = 1.0V. The proposed shift register saves area and power compared to the conventional shift register with flip-flops.

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