ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 7, July 2015

Design and Implementation of VGA Controller on FPGA

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ABSTRACT: This paper presents the design and implementation of VGA Controller. As a standard display interface, VGA (Video Graphics Array) has been widely used. Detailed information of this paper is focused on the system architecture, hardware design and software programming. This controller is developed using Verilog HDL based in the IEEE standards, to ensure the portability with any user. The system can display any image. The results show that this proposed algorithm gives good performance with short processingtime, small power consumption and memory usage

KEYWORDS: VGA Controller; Altera Quartus II; DE2-115 Development Board;Verilog

I. INTRODUCTION

A well-known standard interface VGA is used in many embedded systems video surveillance systems, ATM machines, video players, or video conferencing. This system provides a simple method to connect a system with a monitor for showing images or information. Depending on the needs of these applications, some systems may not require a high display quality. Therefore, VGA controller, which is a logic circuit to control the VGA interface, can be easily realized by FPGA technology with a low cost and high flexibility.

Industrial production machines of today must be highly flexible in order to fulfil all unplanned demands. FPGA are especially suited to fulfil these requirements. FPGA provides an impacted size and low power consumption solution. For study, research and experimentation, the emerging technology of FPGA made VGA controller design accessible and suitable.

In this paper, the Altera's FPGA is used for the hardware circuit. We take top-down programming methodology and adopt the integrated tools (Quartus version 13.0). After designing, compilation, function simulation, layout and timing simulation done and each module can be downloaded into FPGA. This method can reduce the size of the circuit board and enhance reliability of system and design flexibility. As a result, it can reduce the system cost.

II. RELATED WORK

In [1] paper designing is done by using VHDL and implement it on Cyclone EPIC6Q240C8, this device is currently not available with Quartus II version 13.0.

In [2]paper, designing of VGA Controller is based on FSM and implements it on Xilinx xcSpartan3s tool, where utilization of LUT's and IOE is more than 5%.

In [3] paper, designing is done by using VHDL and image is send by mobile to FPGA and displayed it on screen.

In [4] paper, a VGA monitor Controller built with just two 10 bit binary up counter, four SR flop-flops, and 11 AND gates. And implemented on UP2 development board.

In [5] paper, they interface a VGA port available on FPGA board to generate the character(s) from ASCII text characters.They organized the 640x480 display area into "tiles" where each tile represents a character location. In this project, the font size of each character is 16x8(height & Width). This font will display 80 text characters in each line Mapped onto a 640x480 display (i.e., 640 pixels divided by 8 columns per character) and 30 lines (480 / 16). Each of the 640x480 pixels in the display are associated with one of the 80x30 character locations.

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III. PROPOSED WORK

A. *Proposed Block Diagram:*

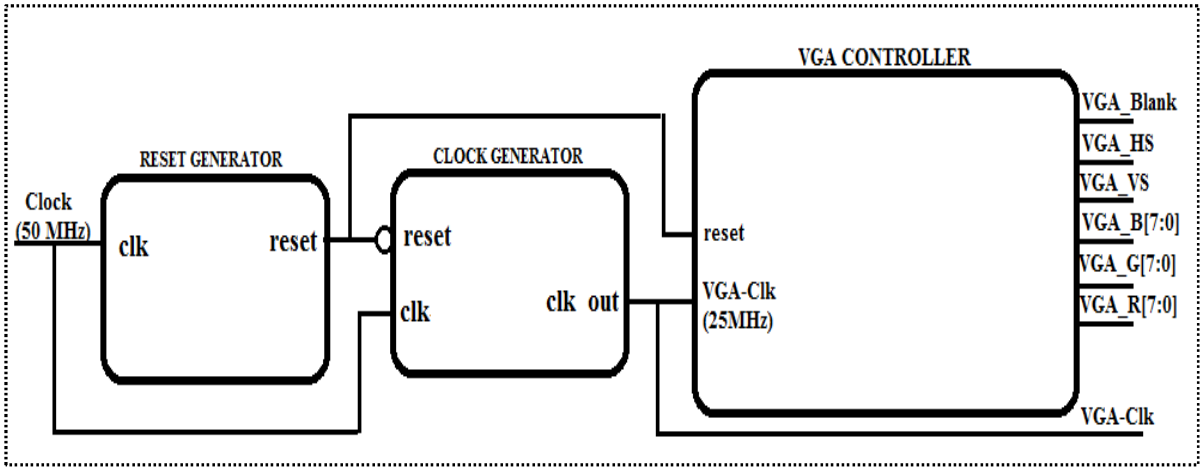

Fig1. Proposed Block Diagram

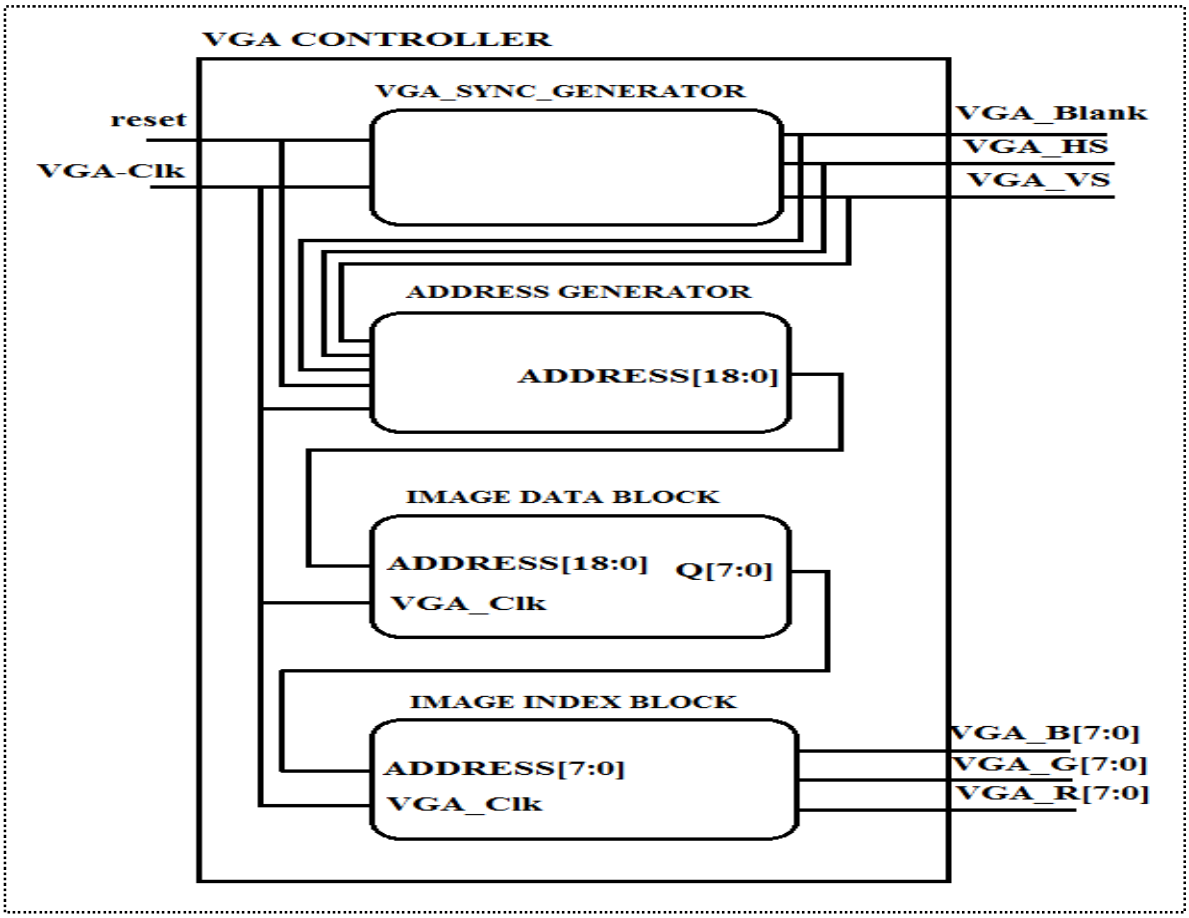

Fig.2. Internal Block Diagram Of VGA Controller.

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B. *Description of the Proposed Diagram:*

Figure 1 & 2 shows, the proposed block diagram of VGA Controller, which consist reset, clock generated block and VGA Controller block. And the internal block diagram of VGA Controller which consists VGA synchronization block, address generator block, image data block, and image index block.

As input we have to give clock pulse and reset signal and at output, we will get RGB (red, green, blue), horizontal synchronization, vertical synchronization and blanking signals.

Referred to Fig. 1 & 2, the function of reset block is to generate the reset signal and the function of "clock generator" block is to reduce the frequency of input clock from 50 MHz to 25 MHz, as to achieve 640 x 480 resolution. Meanwhile, "vga_sync" block is used to generate timing and synchronization signals. while the "h_sync" signal specifies the required time to scan a row, and the "v_sync" signal specifies the required time to scan the entire screen. "vga_sync" block also generates the "blank" signal which indicates retrace period of the display.

Besides that, "address generator" block is used to generate address for the "img_data" block by using the "h_sync", "v_sync" and blanking signal. "img_data" block will get the index data (q) from the MIF file according to the address generated.

Note that the index data are connected to the "img_index" block to use as the address. The "img_index" block will get the RGB data (q) from MIF file according to the address generated (index data). The RGB data consist of 24-bits, whereas "q [23:16] ", "q [15:8]" and "q [7:0]" indicate the "R_data", "G_data" and "B_data" respectively.

IV. DESIGN AND IMPLEMENTATION

A. *Designing of VGA Controller:*

Designing of VGA Controller was done by using integrated tool Altera Quartus II software version 13.0.Block wise designing of VGA Controller is as follows:

Step I: Designing of Clock Generator Block:

To obtain the 640 × 480 screen resolution, a clock with a 25.175 MHz frequency is used. This can be done by using Altera PLL Megafunction.

Megafunctions, such as the ones available in the LPM, are pre-designed modules that you can use in FPGA designs. These Altera-provided Megafunctions are optimized for speed, area, and device family. You can increase efficiency by using a megafunction instead of writing the function yourself. By using each PLL, we can create 5 clock sources.

This design uses a PLL clock source to obtain the 640x480 screen resolution. A PLL uses the on-board oscillator (which is different for different development boards) to create a constant clock frequency of 25MHz as the input to VGA controller. To create the clock source, you will add a pre-built LPM megafunction named ALTPLL.

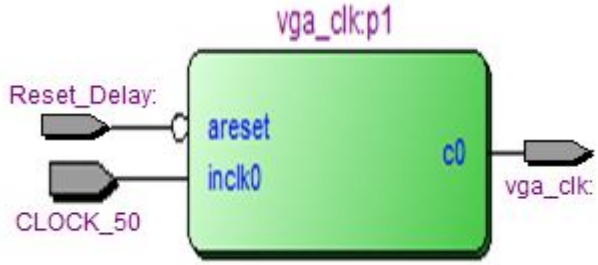

Fig.3. RTL View of Clock Generator Block

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

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Vol. 3, Issue 7, July 2015

Step II: Designing of VGA Synchronization Block:

For horizontal and vertical sync we required **10 bit counter**, as horizontal sync having 800 lines and vertical sync having 525 lines.Inputs of VGA synchronization block are VGA clock signal and reset signal and outputs are horizontal synchronization, vertical synchronization and blanking signal.

Fig.4. RTL View of VGA Synchronization Block

Step III: Designing of Image Data Block:

Inputs to this block is address generated by address generator block and clock signal. And output is index value of image data and that are used as address for image index block.

For this block first we have to extract pixel values from image, for 307200 addresses and then create MIF (memory initialization file) file.

Megafunctions, such as the ones available in the LPM, are pre-designed modules that you can use in FPGA designs. These Altera-provided Megafunctions are optimized for speed, area, and device family. You can increase efficiency by using a megafunction instead of writing the function yourself.This block was designed by using LMP ROM megafunction.

Fig.5. RTL View of Image Data Block

Step IV: Designing of Image Index Block:

Inputs to this block is address generated by image index block and clock signal. And output are RGB data, each of 8bit.

For this block first we have to extract 256 color level values from image and then create MIF (memory initialization file) file.

Megafunctions, such as the ones available in the LPM, are pre-designed modules that you can use in FPGA designs. These Altera-provided Megafunctions are optimized for speed, area, and device family. You can increase efficiency by using a megafunction instead of writing the function yourself.This block was designed by using LMP ROM megafunction.

Fig.6. RTL View of Image Index Block

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

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Vol. 3, Issue 7, July 2015

Step V:Designing of Reset Block:

Inputs to reset block is clock. And output is reset signal.For generating reset block, there is need of **20 bit counter**.

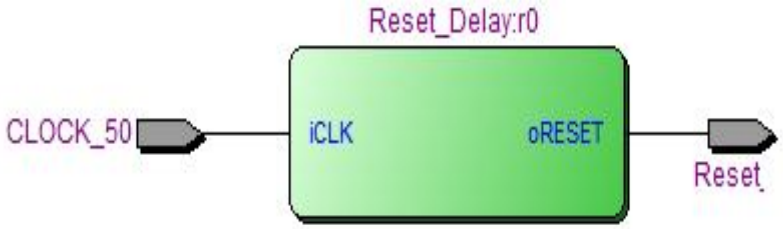

Fig.7. RTL View of Reset Block

Step VI:Designing of Address Generator Block:

Inputs to Address Generator block are clock, reset, horizontal, vertical synchronization and blanking signal from VGA synchronization block. And output is address signal for image data block.

It generates 307,200 addresses and for that there is need of 19 bit counter.

B. *Implementation Of VGA Controller:*

The DE2-115 board includes a 15-pin D-SUB connector for VGA output. The VGA synchronization signals are provided directly from the Cyclone IV E FPGA, and the Analog Devices ADV7123 triple 10-bit high-speed video DAC (only the higher 8-bits are used) is used to produce the analog data signals (red, green, and blue). Figure gives the associated schematic.

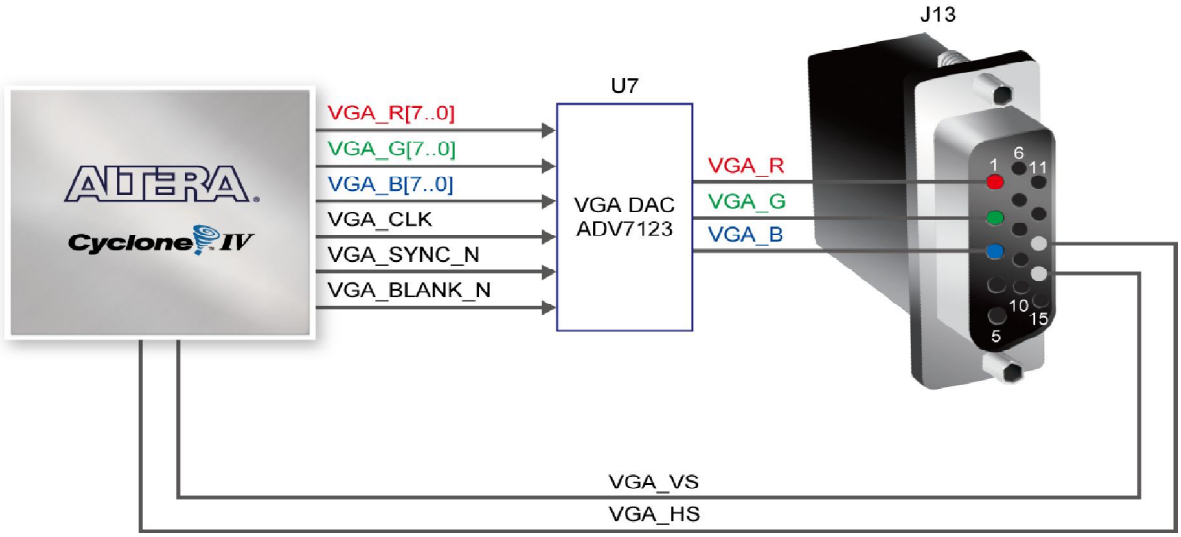

Fig 8. Connections between FPGA and VGA

Steps of Implementation:

I. Take DE2-115 Development Board.
II. Connect 12V supply through adapter to turn ON/OFF the board.
III. Connect USB cable to laptop/computer and also to the USB Blaster of the Board.
IV. Open Quartus II software, by double clicking on Quartus II icon.
V. Compile Verilog code in Quartus II.
VI. Assign a pins at pin planner, by using user manual of DE2-115 board.
VII. For program dumping on board, click Tool > Programmer.

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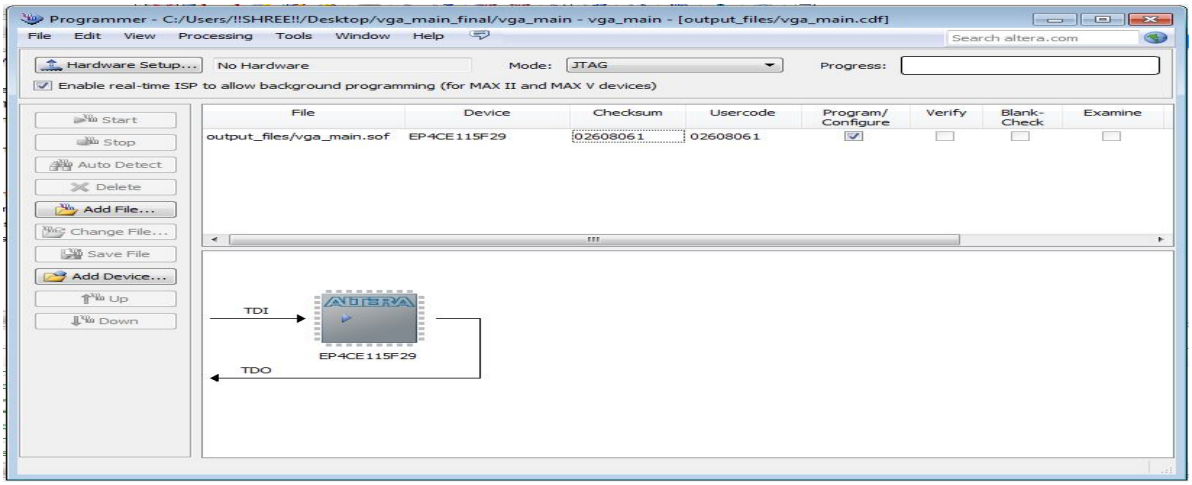

Fig.9. Quartus II Programmer Window.

VIII. There are two modes of Programming and they are,

JTAG programming: In this method of programming, named after the IEEE standards Joint Test Action Group, the configuration bit stream is downloaded directly into the Cyclone IV E FPGA. The FPGA will retain this configuration as long as power is applied to the board; the configuration information will be lost when the power is turned off.

AS programming: In this method, called Active Serial programming, the configuration bit stream is downloaded into the Altera EPCS64 serial configuration device. It provides non-volatile storage of the bit stream, so that the information is retained even when the power supply to the DE2-115 board is turned off. When the board's power is turned on, the configuration data in the EPCS64 device is automatically loaded into the Cyclone IV E FPGA.

IX. Select any programming mode as per choise.

X. Click Start.

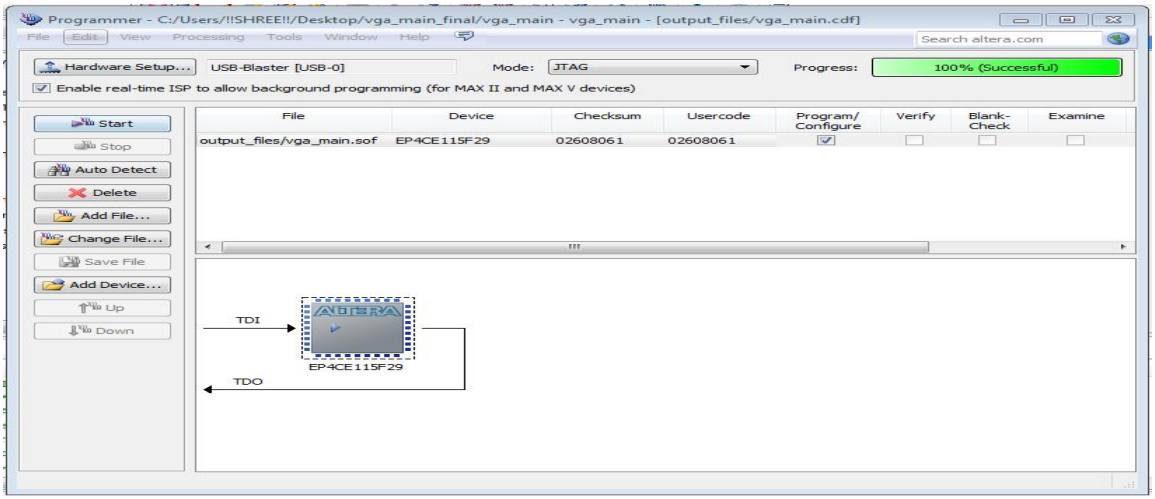

Fig 10. Connections between FPGA and VGA

XI. After successful downloading, connect board with moniter by using VGA cable.

XII. And observe the image on screen.

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V. SIMULATION RESULTS

In order to be able to see the results obtained from the proposed algorithms on an FPGA, astandard VGA monitor may be chosen. The system can be connected to any VGA port LCD (Liquid Crystal Display) or CRT (Cathode Ray Tube) monitor. After compilation is completed, download the Verilog Program into the target device (EP4CE115F29C7). After successfullydownloading, choose working mode of electric circuit and observe image on the monitor.

Following are simulated results of VGA Controller,

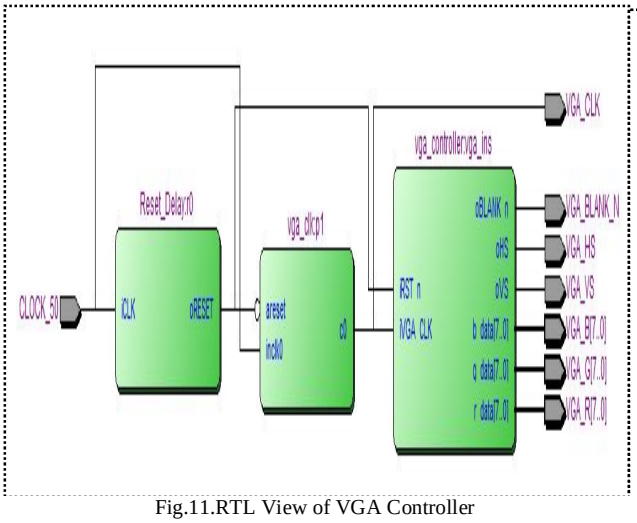

Fig.11.RTL View of VGA Controller

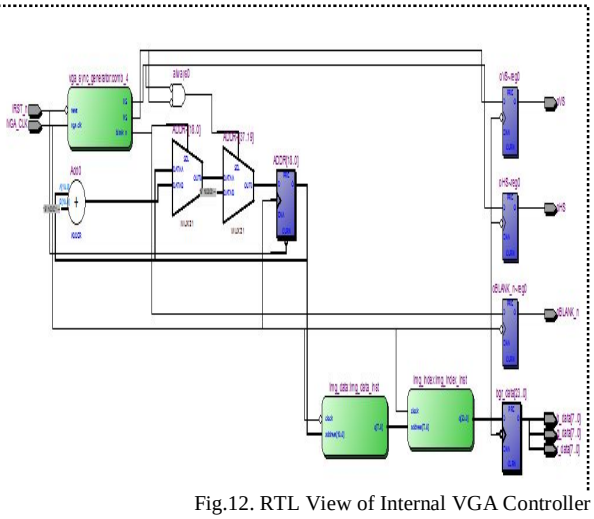

Fig.12. RTL View of Internal VGA Controller

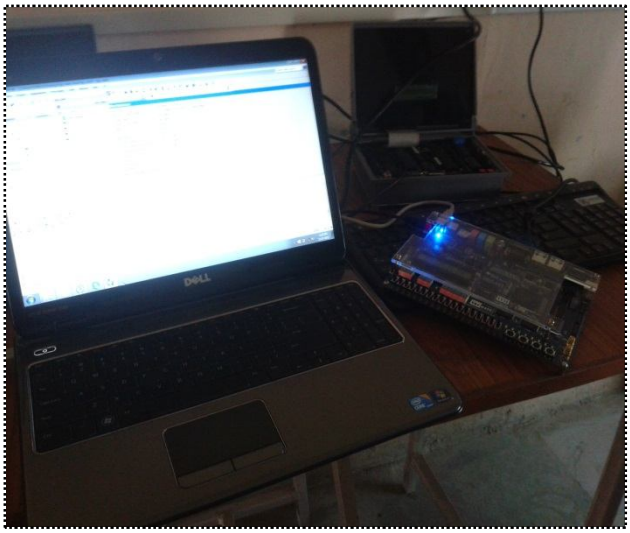

Fig.13. Implementation of VGA Controller

Fig 14. Final Output Image

VI. CONCLUSION

In the proposed vga control system, show the systematic used of fpga to developed this system, which can display image or information. This architecture may be used in any fpga device regardless of the brand or model. Experimental results show processing algorithms programmed by veriloghdl can make design flexible and

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International Journal of Innovative Research in Computer and Communication Engineering

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programming conveniently.this method changes traditional design concept of vga display system by using the programming devices. The controller will be used for image processing research. Vga controller could be constructed easily without constructing the circuit manually; just to write a programming based on its logic flows, then simulate it, synthesize it with netlist, and finally program it onto fpga. It is very effective as this vga controller only needs new data to change to other design display. Thus, fpga-based vga controller might be a good choice as it is easy to be designed and tiny to be used.

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BIOGRAPHY

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