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Energy Efficient Approximate M Bit Vedic Multiplier for DSP Applications

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ABSTRACT: Now a days the digital signal processing and its classification applications on the energy constrained devices should be supported on the basis of efficiency. Because such applications have to perform highly complex computations especially complex multiplication processes while exhibiting tolerance for a large amount of noise and for computational errors too. So, comparing all the arithmetic computations, improving the energy efficiency of multiplication is critical. In this brief, an energy efficient approximate m bit vedic multiplier is proposed which gives a trade off between computational accuracy and energy consumption. The proposed architecture has reduced area compared to other multiplier architectures which process same number of bits. The reduced architecture area reduces the power consumption. Also the vedic technology adopted for the multiplication reduces the delay further. But the approximate architecture output possess a small amount of computational accuracy which is negligible for DSP applications. .

KEYWORDS: digital signal processing; energy efficient; vedic multiplier; approximate multiplier

I. INTRODUCTION

For today's embedded system and mobiles energy consumption is a critical design problem. A lot of efforts have already taken at various levels for improving energy efficiency. Among other arithmetic operations, multiplication is the most time and power consuming operation. It becomes more significant for large operands and complex multiplication. Usually in computing devices for executing the DSP applications and its classifications with more efficiency specialized processors are used. Also many DSP and classification applications are designed to process information which contains large amount of noise.

An adaptive pseudo-carry compensation truncation scheme known as PCT scheme is introduced in earlier efforts [4]. On comparing other truncation methods this method yields low error. But the leakage and dynamic power of PCT multipliers are more than other truncated multipliers. Later a novel architecture of multiplier with tunable error characteristics is proposed [5]. The main advantage of the method is that the architecture consumes comparatively less dynamic power. This multiplier is inherently faster and it needs less gate sizing to meet rising frequency constraints. But the drawback of the architecture is that the error rate is a bit high. Then another multiplier called iterative logarithmic multiplier is introduced [6] which uses logarithmic number system. The method follows the Michelle's algorithm to an extent but it it doesn't follow the approximation techniques. The iterative logarithmic multiplier can afford many number of correction terms as the error rate reduces with increase in number of correction terms but it increases the power consumption.

In this brief, a new approximate multiplier is proposed which selects consecutive 'm' bits from 'n' bits of operands. This new method can provide much more energy efficiency than the truncated methods. The error rate is low because it effectively captures the noteworthy lower bits. For DSP and its classification algorithm, generally one of two operands in the multiplication is stored in the memory. Here it is exploited to improve the energy efficiency of the approximate multiplier further. The area can be effectively reduced by the proposed approximate multiplier because a large number of adders and gates can be excluded in this method compared to other multipliers with the actual n bit operands. Within the approximate multiplier architecture a Vedic technology is used for the multiplication which reduces the delay in the multiplication process.

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The rest of the brief includes different sections which details about the literature survey with former related works, the approximate multiplier architecture and the analysis and conclusion about the brief.

II. LITERATURE SURVEY

R. Hegde and N. R. Shan hag in 1999 proposed a framework for energy efficient digital signal processing [1]. Here to match the critical path delay with the throughput the supply voltage is scaled beyond the critical voltage. To avoid the degradation in the algorithmic performance, algorithmic noise-tolerance (ANT) scheme is applied. Due to deep submicron (DSM) noise the proposed technology can be used to improve the performance of DSP algorithms in presence of bit-error rates of up to 10^{-3}. In 2002 D. Menard, D. Chillet, C. Charot, and O. Sentieys presented an Automatic floating point to fixed-point conversion for DSP code generation [2] which was a new methodology of implementation in Digital Signal Processors (DSP) under accuracy constraint. This architecture was meant for the minimization of power consumption, time and cost. The methodology defined the optimal fixed point data formats for minimizing the power consumption.

V. K. Chippa, D. Mohapatra, A. Raghunathan, K. Roy, and S. T. Chakradhar proposed a scalable effort hardware design [3] in 2010 as a new approach to tap the reservoir of algorithmic resilience and translate it into highly efficient hardware implementations. at each level of design abstraction the scalable effort design approach identifies mechanisms that can be used to vary the computational effort expended towards generation of the correct result. These scaling mechanisms can be used to achieve improved energy efficiency. C. H. Chang and R. K. Satzoda in 2010 proposed a low error and high performance multiplexer-based truncated multiplier which uses an adaptive pseudo-carry compensation truncation (PCT) scheme [4]. Among the other existing truncation methods the proposed method gives low average error. The proposed PCT multiplier runs 21% faster than the VCT multiplier with comparable dynamic power dissipation.

P. Kulkarni, P. Gupta, and M. Ercegovac proposed a new architecture for multiplier in 2011 named Trading accuracy for power with an under designed multiplier architecture [5]. Here they proposed a novel multiplier architecture with tunable error characteristics. The authors improved the design using a residual adder for the correct operation of the multiplier for non error resilient applications.Z. Babi´c, A. Avramovi´c, and P. Bulic proposed an iterative logarithmic multiplier [6] in 2011. This iterative logarithmic technique is about enabling achievement of an arbitrary accuracy for multipliers. It is based on the Mitchell's algorithm number representation but does not use the approximation logarithm. The proposed technique is efficient and simple and the error rate is very small. In this method parallel circuits are given for error correction and hardware is not much power consuming.

Poornima M, Shivraj Kumar Patil, Shivkumar, Sridhar K P and Sanjay H, introduced a brief about Implementation of Multiplier using Vedic Algorithm in 2013 [7]. It gives an idea about the Vedic technology and about the multiplication process using the vedic technology. The basic unit of a vedic multiplier is the 2×2 vedic multiplier architecture and the higher order multipliers can be built from it.

III. PROPOSED 'M' BIT SELECTION ARCHITECTURE

The structure of the proposed M Bit Selection Architecture of approximate multiplier is shown in Fig. 1.

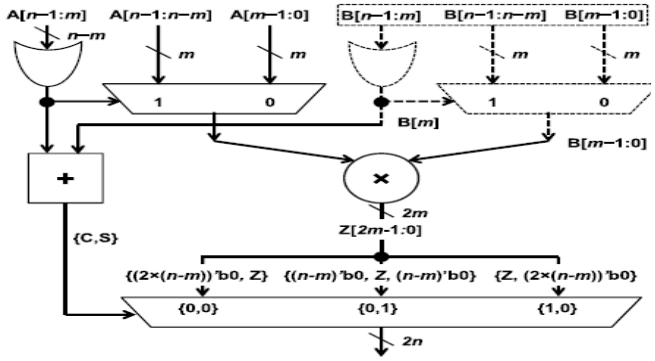

Fig 1. Proposed m bit mulplier architecture

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The architecture consists of two 'm' bit selection units for each n bit operands , a multiplier unit ,a 3 to 1 mux as output unit and a half adder which gives the selection bit for the output mux.

Here the approximate multiplier takes only 'm' consecutive bits for multiplication from each 'n' bit operands. The 'm' can be equal or greater than 'n/2'. The m bit segment is selected only from one of two or three fixed bit positions of a positive number depending on where is its leading one bit. This technique gives a higher accuracy than simply truncating the LSBs. In this approach the m bit segments are selected from each operands from the leading one positions and it is then steered into an m × m multiplier (which is here a Vedic multiplier) and then the 2m output obtained from the multiplier is expanded to 2n output bits.

A. *The M Bit Selection Of The Proposed Approximate Multiplier:*

The figure 2 below shows an example of a multiplication after taking8-b segments from 16-b operands.

×					**0111**	**0111**	**0**101	1010
					0000	00**11**	**1011**	**10**11
=	0001	0001	0100	1001	0101	0000	0000	0000

Fig 2. Example of a multiplication with 8-b segments of two 16-b operands; bold-font bits comprise the segments

But, for such a multiplication approach there is a small negative impact on the computational accuracy that it may eliminates redundant bits (i.e., sign-extension bits) while steering the most useful *m* significant bits to the multiplier unit. So much more sophisticated combinations of bits are extracted in figure 3. The figure below shows examples of extracting 8-b and 10-bsegments from a 16-b operand.

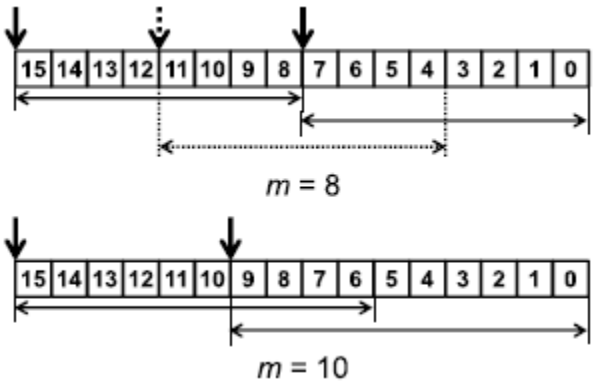

Fig 3. Possible starting bit positions of 8-b and 10-b segments indicated by arrows;
The dotted arrow is the case for supporting three possible starting bit positions.

For a multiplication process with m segments from n bit operands the output from the multiplier will have 2m bits. It can be further expanded to 2n bits by a suitable shift from 3 possible shift amounts. The three possible shifts are:-

1. No shift when both segments are from the lower *m*-bit segments.
2. (*n*–*m*) shift when two segments are from the upper and lower ones, respectively.
3. 2× (*n*–*m*) shift when both segments are from the upper ones.

The scalability for various m and n is the key advantage of the approximate multiplier architecture. Because the complexity like area and power consumption of the auxiliary circuits scales linearly with m.

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The possible shift operations depending on the selection of m bit segments are shown in the figure 4. The shaded cells represent 8-bit segments and the aligned position of 8×8 multiplication results.

×					01xx	xxxx	xxxx	xxxx
					0001	xxxx	xxxx	xxxx
=					0000	0000	0000	0000
×					01xx	xxxx	xxxx	xxxx
					0000	0000	01xxx	xxxx
=	0000	0000					0000	0000
×					0000	0000	01xx	xxxx
					01xx	xxxx	xxxx	xxxx
=	0000	0000					0000	0000
×					0000	0000	01xx	xxxx
					0000	0000	01xx	xxxx
=	0000	0000	0000	0000				

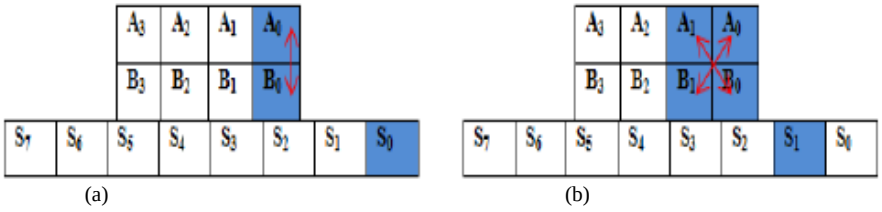
Fig. 4. Examples of 16×16 multiplications based on 8-b segments with two possible starting bit positions for 8-b segments.

Here the multiplier output is is approximated to 2n bits by suitable shift operations and is mainly meant for DSP applications. Hence the bit error at the approximate output is not much significant. Even though the difference in the approximate output is not much important for DSP applications it can be furthermore improved by steering the m segments from the other set of operands to the multiplier (which is not the output of m bit selection mux). Then this 2n bit output from the output mux is added with the previous 2n bit outputs.

IV. VEDIC ARCHITECTURE FOR THE MULTIPLIER UNIT

A. *Vedic Multiplication Process*

For the Vedic multiplication consider a 4×4 multiplier whose operands are $A_3A_2A_1A_0$ and $B_3B_2B_1B_0$. Then the LSB of the sum S_0 is the vertical product of A_0 and B_0, S1 is the sum of $A_0 * B_1$ and $A*_1B_0$ and tens bit of previous sum (S_0). The same process is applied for all the multiplication. The ten's and the hundred's position bit are forward as the carry to next addition. Only the S_7 bit of answer will comes from the tens bit S_6 in the 4 bit multiplication process. In the n bit multiplication process the 2n-1 bit of answer is calculated like the same way as S_7 bit. The 4 bit multiplication process is shown in the figure 5.



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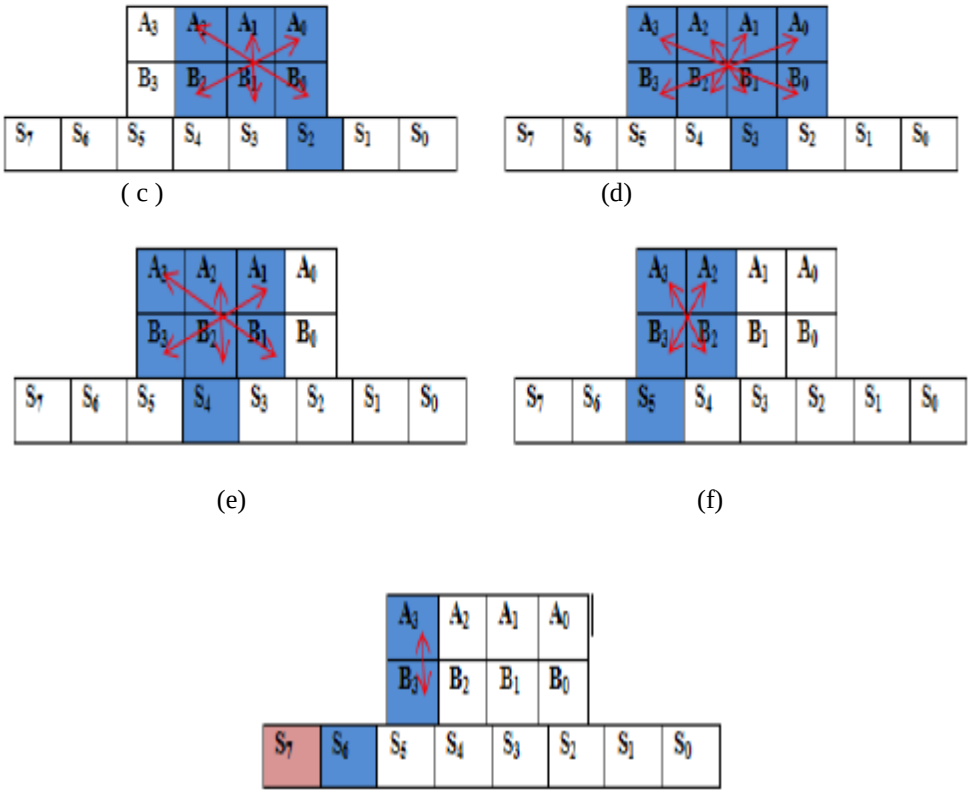

Figure 5 (a) to (g). Calculation of output bits from S_0 to S_7 respectively

For the multiplication of a single bit a simple AND gate is used. From figure 5 the generalised equations for the output bits of a 4×4 multiplier can be written as

- $S_0=A_0*B_0$
- $S_1=A_0*B_1 + A_1*B_0$
- $S_2=A_0*B_2 +A_1*B_1 + A_2*B_0$ +prev carry
- $S_3=A_0*B_3 +A_1*B_2 + A_2*B_1 +A3*B_0$ + prev carry
- $S_4=A_1*B_3 +A_2*B_2 + A_3*B_1$ +prev carry
- $S_5=A_2*B_3 + A_3*B_2$ + prev carry
- $S_6=A_3*B_3$

The S_7 bit is the carry of the previous addition process. Thus 8 bit output is obtained.

B. *Hardware Architecture Of Vedic Multiplier*

A 4 bit vedic multiplier architecture is shown in figure 6. The architecture consist of many full adders, half adders and an or gate.

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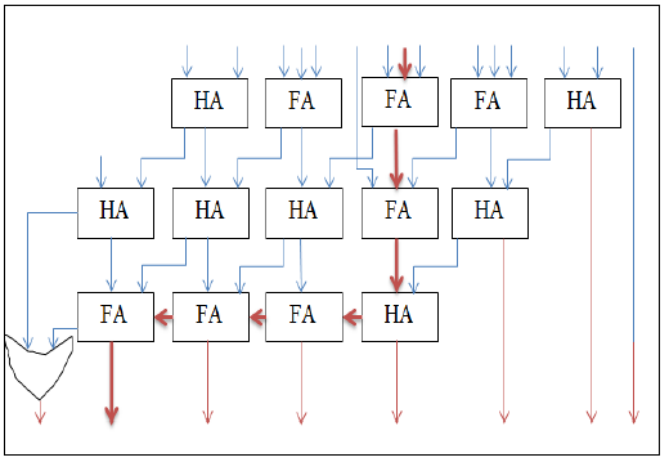

Fig 6. Common architecture for a 4 bit vedic multiplier

Few full adder circuits are replaced in the architecture shown in figure 6 by some half adders and an or gate to obtain a delay reduced architecture for 4 bit vedic multiplier and is shown in figure 7.

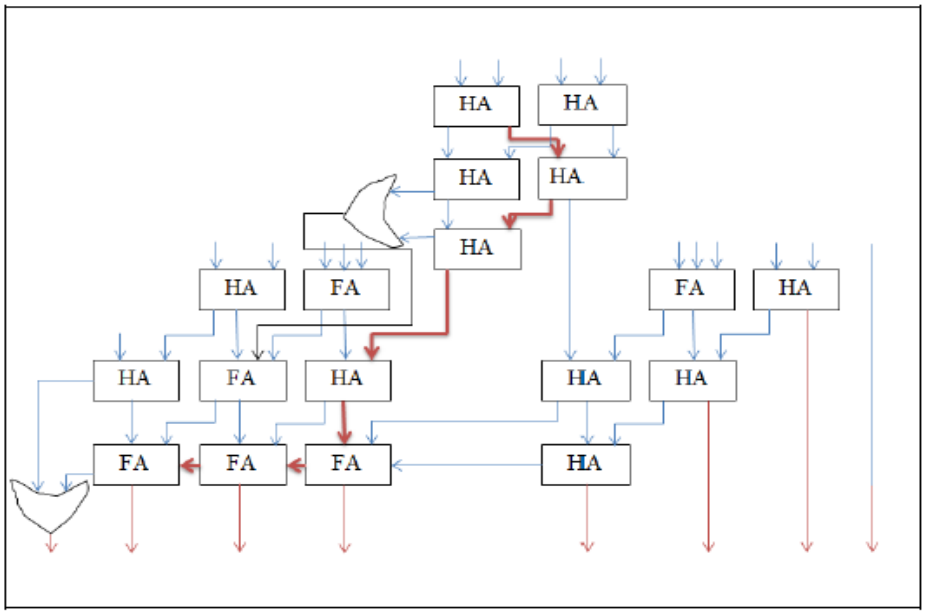

Fig 7. The 4 bit vedic architecture with reduced delay

In both figures (fig 6 and fig 7) the red dark lines shows the critical path and from the figures it is clear when the full adders are replaced with the half adders the critical path delay is reduced to a great extent.

The higher bit vedic multiplier architectures like 8 bit, 16 bit, 32 bit etc can be built using these 4 bit vedic multipliers. The figure 8 shows the architecture of an 8 bit vedic multiplier using 4 bit vedic multipliers.

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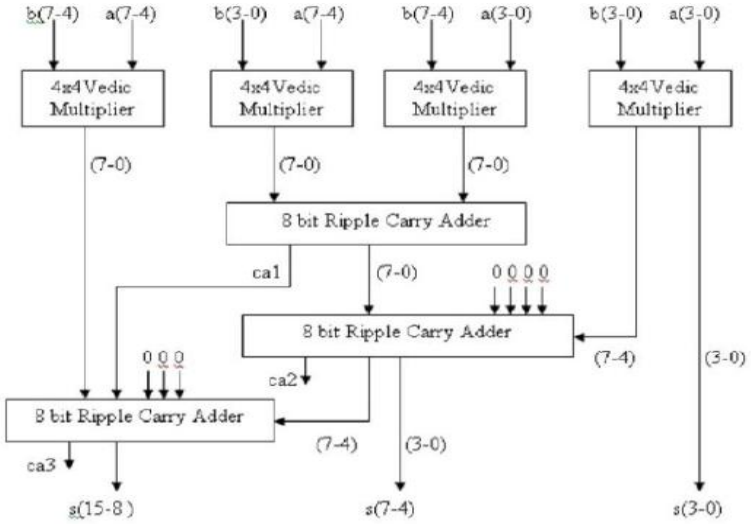

Fig 8. Architecture of 8 bit vedic multiplier

V. SIMULATION AND IMPLEMENTATION RESULTS

The simulation and implementation result of the proposed work is given here. The proposed m bit multiplier design is developed using VHDL and synthesized using XILINX 13.2 software and it is simulated in ISim for Spartan-3E FPGA series. The simulation result of 16×16 energy efficient approximate m bit vedic multiplier is shown in Fig. 9. Here in the figure m1_1 and m1_2 are the 16 bit operands and out 5 is the output. Out 3 and out4 are the two shifted outputs.

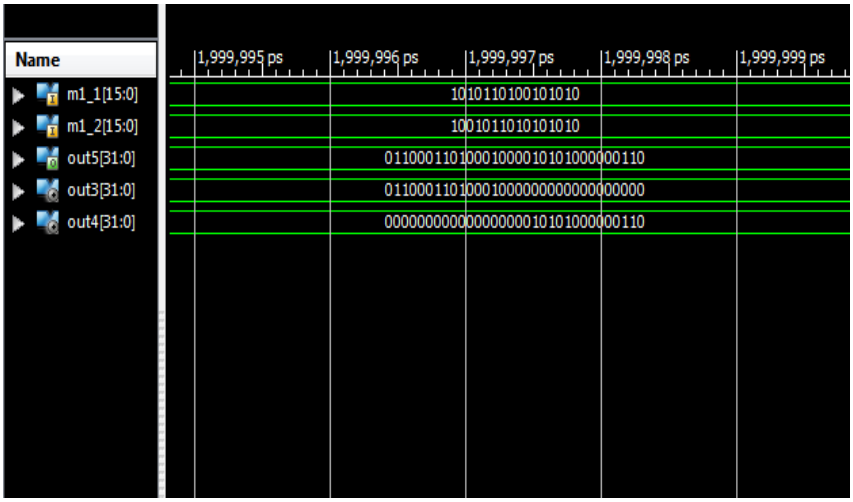

Fig 9. Simulation result of proposed multiplier

Table 1 shows the comparison of area, delay and power for the conventional 16×16 array multiplier and the proposed multiplier The number of and gates, half adders and full adders used in the proposed multiplier architecture is much less than the conventional multiplier architectures. The significant reduction in the proposed architecture offers a great advantage in the reduction of area and therefore the total power consumption. Thus the proposed m bit multiplier

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is more energy efficient than the other conventional multipliers. Also the bit reduction using m bit selection reduces the computational complexity which leads to a reduced delay and also the reduced delay vedic architecture further reduces the delay.

Design	Bits	Area (No. Of slices)	Delay (Ns)	Total power (W)
Array multiplier	16	577	67.42	0.1921
Iterative logarithmic multiplier	16	381	41.55	0.1474
Proposed m bit multiplier	16	186	37.44	0.1303

Table 1. . Comparison of Area, Delay and Power Consumption of multipliers

VI. CONCLUSION

Area, power consumption and increased delay are the constituent factors in VLSI design that degrades the performance of any circuit. This brief proposed architecture an energy efficient multiplier in which the area, delay and power consumption are reduced to a great extent on comparing with the present works. The Vedic technology adopted in the multiplier makes the architecture even faster. The reduction of number of bits which takes part in multiplication reduces the complexity of the multiplication process and thus improves the efficiency. The m bit approximate vedic multiplier can be used for various digital signal processing applications where complex computations are to be performed.

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BIOGRAPHY

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