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Type III Digital Compensator Design for Buck Converter

Shreyas R H ¹, Vishrutha G ², Shubha Rao K³

Student, Department of Electrical and Electronics, BNM Institute of Technology, Bengaluru, Karnataka, India^{1,2}
Associate Professor, Department of Electrical and Electronics, BNM Institute of Technology, Bengaluru,
Karnataka, India³

ABSTRACT: The objective of this paper is to design a type III analog and digital compensator for a buck converter and to perform a simulative analytical study. A comparison has been made and the advantages and disadvantages of each method have been highlighted. The analog controller needs a lot of calculations to determine the values of the analog components used for the compensator and if the parameters of the converter are changed, the mathematics must be re-evaluated to get the new values of the compensation components and the physical compensator must be changed. Using the type III digital compensator proposed in this paper, once the algorithm is implemented in the microcontroller/DSP controller/FPGA controller if there is a change in the converter hardware, the designer has to only deliver the new values of the components to the controller and since it is software implemented, there is no need of soldering or redesign of the board.

KEYWORDS: Buck converter; Type-III compensator; Pulse width modulation; load regulation;

I. Introduction

A Buck converter is a DC-DC voltage step down converter. It is one of the extensively used DC-DC converter topologies in power management systems, because of its high efficiency over a wide range of load current, The Buck converters are used for fast load line transient response and also for high efficiency over a large load current range. For example, in a computer motherboard the load voltage can be regulated to 5v or 3.3v to satisfy the requirements of Integrated circuits[IC] or sub-circuits. Here the voltage is constant unlike the batteries, where the voltage declines after a certain period of operation.

In this paper first a type III analog controller with its time domain transfer function and frequency response is presented. The analog compensator was designed without any adjustments but only by placing the position of the poles and zeros by a first approximation based on the buck converters passive components. The type III digital controller is obtained from the transfer function of an analog type III compensator transposed into digital using the bilinear transformation. After mathematical calculations the z coefficients for the linear difference equation needed to implement the compensator in digital domain, are obtained. These coefficients are dependent only on the pole-zero placements. The control mode used for buck converter is voltage mode control. The models are designed and simulated in MATLAB/Simulink. Static and dynamic performances of the closed loop buck converter in analog and digital domain are analyzed and the results are compared.

II. RELATED WORK

Buck converter used to supply power to a load is required to maintain the voltage constant irrespective of changes in load current and voltage. This necessitates a controller to be designed for buck converter to supply a constant voltage to a load. An extensive research is being carried out in area of control of switched mode buck converter.

The dynamic performance of the buck converter was improved by the design of discrete PID PWM controller in the paper [1]. ADC, DAC and Discrete PID controller have been implemented which is well suitable for high frequency SMPS controllers. The response of the system obtained is much faster compare to analog controller. In paper [2], A



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PID compensator control for the synchronous rectifier buck dc-dc converter is being designed. The primary idea of a synchronous buck converter is to utilize a MOSFET as a rectifier that has very low forward voltage drop in comparison to a diode rectifier. By lowering the forward voltage drop of diode, the overall efficiency for the conventional buck converter can be increased. In paper [3], Time domain design of digital compensators for pwm dc-dc converters has been successfully implemented. The system's closed loop response is largely determined by the first few samples of the step response of the compensator. Based on this conjecture, many templates can be fitted to approximate the 'ideal' compensator. Teaching "switching Converter Design" course using Problem-based learning was proposed in paper [4]. Switching converter and its controller was designed using 'sisotool' MATLAB toolbox in frequency domain.

III. BUCK CONVERTER: PRINCIPLE OF OPERATION

Buck Converter is a type of SMPS where the DC output voltage needs to be lower than the DC input voltage. Hence, a Buck Converter is also known as a Step – down Converter. It is one of the simplest SMPS power converter techniques and is often used in RAM, CPU, and USB etc. The DC input can be derived from rectified AC or from any DC supply. It is useful where electrical isolation is not needed between the switching circuit and the output. The circuit of synchronous buck converter is as shown in fig 1.

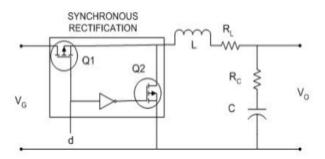


Fig 1.synchronous buck converter

When the transistor Q1 is ON and Q2 is OFF, the input voltage appears across the inductor and current in inductor increases linearly. In the same cycle the capacitor is charged. When the transistor Q2 is ON and Q1 is OFF, the voltage across the inductor is reversed. However, current in the inductor cannot change instantaneously and the current starts decreasing linearly. In this cycle also the capacitor is also charged with the energy stored in the inductor [5].

The buck converter can be operated in two modes of operation namely:

- Continuous
- Discontinuous mode.

In continuous mode, the inductor current never reaches zero and in discontinuous mode the inductor current reaches zero in one switching cycle. At lighter load currents the converter operates in discontinuous mode. The regulated output voltage in discontinuous mode no longer has a linear relationship with the input voltage as in continuous conduction mode operation [6][13].

IV. COMPENSATOR FOR BUCK CONVERTER

An open loop DC-DC converter cannot regulate its output voltage due to variation in input voltage and changes in load. Compensator is used to overcome this problem, so that the converter will produces stable output voltage.

Compensators are specialized filters. The additional component which compensates for deficient performance of the original system is known as "Compensator". Compensation is the alteration or adjustment of system to obtain desired performance. There are three types of compensator namely type-I, type-II and type-III compensator. This paper presents design of type-III compensator for buck converter both in analog domain and digital domain.



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A. Analog Type-III compensator

The type III compensator presented in figure 2 introduces two zeros and three poles. The two zeros boost up the phase with 180 degrees needed to counteract the effect of the output double pole [4][7].

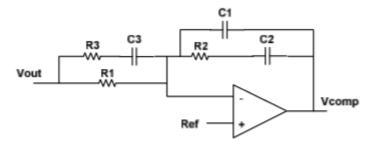


Fig 2. Type III compensator design

The transfer function for the type III converter is presented in (1).

$$H_{c}(s) = \frac{\omega_{p0}}{s} \cdot \frac{\left(\frac{s}{\omega_{z1}} + 1\right) \cdot \left(\frac{s}{\omega_{z2}} + 1\right)}{\left(\frac{s}{\omega_{p2}} + 1\right) \cdot \left(\frac{s}{\omega_{p3}} + 1\right)} \tag{1}$$

The ωp and ωz coefficients represent the angular frequencies of the poles and zeros of the compensator. For the ease of interpretation the angular frequencies are replaced by frequencies in table 1.

The link between the angular frequencies of the poles and zeros and the passive components of the type III compensator is given by (2) to (6).

$$\omega_{z1} = \frac{1}{R_2 C_1} \tag{2}$$

$$\omega_{z2} = \frac{1}{C_1(R_1R_3)} \tag{3}$$

$$\omega_{p0} = \frac{1}{R_1(C_1 + C_3)} \tag{4}$$

$$\omega_{\rm p2} = \frac{(C_1 + C_3)}{R_1 C_1 C_3} \tag{5}$$

$$\omega_{p3} = \frac{1}{R_3 C_2} \tag{6}$$

By choosing the frequencies of the poles and zeros in such a way that the system is stable and the response of the converter is fast enough at load changes one can determine the physical values of the passive components.



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Table 1 Equations of frequencies of poles and zeros

Fp0	Fp2	Fp3	Fz1	Fz2
$\frac{V_{ramp}.f_x}{V_{in}}$	F_{ESR}	$\frac{F_{sw}}{2}$	$\frac{F_{LC}}{2}$	F_{LC}

Where F_{LC} and F_{ESR} frequency of output double pole and the output capacitor and its parasitic resistance. The equation for F_{LC} and F_{ESR} is given by (7) and (8) respectively:

$$F_{LC} = \frac{1}{2.\pi \cdot \sqrt{L_o C_o}} \tag{7}$$

$$F_{ESR} = \frac{1}{2.\pi \cdot ESR \cdot C_0}$$
 (8)

 V_{ramp} is the amplitude of the saw tooth signal, f_x is the crossover frequency, V_{in} is the input voltage and f_{sw} is the switching frequency of the converter.

B. Design of type III digital compensator

Based on the analog compensator time domain transfer function and using the bilinear transformation command in MATLAB, the z domain transfer function of the digital controller is obtained as in (9) and fig.3 shows the Direct form of the IIR digital filter structure of type-III compensator[8][9].

$$H[z] = \frac{y[z]}{x[z]} = \frac{B_3 \cdot z^{-3} + B_2 \cdot z^{-2} + B_1 \cdot z^{-1} + B_0}{-A_3 \cdot z^{-3} - A_2 \cdot z^{-2} - A_1 z^{-1} + 1}$$
(9)

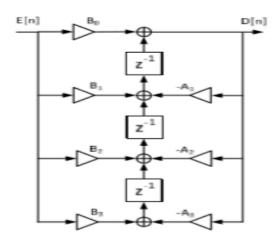


Fig.3 Direct form of the IIR digital filter structure



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V. MODELLING OF CLOSED LOOP BUCK CONVERTER

In order to analyze the performance of closed loop buck converter using type-III compensator, modeling of various sub systems was done in MATLAB/SIMULINK. The following sub sections explain the modeling of various components of closed loop buck converter [10]

A. Buck Converter Sub system

A buck converter was designed using its state equations as in Eq. (6.1), Eq.(6.2) and output equations as in (10) to (12)[11].

$$\frac{di_L}{dt} = \frac{1}{L} \left(V_g \cdot d - i_L R_L - v_0 \right) \tag{10}$$

$$\frac{di_L}{dt} = \frac{1}{L} (V_g \cdot d - i_L R_L - v_0)$$

$$\frac{dv_c}{dt} = \frac{1}{C} (i_L - i_{out})$$

$$v_0 = v_c + R_{esr} (i_L - i_{out})$$
(12)

$$v_0 = v_c + R_{esr}(i_l - i_{out}) \tag{12}$$

Where Vg is Input voltage, $d = \{0,1\}$ Switching signal, iout is Load current, Vo is Output voltage, iL is Inductor current, VC is voltage across the capacitor [12].

The modeling of the buck converter in simulink is as shown in fig. 4.

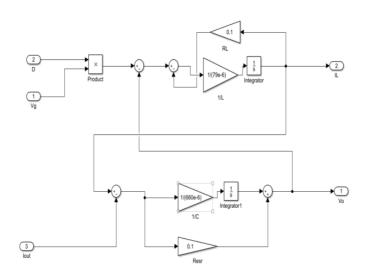


Fig. 4 Buck converter sub-system block

B. PWM Sub-systems

The Pulse width modulation (PWM) is a method of generating gate pulses of adjustable duty cycle to switches of converter. Main components of a PWM are a saw tooth waveform generator and a comparator. The PWM model in is as shown in fig. 5.



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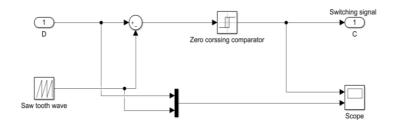


Fig. 5 Pulse width modulation sub-system block

C. Closed-Loop Analog Model of buck converter

The modeling of closed loop operation of buck converter in analog domain is as shown in fig.6. A type III compensator was designed to stabilize the closed loop operation and to obtain sufficient phase margin and band width.

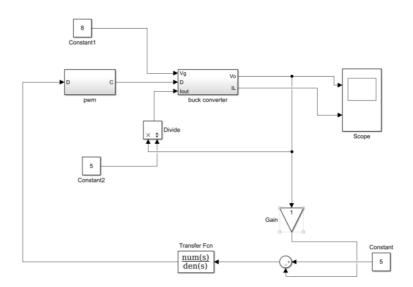


Fig. 6 Closed loop model of buck converter under analog domain

D. Digitally Controlled Buck Converter Model

A digitally controlled buck converter model in simulink is as shown in fig.7. The parts of the system that model the digital controller includes:

- A/D converter
- Discrete-time compensator, and
- Digital PWM

Analog output voltage of buck converter is compared with reference voltage to generate an error signal. An analog to digital converter is required to convert analog error voltage into digital. Then digital error signal is processed by the compensator to generate a control signal which is duty cycle value. The duty cycle value which is in digital form is converted into an analog pulse signal by Digital PWM.



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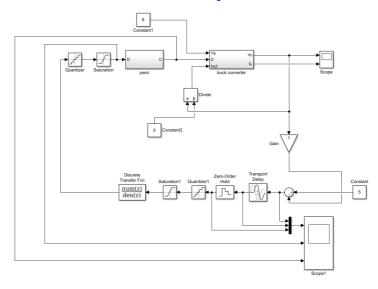


Fig. 7 Digitally Controlled Buck Converter Simulink Model

VI. SIMULATION AND RESULTS

Once the modeling of open loop buck converter, closed loop buck converter in analog and digital domain was completed, simulations were carried out to analyze and compare the performances under steady state and transient conditions. Both line and load transient conditions were considered to analyze the dynamic performance of open loop, closed loop analog and closed loop digital buck converter. A summary of simulation results were tabulated and comparison was done regarding their performances under different conditions.

Table 2 shows the specifications of buck converter system used for simulation.

Table 2 Buck converter specifications

Parameters	Value			
Output voltage (V_o)	5V			
Input voltage (V_{in})	8V			
Switching frequency (f_{sw})	100kHz			
Load (RL)	5Ω			
Output capacitance (C_{out})	680μF			
Inductance (L _{out})	79μΗ			
Capacitance parasitic resistance	0.1Ω			
(ESR)				
Saw-tooth amplitude (V_{saw})	1V			
Cross over frequency (f_x)	5kHz			



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Table 3 shows a comparison of steady state performance of open loop, closed loop analog and digital buck converter. The steady state value of output voltage in open loop configuration is found to be lesser. Ripples in output voltage and inductor current obtained lesser in all three configurations.

Table 3 Comparison table for steady state operation

$V_{in} = 8V$		$V_{out} = 5V$				
Configuration	$V_{avg}(v)$	$I_{avg}(A)$	$%V_{ripple}$	%I _{ripple}		
Open loop	4.901	0.98	0.469	24.5		
Close loop analog	5	0.99	0.45	23.5		
Close loop digital	5.02175	1.0002	0.52	27.43		

Table 4 shows a comparison of transient performance of all three buck converter configurations when line voltage variations occur. Digital buck configuration is found to be best as far as settling time is considered.

Table 4: A comparison table of line regulation performance

Variation in line regulation								
	Increase in Voltage (8-10V)			Decrease in voltage(14-12V)				
	%M _p	Ts	ΔVL	Vo	%Mp	Ts	ΔVL	Vo
Open loop	34.25	3m	1.223	6.125	6.9	4m	2.98	7.89
Closed loop analog	1.04	2.2m	0	5	4.963	2.2m	0	5
Closed loop digital	1.14	1.5m	3.25m	5.025	4.986	1.5m	3.25m	5.025

Table 5 shows a comparison of transient performance of all three buck converter configurations when load current variations occur. Digital buck configuration is found to be best as far as settling time is considered.



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Table 5: A comparison table of load regulation performance

Variation in load regulation								
	Increase in load current				Decrease in load current			
	(0.8 to 1)A				(1 to 0.8)A			
	%M _p	Ts	ΔI_{L}	Io	%M _p	Ts	ΔI_{L}	Io
Open loop	17.99	2.2m	1.5m	0.9785	34.26	2.2m	0.1675	0.8125
Closed loop analog	12.77	0.4m	1.6m	1.0015	28.265	0.4m	0.1674	0.8325
Closed loop digital	16.12	0.2m	11.95m	1.0121	31.27	0.2m	0.1603	0.8398

Fig. 8 shows the simulation results output voltage and inductor current of digitally controlled buck converter. Fig. 9 shows the ripples in output voltage and inductor current.

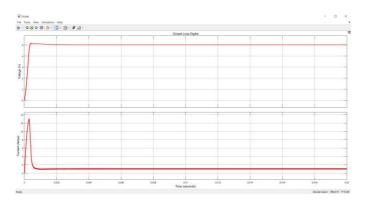


Fig. 8 waveforms of output voltage and inductor current of digital controlled closed loop buck converter.

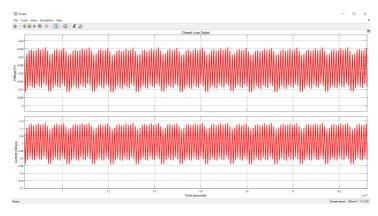


Fig. 9 ripples in output voltage and inductor current of digital controlled closed loop buck converter



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VII. CONCLUSION AND FUTURE WORK

The design of a type III digital compensator to obtain a regulated output voltage and a stable operation under load and line variations for a buck converter was completed. Both type III analog and digital compensator was designed for a buck converter.

Compared with the analog controller, the proposed digital controller needs no calculations made by the engineer if the hardware is changed, and also the compensator because it is software implemented needs no soldering or redesign of the board.

In terms of performance the analog controller is better than the digital controller but in low power designs and taking into account that the digital controller is more versatile and can deliver a stable converter without any calculation from the designer regarding the compensator, one can conclude that the digital compensator can be used successfully. The digital controller can be tuned and more features can be added to the functionality.

In conclusion the simulations results validate the method used and the designed digital controller can be used for synchronous buck converters without any further calculation as long as the parameters of the converter are delivered to the controller.

A hardware implementation of closed loop buck converter can be carried out as future scope. A comparison of performance of analog and digital controlled buck converter hardware implementations can be carried out.

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