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Low Power BIST for ALU Using LP-LFSR

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ABSTRACT: The main challenging areas in VLSI are performance, cost, and power dissipation. The demand for portable computing devices and communications system are increasing rapidly. These applications require low power dissipation VLSI circuits. The power dissipation during test mode is 200% more than in normal mode. This research article proposed a logic BIST using low power linear feedback shift register (LFSR) to generate low power test patterns. The designed architecture is programmed using VHDL and simulated using free active HDL tool. The experimental results demonstrate significant power reduction by low power TPG than compared to standard LFSR.

KEYWORDS: Low power, Test Pattern Generation, Linear Feedback Shift Register, Logic Built in Self Test, CUT.

I. INTRODUCTION

POWER dissipation is a challenging problem for today's system-on-chips (SoC s) design and test. In general, the power dissipation of a system in test mode is more than in normal mode. Four reasons are blamed for power increase during test:
1. High-switching activity due to nature of test patterns,
2. Parallel activation of internal cores during test,
3. Power consumed by extra design-for-test (DFT) circuitry, and
4. Low correlation among test vectors.

This extra power consumption (average or peak) can create problems such as instantaneous power surge that cause circuit damage, formation of hot spots, difficulty in performance verification, and reduction of the product yield and lifetime. Solutions that are commonly applied to alleviate the excessive power problem during test include reducing frequency and test partitioning/scheduling to avoid hot spots. The former disrupts at-speed test philosophy and the latter may significantly increase the time. Built-In Self-Test (BIST) is a DFT methodology that aim sat detecting faulty components in a system by incorporating the test logic on chip .In BIST, a linear feedback shift register (LFSR)generates pseudorandom test patterns for primary inputs (for a combinational circuit) or scan chain inputs (for a sequential circuit).

The presented work proposes a low power Test Pattern Generator (TPG) to reduce the dynamic power consumed by Circuit under Test (CUT). The proposed design is programmed using VHDL language and simulated using free EDA tool or Active HDL tool. The design technique increases the correlation between successive test patterns to slenderize switching activity in Circuit under Test (CUT) whichin turn decreases overall dynamic power consumption of CUT during test mode.

II. PREVIOUS WORK

There has been various low power approaches proposed to solve the problem of power dissipation during the testing. One method is to use Random Single Input Change (RISC) test generation, which is used to generate low power test pattern. In this method, power consumption is reduced but at the additional cost is between 19% to 13%. In the second method it targets the average power consumption during normal circuit operations; they do not concern the average power consumption during test.

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III. PROPOSED WORK

In the proposed approach, an LFSR act as the LPLFSR that produces the modified test vectors to minimize the switching activity and consumes less power as compared to the normal LFSR .For low power BIST circuit partitioning suitable method to reducing the power. This approach consists in partitioning the original circuit into structural sub circuits so that each sub-circuits can be successively tested through different BIST session. The idea behind the use of such a low power TPG is to reduce the number of transition on primary inputs at each clock cycle of the test session, hence it reduces the total switching activity generated in the CUT i.e ALU.

A. Proposed system architecture

a. Original Design

A typical BIST architecture consists of a test pattern generator (TPG),usually implemented as a linear feedback shift register(LFSR), MUX, CUT(ALU), BIST controller unit, comparator and ROM. The original BIST architecture and its components are given below.

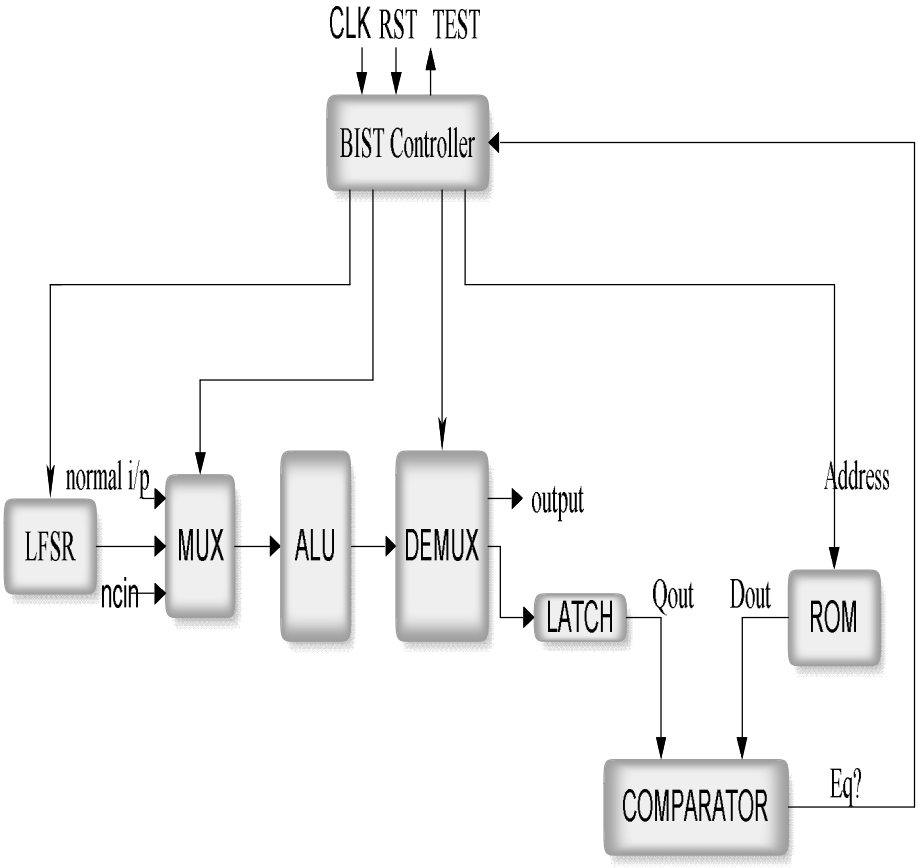

Figure1: Original BIST architecture

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b. Power Optimized Design

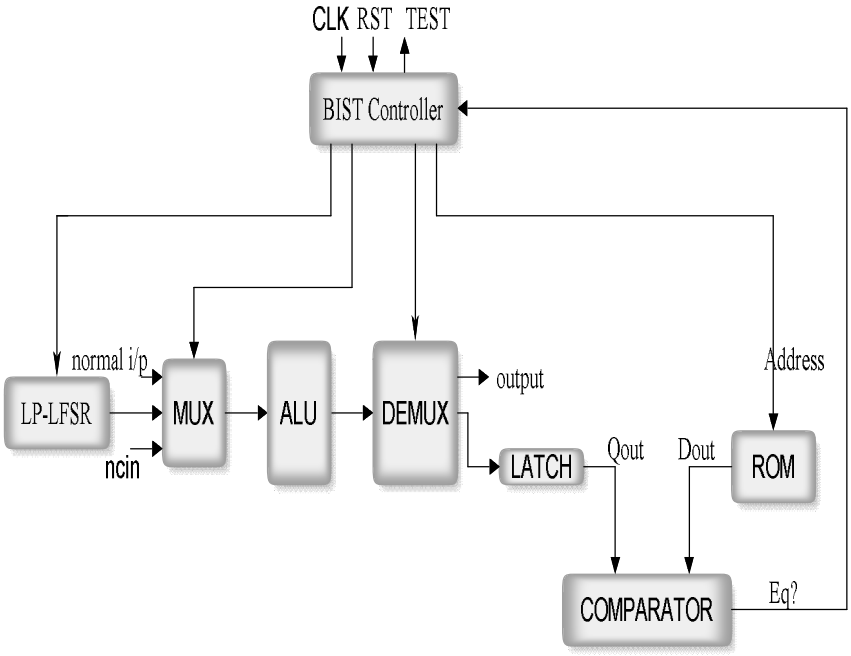

Figure2: Power optimized BIST architecture

The difference between the original and proposed design is that instead of using conventional LFSR we use low power LFSR.

Hardware Test Pattern Generator(LP-LFSR): This module generates the test patterns required to sensitize the faults and propagate the effect to the outputs (of the ALU). As the test pattern generator is a circuit (not equipment) its area is limited. Instead, the test pattern generator is basically a type of register which generates random patterns which act as test patterns. The main emphasis of the register design is to have low area yet generate as many different patterns (from 0 to 2n, if there are n flip-flops in the register) as possible.

Input Multiplexer: This multiplexer is to allow normal inputs to the circuit when it is operational and test inputs from the pattern generator when BIST is executed. The control input of the multiplexer is fed by a central test controller.

Read Only Memory (ROM):Stores the test pattern that needs to be compared with the ALU response.

Comparator*:* Hardware to compare compacted ALU response and the data which is already stored in the ROM.

Test Controller**:** Circuit to control the BIST. Whenever an IC is powered up (signal start BIST is made active) the test controller starts the BIST procedure. Once the test is over, the status line is made high if fault is found. Following that, the controller connects normal inputs to the ALU via the multiplexer, thus making it ready for operation. Among the modules discussed above, the most important one is hardware test pattern generator(LFSR).

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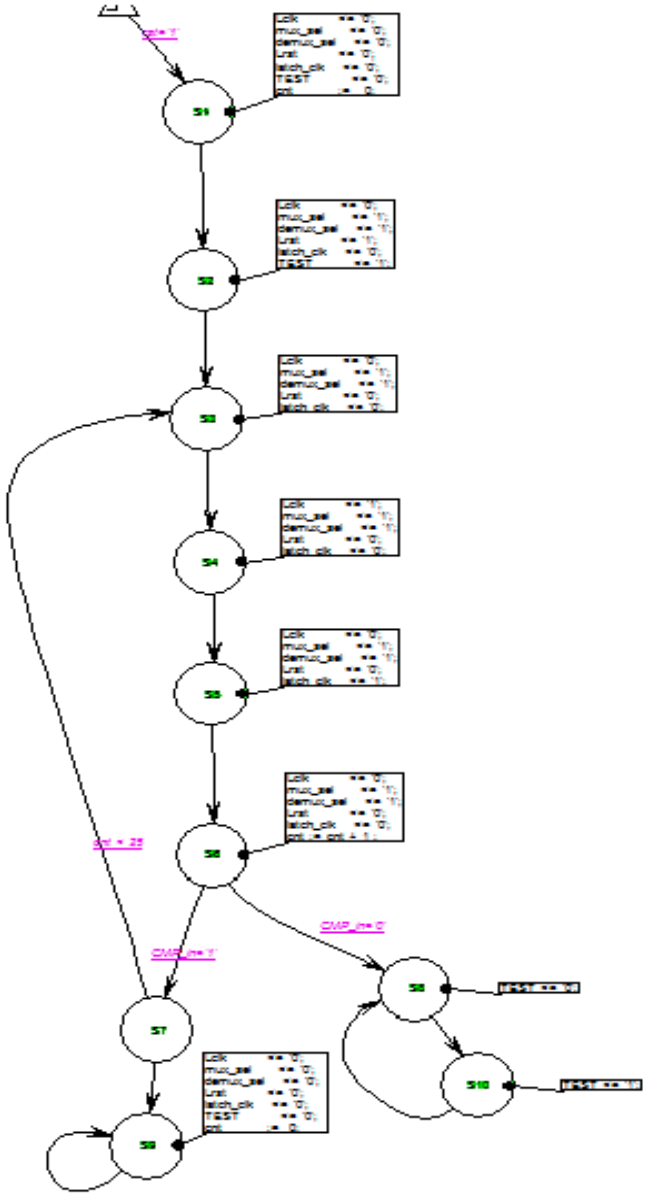

Figure3: State diagram of controller

ALU:ALU which is CUT referred to be the device under test i.e. the device which has to be tested. Here we tested the ALU. It performs the arithmetic and logical operations. DUT may be a combinational circuit or a sequential circuit. The truth table is given below:

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Select Lines				Operation performed
s(0)	s(1)	s(2)	s(3)	
0	0	0	0	a
0	0	0	1	a+1
0	0	1	0	a-1
0	0	1	1	b
0	1	0	0	b+1
0	1	0	1	b-1
0	1	1	0	a+b
0	1	1	1	a+b+cin
1	0	0	0	not a
1	0	0	1	not b
1	0	1	0	a AND b
1	0	1	1	a OR b
1	1	0	0	a NAND b
1	1	0	1	a NOR b
1	1	1	0	a XOR b
1	1	1	1	not(a XOR b)

Table1: Table of ALU operation

DEMUX: Demultiplexer is allow the output of ALU to the comparator when it is in test mode. After the testing, if the ALU is working properly it can be used for the operation. The control input of the demultiplexer is fed by the central test controller.

LATCH: Latch is used to hold the value of demultiplexer so that it cannot fluctuate.

B. METHODOLOGY:

A test controller provides all the necessary control signal to activate all the blocks.
For test pattern generator we can use LP-LFSR as it uses less power.
By selecting a control signal for mux,mux select the input from LP-LFSR for testing.
The pattern from LP-LFSR is then fed to the ALU and according to the ALU, it perform the operation and output is given to the latch.
Latch hold the output value for that particular is already stored in the ROM(Dout) get compared by using comparator.
If the Qout is equal to the Dout then it informed to the controller and again next pattern is given to the ALU.
In this way all the patterns get checked and if output is equal then we can say that ALU is working properly.
If the ALU is not faulty then test pin becomes zero that means testing is done and we can apply normal input to the ALU and we can use it.
If the design is faulty then the test pin toggle between 1 and 0.

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c. PROPOSED LP-LFSR:

Using Low power test pattern generator, a circuit's performance can be increased and switching activities can be reduced so that power dissipation will be reduced during test mode. We are going to implement a LP-LFSR techniques so that the power will reduce compared to previous works and also switching rate will be reduced in future.In the proposed LP-LFSR, only one of the flip-flops in the LFSR register is enabled or activated during each shift operation, and as a result the low power LFSR according to the invention generates the same output bit sequence as a conventional LFSR. This lower flip-flop activity causes less power loss and, further, the longer the shift register and the smaller the feedback the more efficient is the low power LFSR.

d. Conventional LFSR Architecture:

In computing, a linear-feedback shift register (LFSR) is a shift register whose input bit is a linear function of its previous state. The most commonly used linear function of single bits is exclusive- or (XOR). Thus, an LFSR is most often a shift register whose input bit is driven by the XOR of some bits of the overall shift register value. The initial value of the LFSR is called the seed, and because the operation of the register is deterministic, the stream of values produced by the register is completely determined by its current (or previous) state. Likewise, because the register has a finitenumber of possible states, it must eventually enter a repeating cycle. However, an LFSR with a well-chosen feedback function can produce a sequence of bits which appears random and which has a very long cycle.

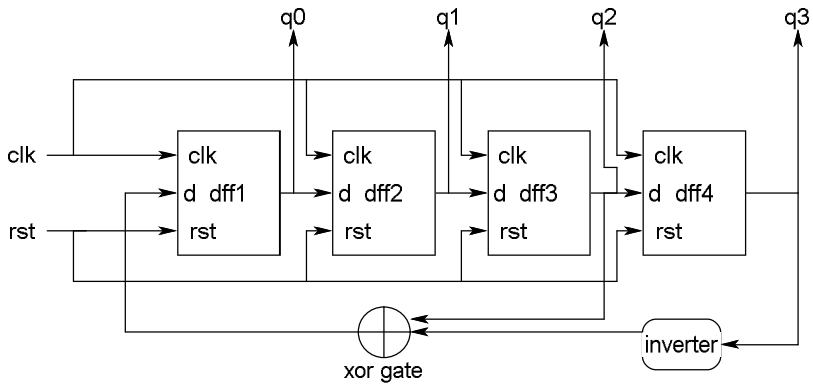

Figure4:Conventional LFSR architecture

e. Proposed LP-LFSR Architecture:

Fig. shows the schematical block diagram of an embodiment of a proposed shift register (LFSR).

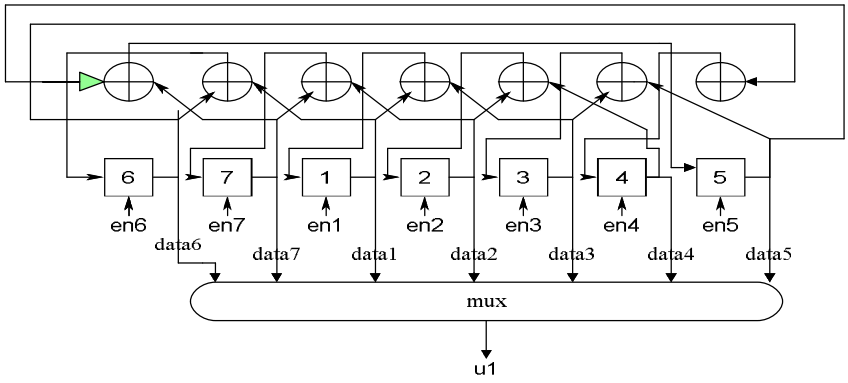

Figure5: Proposed design of low power LFSR

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A low power linear feedback shift register according to the proposed architecture, using memory means such as flip-flops not consuming power when they are disabled. The register does not shift any bits but still generates the random sequence as a conventional linear feedback shift register.
The register comprises enabling means enabling a single current memory means at every shift operation, register stages, each comprising a low power memory means consuming a minimum of power when it is disabled, and feedback means of each stage. Each memory is connected to selection means, selecting at every shift operation the output terminal of a first subsequent memory means following the current memory means being enabled at the current shift operation.

IV. SIMULATION RESULTS

4.1 Simulation result of BIST circuitfor ALU

RTL To validate the effectiveness of the proposed approach we select traditional LFSR technique for comparison, simulation and synthesis were carried out with Active HDL tool and Active HDL RTL Compiler CMOS library is used. In our experimentation we used the polynomial for both LFSR and LP-LFSR. The test patterns are generated using an LFSR written inVHDL program and block diagram. As we used 8 bit ALU as Circuit under test. Figure shows the simulation result of BIST circuit for ALU and power report extracted.

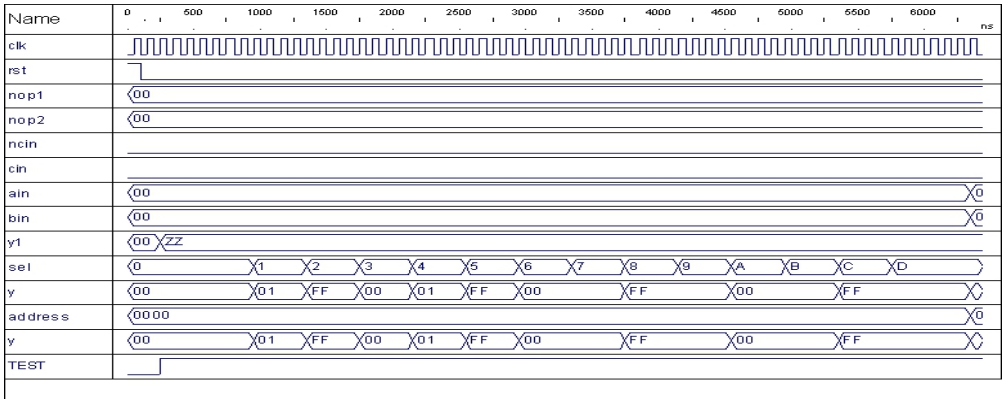

Figure6: Simulation result of BIST circuit for ALU

4.2 Power Estimation Table

Design	Technology used	Dynamic power	Cell area	Delay(slack)
Conventional LFSR	45nm	133.42uw	113.57um^(2)	1.66us
	90nm	10.82uw	291.22um^(2)	1.84us
Low power LFSR	45nm	19.68uw	503um^(2)	0.29us
	90nm	8.27uw	1205.45um^(2)	0.64us
ALU design using conv.LFSR	45nm	501uw	4606.64um^(2)	1.92us
	90nm	518.46uw	15187.4um^(2)	1.83us
ALU design using LP-LFSR	45nm	488.95uw	3799.9um^(2)	1.98us
	90nm	502.9uw	12430.5um^(2)	1.83us

Table2: Power estimation table

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The Table shows the comparison of experimental results of the test power consumption,cell area and delay with the proposed method. In Table the columns refers to the test power consumption with Standard LFSR, low power LFSR,ALU design using conv. LFSR and ALU design using LP-LFSR . It can be found that the LFSR circuit consumes 133.42 uw test power using 45nm technologywhere as the LP-LFSR circuit consumes 19.68 uwpower using 45nm technology with improvement of power consumption during testing.

V.CONCLUSION

In this paper, the BIST circuit is designed for ALU using conventional LFSR and low power LFSR.The power dissipated, cell area of LP-LFSR is less as compared to conventional one. So as the power consumed by BIST circuit for ALU using LP-LFSR is less than the BIST circuit for ALU using conventional LFSR.

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