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Low Power and Energy Efficient Logic Circuit Design by using Adiabatic Techniques

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ABSTRACT: In conventional CMOS circuits power dissipation can be reduced through adiabatic technique. By using this technique the dissipation in PMOS network can be minimized and some of energy stored at load capacitance can be recycled instead of dissipated as heat. But this technique is highly dependent on parameter variation. With the use of MICROWIND simulations, the energy consumption is analyzed by variation of parameter. The two types of adiabatic logic families, ECRL (Efficient Charge Recovery Logic) and PFAL (Positive Feedback Adiabatic Logic) are compared with conventional CMOS logic for inverter, NAND and NOR circuits. It is finding that adiabatic technique is good choice for low power application in VLSI technology.

KEYWORDS: Power dissipation in CMOS, Adiabatic Technique, Power Clock, Equivalent Circuits

I. INTRODUCTION

In conventional CMOS logic circuits, from 0 to VDD transition of the output node, the total output energy drawn from power supply and stored in capacitive network. During switching process adiabatic logic circuits reduce the energy dissipation and utilize this energy by recycling from the load capacitance. The adiabatic circuits use the constant current source power supply for recycling and it uses the trapezoidal or sinusoidal power supply voltage for reducing dissipation. During charging process of the output load capacitance the equivalent circuit is used to model the conventional CMOS circuits. But, here the constant voltage source is replaced with the constant current source to charge and discharge the output load capacitance. Therefore, the adiabatic switching technique offers less energy dissipation in PMOS network and reuses the stored energy in the output load capacitance by reversing the current source. The adiabatic Logic do not abruptly switch from 0 to VDD (and vice versa), but a voltage ramp is used to charge and recover the energy from the output.

Adiabatic circuits are also called low power circuits because they use “reversible logic” to conserve energy. While this is an active area of research, current techniques rely heavily on transmission gates and four-phased trapezoidal clocks to achieve this goal.

II. EXISTING SYSTEM

CMOS Logical Families:

The types of logic circuits are

- CMOS INVERTER
- CMOS NAND
- CMOS NOR

CMOS Inverter

It consists of only two transistors, one N-type and the other is P-type transistor. As shown in fig.1.Voltage levels at logical ‘1’ corresponds to electrical level VCC, and at logical ‘0’ corresponds to 0V or GND.RREP. Optimization function uses the individual node’s battery energy; if node is having low energy level then optimization function will not use that node.

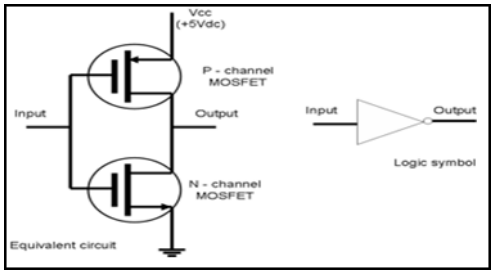

Fig. 1: CMOS Inverter

The layout of CMOS inverter is drawn according to its circuit diagram as shown in fig. 1. Here, brown color shows PMOS and green color shows NMOS, the metal1 through which they are connected is blue in color. The red color shows a polysilicon layer which is used to give input.

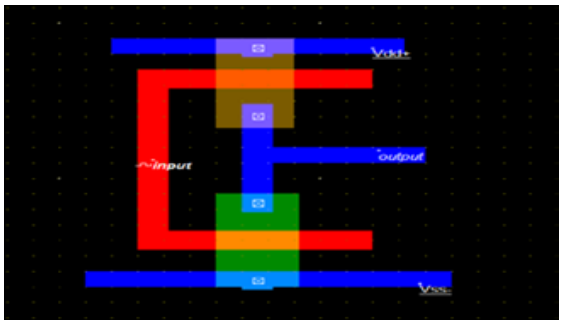

Fig. 2: Layout of CMOS Inverter

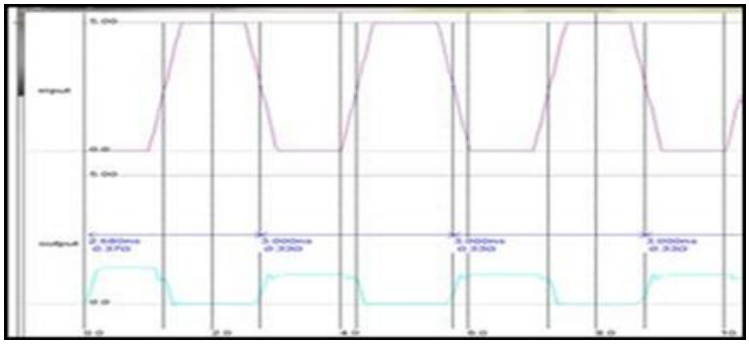

Fig. 3: Waveform of CMOS Inverter

In this simulation, it is noted that when input is 'High' the corresponding output is 'low'.

CMOS NAND

It is a logic gate which produces an output that is false only if all its inputs are true. The output results LOW(1) only if both the inputs to the gate are HIGH (1); if one or both inputs are LOW (0), a HIGH (1) output results. It is significant because any Boolean function can be implemented by using a combination of NAND gates. This property is called functional completeness. In CMOS NAND circuit, PMOS is connected in parallel and NMOS is connected in series.

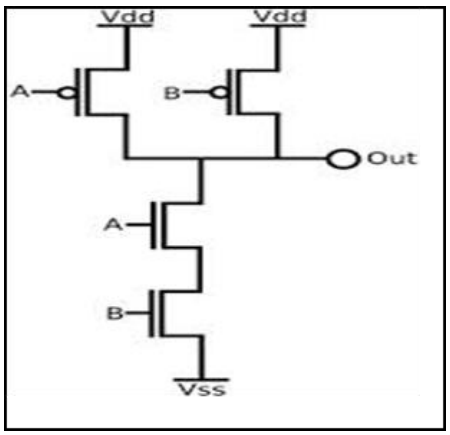

Fig. 4: CMOS NAND Gate Circuit

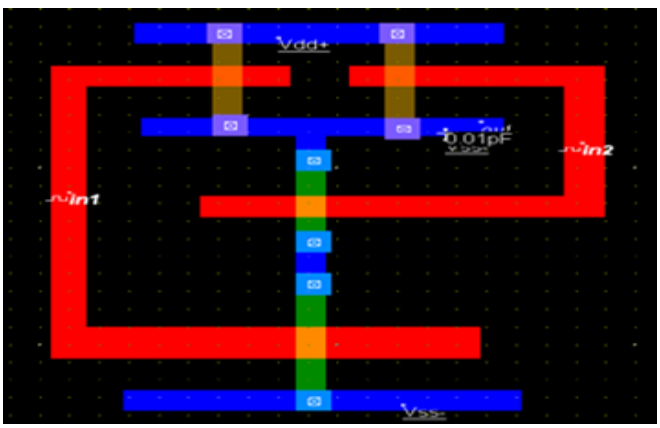

Fig. 5: Layout of CMOS NAND Gate

The layout of CMOS NAND is drawn according to its circuit diagram. In the two-input NAND gate the P-type transistors are connected in parallel between VCC and the output, while the N-type transistors are connected in series from Vss to the output.

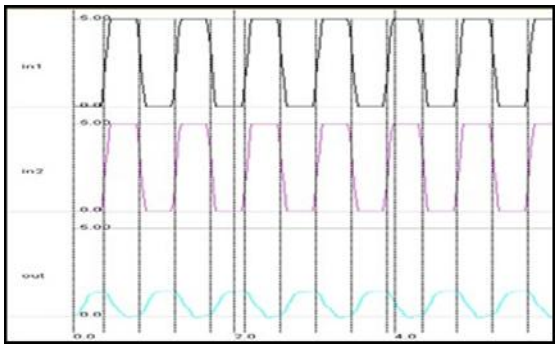

Fig. 6: Waveform of CMOS NAND Gate

In this simulation , it is seen that when both inputs are at 'High', the corresponding output is 'Low' and vice versa.

CMOS NOR Circuit

The NOR gate implements logical NOR . A HIGH output (1) results only if both the inputs are LOW (0); if one or both input is HIGH (1), a LOW output (0) results.

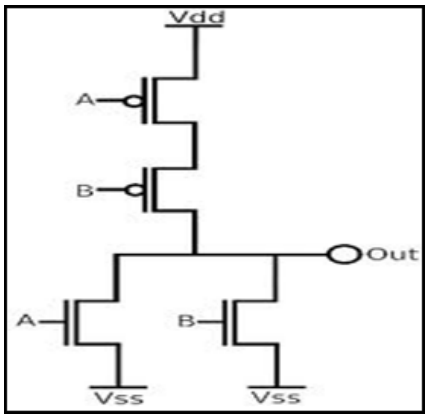

Fig. 7: Circuit of CMOS NOR Gate

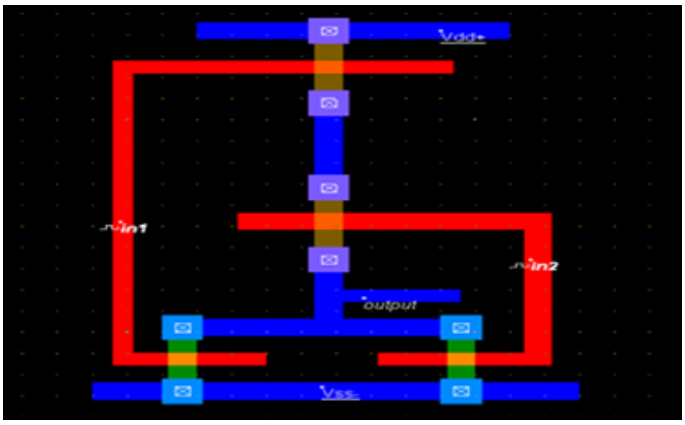

Fig. 8: Layout of CMOS NOR Gate

NOR gates can be combined to generate any other logical function. The layout of CMOS NOR is drawn according to its circuit diagram as shown in fig. 7. In two input NOR gate the P-type transistors are connected in series between VCC and the output, while the N-type transistors are connected in parallel from GND to the output

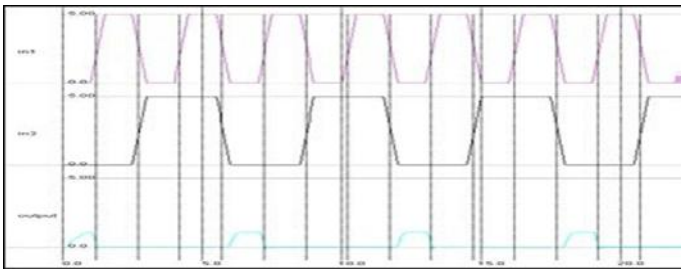

Fig. 9: Waveform of CMOS NOR Gate

In this simulation, it is seen that when both inputs are at 'Low', the corresponding output is 'High' and vice versa.

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III. PROPOSED METHOD

Adiabatic Logic Families

There are two types of adiabatic logic circuits ECRL and PFAL.

ECRL Inverter

In this two inverters are cross coupled to each other and one inverter's input is others output and vice versa

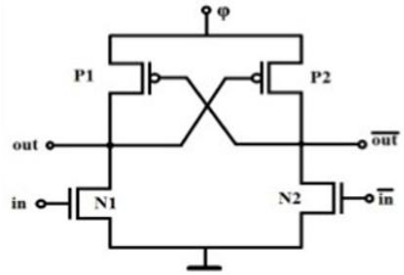

Fig 10: ECRL inverter

Layout of ECRL Inverter

The layout of ECRL inverter is drawn according to its circuit diagram. The schematic and simulated waveform of the ECRL inverter gate respectively. Initially, the input 'in' is high and the input '/in' is low.

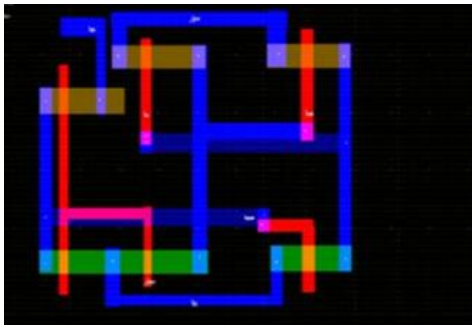

Fig11: layout of ECRL Inverter

Simulation Graph of ECRL Inverter

When the power clock (pck) rises from zero to VDD, the output 'out' remains at ground level. Output '/out' follows the pck. When pck reaches to VDD, outputs 'out' and '/out' hold logic value zero and VDD respectively. This output values can be used for the next stage as an input. Now pck falls from VDD to zero, '/out' returns its energy to pck. Therefore the delivered charge is recovered. ECRL uses four phased clocking rules for efficient recovery of the charge delivered by pck.

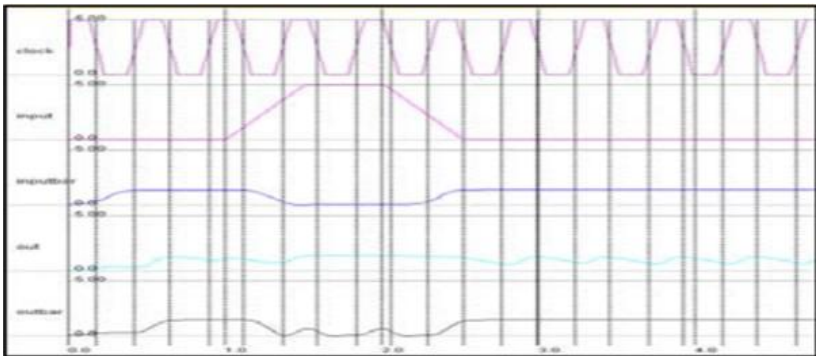

Fig 12 : Waveform of ECRL Inverter

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||Volume 9, Issue 5, May 2020||

ECRL NAND GATE

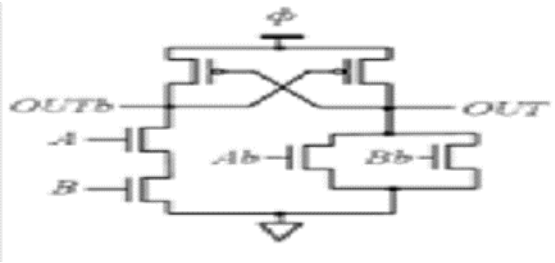

Fig 13 ECRL NAND gate

The figure shown above is ECRL NAND. The function of ECRL NAND is same as that of CMOS NAND circuit.

ECRL NAND Layout

The layout of ECRL NAND is drawn according to its circuit diagram. According to the graph, when both the inputs are low then the output is high and when both the inputs are high then the output is low. When one of the input is high and the other is low then the output is one and vice versa.

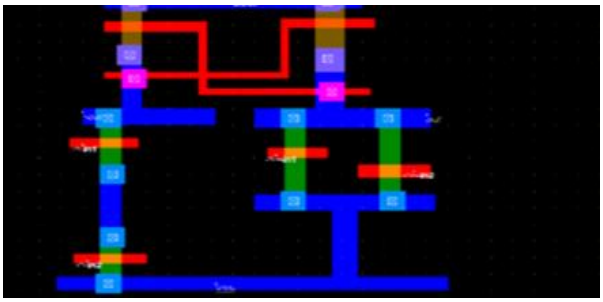

Fig 14: Layout of ECRL NAND gate

Simulation Graph of ECRL NAND

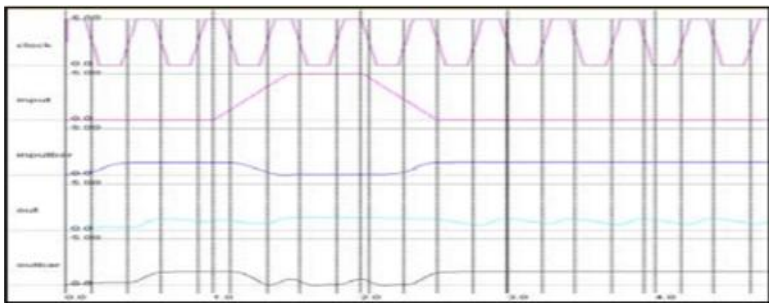

Fig 15: Waveform of ECRL NAND GATE

ECRL NOR GATE

It functions same as that of the CMOS NOR circuit

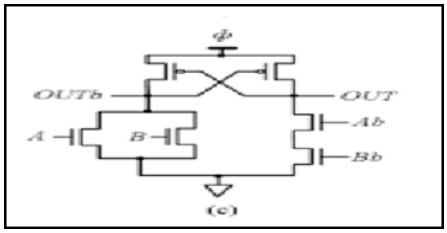

Fig 16 ECRL NOR GATE

ECRL NOR LAYOUT

The layout of ECRL NOR is drawn according to its circuit. When both the inputs are high then the output is low and when both the inputs are low then the output is high. If one of its input is high and the other is low then the output is zero.

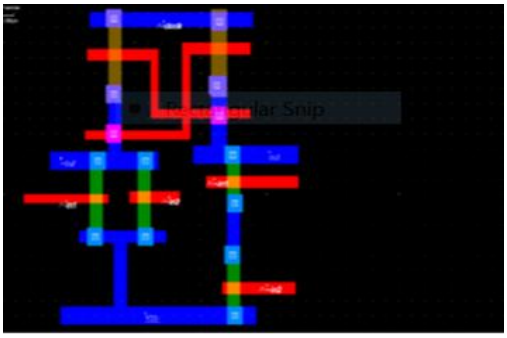

Fig17: ECRL NOR layout

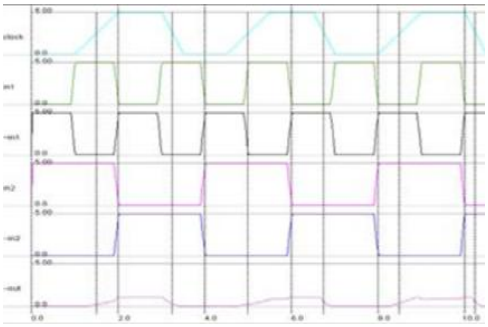

Fig18:Waveform of ECRL NOR gate

PFAL Inverter

The schematic and of the PFAL inverter gate. Initially, the input 'in' is high and the input '/in' is low. When the power clock (pck) rises from zero to VDD, output 'out' remains at ground level. Output '/out' follows the pck. When pck reaches to VDD, the outputs 'out' and '/out' hold the logic value zero and VDD respectively. This output values can be used for the next stage as an input. Now pck falls from VDD to zero and the '/out' returns its energy to pck. Therefore the delivered charge is recovered. To efficiently recover the charge delivered by pck PFAL uses four phase clocking rules.

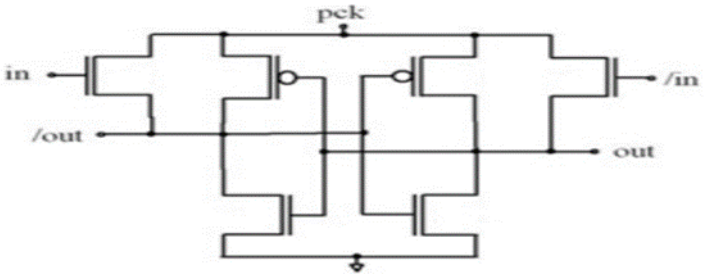

FIG 19 : PFAL Inverter

PFAL Inverter Layout

The layout of PFAL inverter is drawn according to its circuit diagram as shown in fig. 19. This simulation shows that when the input is 'High', the output bar follows the power clock and when the input is 'low', the output follows the power clock

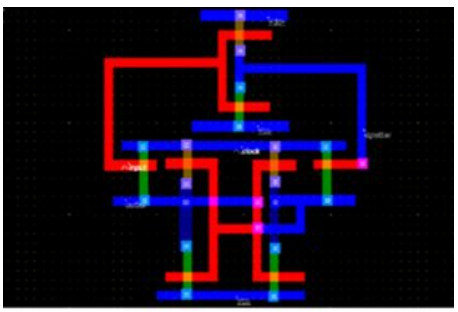

Fig 20: PFAL Inverter Layout

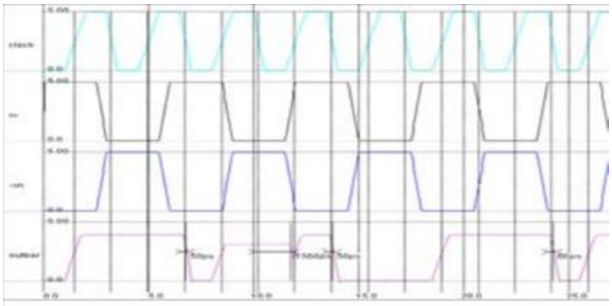

Fig 21: PFAL Inverter Waveform

PFAL NAND GATE

It consists of two inverters in which both out and /out are cross coupled to both the inverters. In the left hand side of the

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||Volume 9, Issue 5, May 2020||

inverter two NMOS are connected parallelly and in the right hand side of the inverter two NMOS are connected serially. It contains power clock and ground.

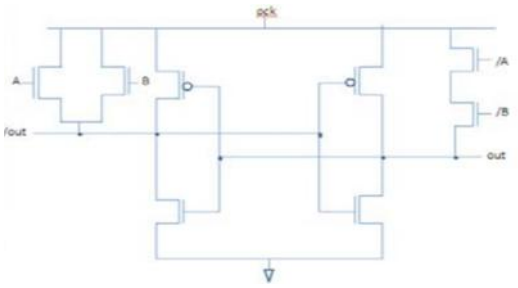

Fig 22: PFAL NAND Gate

PFAL NAND Gate Layout

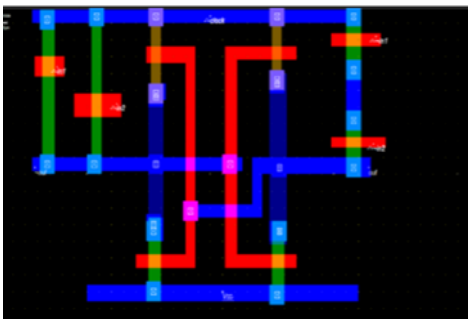

Fig 23: PFAL NAND Gate Layout

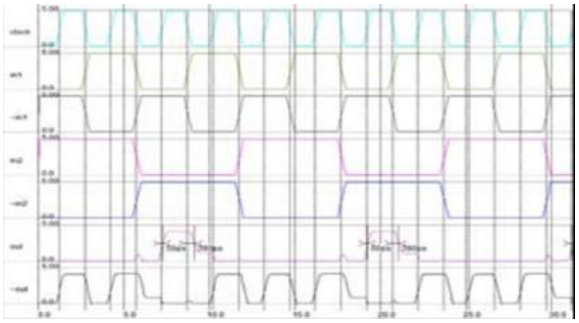

Fig 24: Waveform of PFAL NAND gate

The above layout has been designed according to the circuit. According to the graph when both the inputs are low then the output is high and when both the inputs are high then the output is low. When one of the input is high and the other is low then the output is one and vice versa.

PFAL NOR Gate

In PFAL NOR circuit two inverters are used. The outputs /out and out are cross coupled. In the left-hand side of the inverter two NMOS are serially connected and in the right hand side of the inverter two NMOS are parallelly connected.

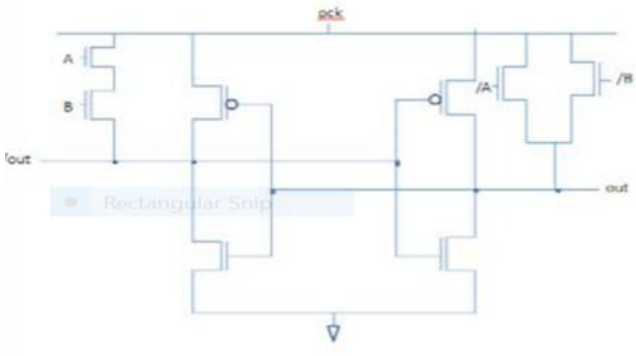

Fig 25: PFAL NOR Gate

PFAL NOR Gate Layout

The layout of PFAL NOR is drawn according to the above circuit. When both the inputs are high then the output is low and when both the inputs are low then the output is high. If one of the input is high and the other is low then the output is zero or vice versa.

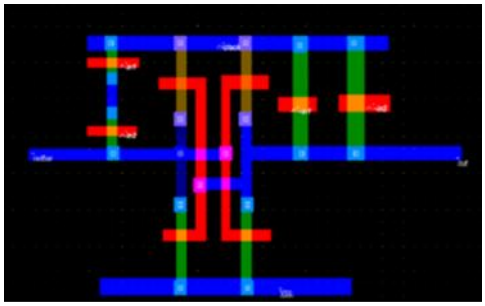

Fig 26: PFAL NOR Gate Layout

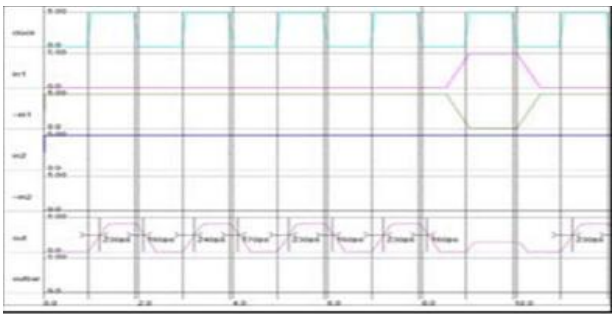

Fig 27: Waveform of PFAL NOR Gate

IV. RESULTS

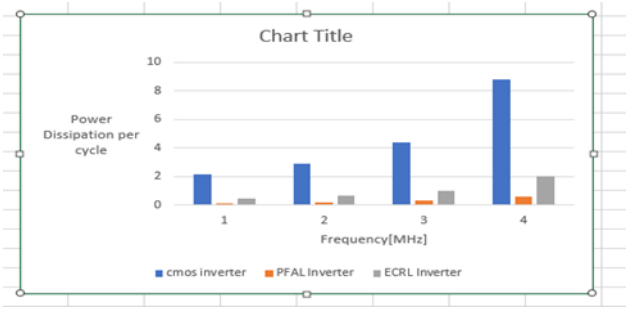

Fig 28: Comparison of Inverters

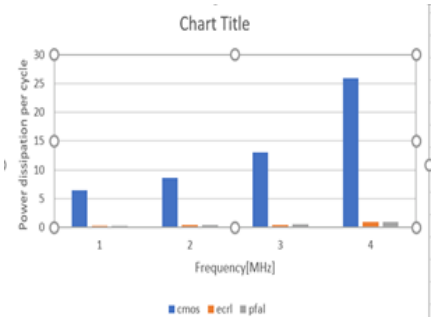

Fig 29: Comparison of NAND Circuits

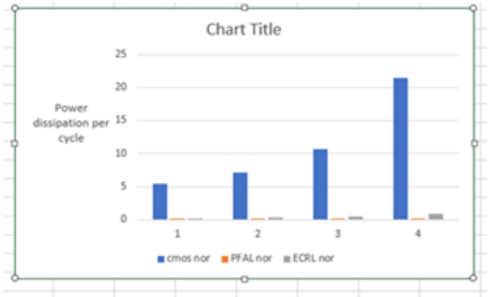

Fig 30: Comparison of NOR Circuits

V. CONCLUSION

The various parameter variations against adiabatic logic families are investigated, that shows adiabatic logic families highly depends upon its parameter variations. The less energy consumption in adiabatic logic families can be still achieved than the CMOS logic over the wide range of parameter variations. PFAL is better in energy savings than ECRL at high frequency and high load capacitance. Especially PFAL NOR produces better efficiency of power saving when compared to all the circuits. Therefore, the adiabatic logic families are used for low power application over the wide range of parameter variations.

With the adiabatic switching approach, circuit energies are conserved instead of dissipating as heat. This approach can sometimes be used to reduce the power dissipation of digital systems by depending on the applications and the system requirements.

VI. FUTURE SCOPE

In future, it is a chance of introducing more adiabatic techniques that can help to overcome the disadvantages of recent adiabatic logic circuits. For example:-DFAL (Diode Free Adiabatic Logic Circuit). Research is going on in introducing carbon nanotube based adiabatic logic. If carbon annotates becomes successors to planar CMOS transistors, they offer a tremendous energy saving impact and improved performance especially in Adiabatic Logic.

Due to their superior carrier transport they offer a small on resistance and thus exceptionally well applicable in Adiabatic Logic, where energy per operation depends not only on capacitance, as in static CMOS, but also on resistance. The study of comparisions of adiabatic logic is connected with different types of multipliers in different parameters may also be done in future.

Future work can also includes the design of larger adiabatic gates and circuits from the proposed buffer/inverter and dissipated energy analysis at higher frequencies and comparison with other adiabatic families.

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