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# FPGA Design and Simulation of Efficient Binary Image Transmission via DS-CDMA Transmitter Using Pseudo Noise Sequence Generator

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**ABSTRACT:** The paper proposes an efficient wireless transmission of binary image under high transmission rate using DS-CDMA – One of the prominent spread spectrum techniques that divide the channels into many sub channels for transmission. A detailed design of DC-CDMA transmitter using Pseudo Noise sequence Generator is implemented on Field Programmable Gate Array (FPGA) using Verilog Hardware Description Language (HDL). During data transmission of each image, the multiple access inference effect of DS-CDMA allows the data to be transmitted via sub channels usually performed using different codes generated by the PN-code generator. The design involves five separate blocks forming a digital design approach of a transmitter circuit. The blocks are the PN-code generator, Multiplexer, the Shift register, the Parity Check and the BPS modulator. The coding part is done using Verilog HDL and is further simulated using ModelSim Altera Edition 6.5b for functional simulation and verification of the logic design.

**KEYWORDS**: DS-CDMA, Spread spectrum, Multiple user inference, PN-sequence generator, BPS Modulator

## I. INTRODUCTION

In the digital cellular system, transmission of signals takes place through any type of electronic circuits. Some use passive components which need high power to drive the circuit. This in-turn may reduce the transmission rate when the transmitter operates with long time duration thus decreasing the efficiency of transmission. In addition, services provided by communication technologies (like data and voice transmission, video conferencing, Internet usage) exhibit huge data traffic and thus require a faster system to process these volumes of requests constantly in terms of quality. As digital cellular systems are more rigorous in providing multiple services to customers, multi information transmission is possible by using standards based on Multi-carriers, namely Frequency Division Multiple Access (FDMA), Time Division Multiple Access (TDMA) and the Code Division Multiple Access (CDMA). By spreading the signal (same frequency band shared by multiple signals), it allows the data to be transmitted using Direct sequence CDMA spread spectrum transmission [1, 2].

In Cellular systems the message is multiplied with spread spectrum signal (pseudo sequence) and transmitted faster when compared to transmitting a message [3]. The type of signals includes Maximum length and gold code sequence generated using LFSR's [1, 5]. The high cross correlations of the PN sequence leads to loss of signals due to interferences. The IS 95 employs Walsh codes along with PN sequence [1] which was out of synchronization when received. PN sequence generator composed of D-flip flops and XOR gates to generate spread signal [7]. The noise impacts the receiver from receiving the signals. The MS-CDMA systems degrade the performance of the subcarriers by introducing interferences and noise error [4]. For tracking quality of signal acceptance some filters are used like Multiuser Steepest Weiner LMS and structure algorithms [9]. To speed up the execution time, DS-CDMA is incorporated in the design [6, 7, and 8].

A pseudo-noise (PN) sequence have been extensively used in spread spectrum communication (SS) systems to widely spread the bandwidth of the transmitting signal where in the expansion of the bandwidth is not sufficient enough(spread spectrum), but also involves the accomplishment of the bandwidth signal with separate signatures

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known as spreading sequence. The main goal is to have a sequence randomly distributed with independent bits and no correlation between any two sequences. This helps in widely transmitting the signals, where the receiver on the other end receives these signals and continues to process.

The work proposed here is the design of DS-CDMA Transmitter. For the above reasons, DS-CDMA [10, 11 and 12] wireless transmitters are made of digital components like the flip-flops, gates etc. using FPGA. Using the spread spectrum technology, widely used in both wired and wireless network communications, spreading the signal spectrum by PN-code generator provides many advantages such as noise reduction, robustness against interfaces, less interrupts, CDMA realization and so on, thus producing higher transmission rates.

In this generation of handheld devices, the communication between the mobile handset devices and wireless base stations should take place with a same frequency spectrum. A unique code sequence is to be broadcasted between the wireless base stations and the handset devices. Such a unique code sequence is also called as Pseudo noise code generated by a Pseudo noise code generator using 8 bit LFSR's. The modulation of the carrier signal is achieved using a Binary Phase shift keying Modulation technique. Different code sequences from different handheld devices are broadcasted to the Base station. The Base station must have the capability to discriminate these code signals to differentiate among their transmissions from the other.

The paper includes the following sections: In Section III, we explain the design and implementation of CDMA transmitter. Section IV explains the Results of our implementation. Section V provides the Conclusion.

## II. DESIGN AND IMPLEMENTATION OF DS-CDMA TRANSMITTER

Transmission of a binary image through DS-CDMA is in demand by the users over the communications channels via internet, satellite and so on. The transmission is simulated at different stages – Bit stream data buffer surface creation (Data Sampler), spreading and Modulation. First step is converting the image into binary signals. It also uses the Master clock to generate different clock signals which in turn is used in generating the spread spectrum signal. Later m-sequences are generated based on the number of users. The DS-CDMA transmitter design comprises of very important block namely PN sequence generator.

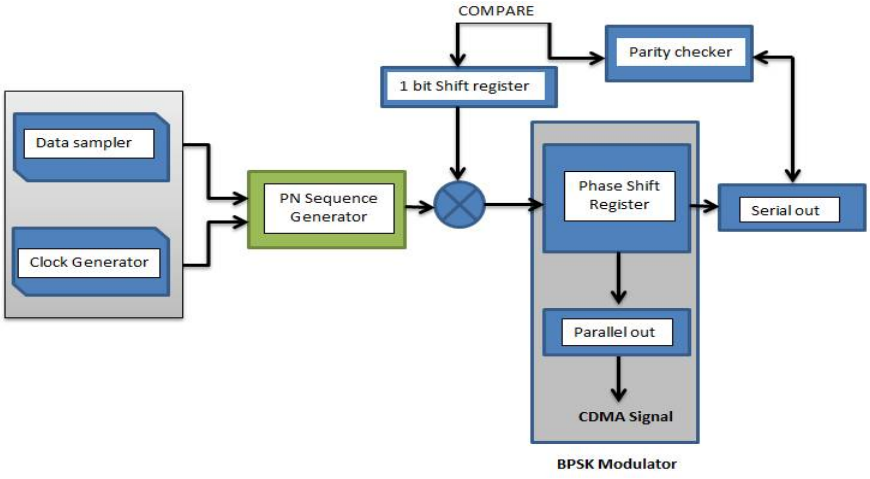


Figure 1: CDMA Transmitter Block Diagram

This block is used to generate various PN sequences using 8 bit LFSR's. In the paper we consider two types of PN sequences generators, one is the Maximum length sequences (ML) and the other Gold code sequences. Since the LFSR used here is 8 bit implementation, the ML sequence length is 255 i,e 2n-1 where n is 8. So it can support 255 communication links. The gold code sequence generator uses two PN sequence generators resulting in a pair of sequences which is then operated by an XOR operation to get the output sequence. It has good cross-correlation properties and hence most preferred. The Shift register is used to shift input data from the PN sequences by one position which can have both serial and parallel inputs and outputs. We use both Serial in parallel out conversion and

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parallel in serial out conversion. Serial to parallel conversion converts serial data into parallel data format. It is performed by clocking in single bit stream into a register and shifting each bit in turn until the register is full. Parallel to Serial Conversion is a way to convert a parallel data into a serial format. Parallel-in/ serial-out shift register stores data into all stages, shifts it on a clock by clock basis, and delays it by the number of stages times the clock period.

Later Parity checker is used to ensure the data transmission between the nodes during communication is accurate. Final step is the Modulation. A simplest form of phase shift keying is the BPSK Modulation. It modulates the spreaded signal by producing a band pass spread signal which is suitable for transmission. Later with reconstruction of these transmitted signals, the exact binary signals were received via the DS-CDMA at the receiver and bit stream buffer of the image was reconstructed. The main blocks of the DS-CDMA transmitter are shown in the fig. 1. These blocks are implemented using Verilog HDL. Verilog HDL programs are the source codes written using the normal TEXT editor which is then saved as a VHDL file and complied to see if any errors. If the compilation shows no error(s), the file is further simulated using ModelSim Altera Edition 6.5b for functional simulation and finally the verification of the logic design is implemented with FPGA.

## III. EXPERIMENTAL RESULTS

As the above section describes the design and implementation of the DS-CDMA transmitter, transmission is simulated at different stages. The Simulation result of each block is shown in this section. Fig. 2 describes the wave form of 8-bit linear feedback shift register. It helps supporting 255 communication links.

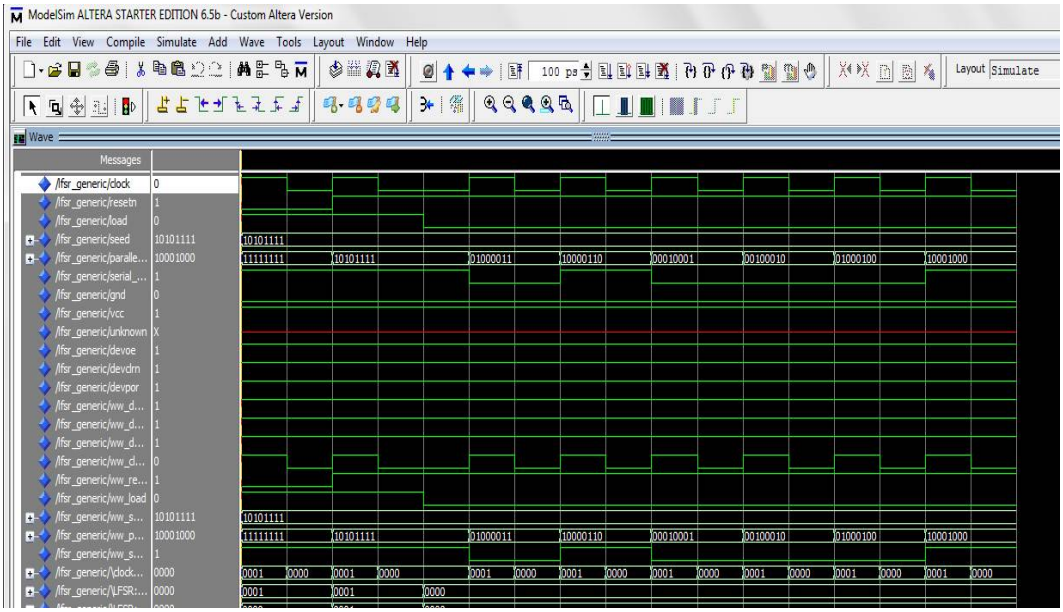


Fig. 2. Wave form of 8-bit Linear feedback shift register

The Shift register is used to shift input data by one position and helps pass sequences of inputs to Serial-in-Parallel or Parallel-in-serial blocks. The Fig. 3 and 4 represents the wave forms of Serial-in-Parallel and Parallel-in-serial conversion respectively.

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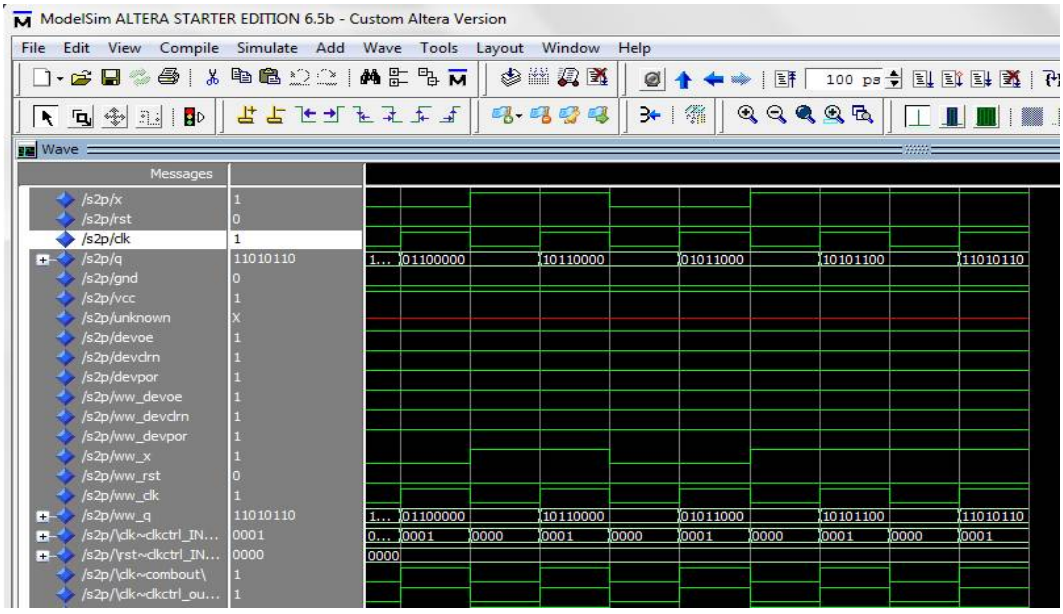


Fig. 3. Wave form of 8-bit Serial to parallel conversion

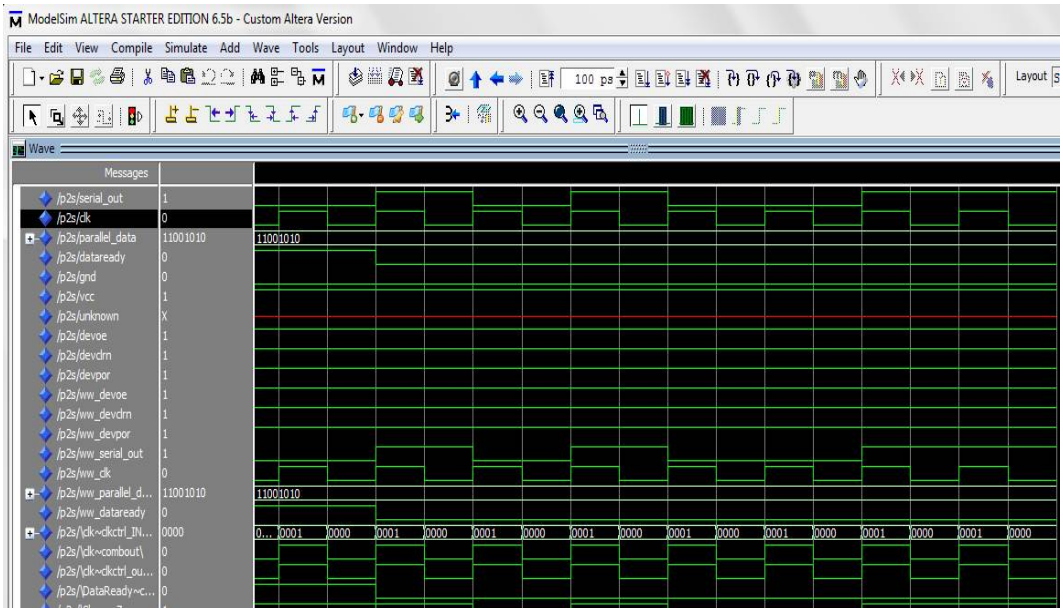


Fig. 4. Wave form of Parallel to Serial Conversion

Later Parity checker is used to ensure the data transmission is accurate between the nodes during communication. The fig. 5 and fig.6 represents to wave form of Shift register and Parity checker respectively. Thus the DS-CDMA transmitter blocks are implemented using Verilog HDLand simulated using ModelSim Altera Edition 6.5b.

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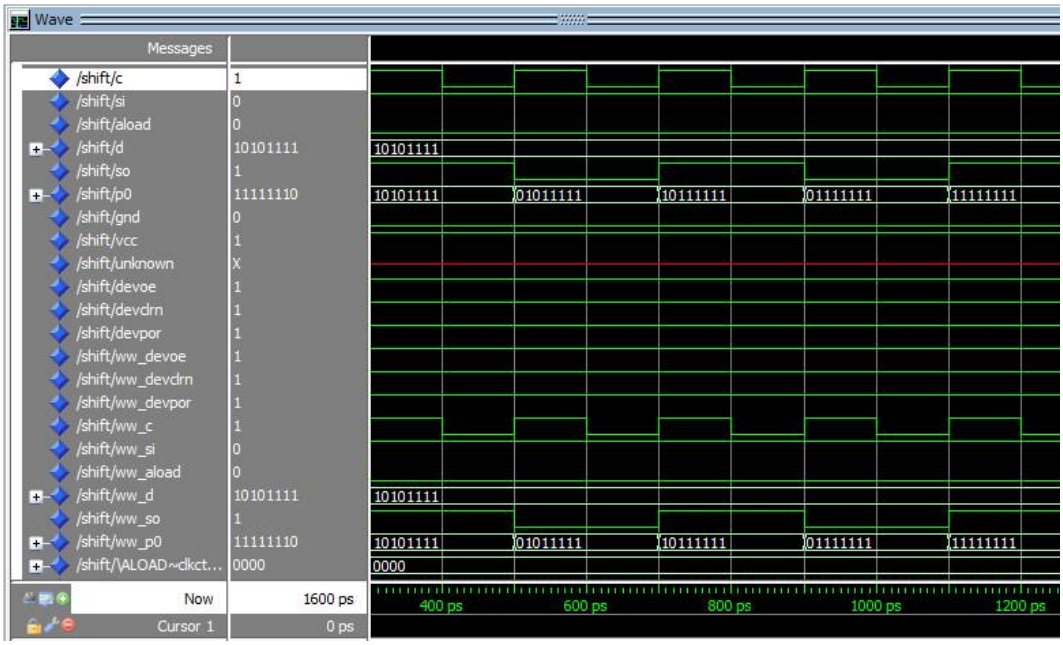


Fig. 5. Wave form of Shift Register

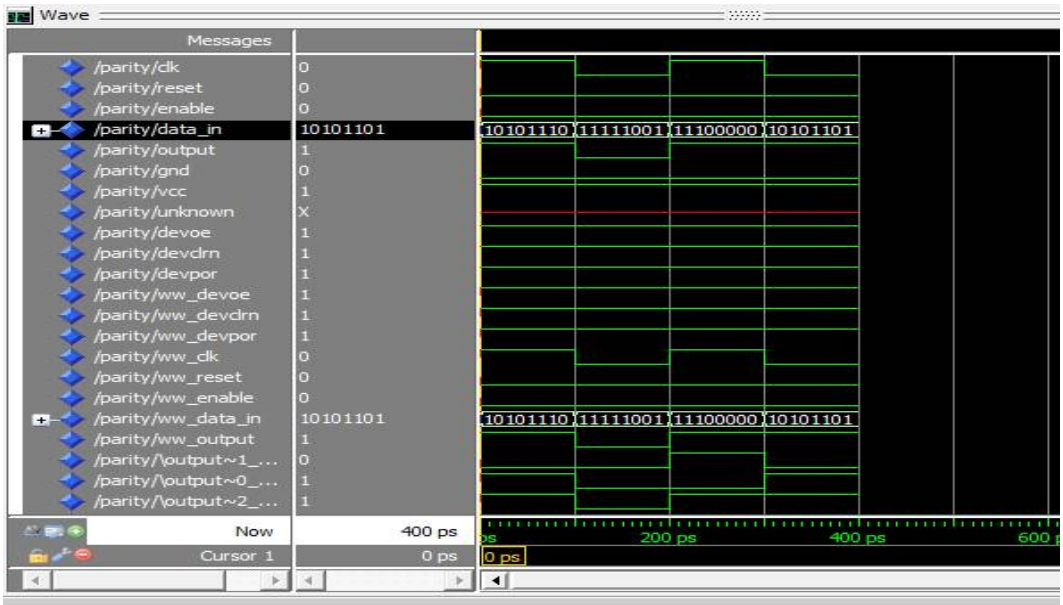


Fig. 6. Wave form of Parity Checker

## IV. CONCLUSION

The implementation of the DS-CDMA transmitter modules are presented in this paper. DS-CDMA acts as a very important multiple access technique enhancing the capability of increasing the number of bits through which the PN sequence can be changed very easily. In our implementation we have 8-Bit LFSR used to generate the ML and gold code sequence with 255 communication links. An arbitrary binary image data stream was chosen and tested against the implemented transmitter and observed the multi access inference quality of DS-CDMA transmission successful. Also

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the reconstructed binary signals received via the DS-CDMA at the receiver matched with the transmitted signals and data stream buffer of the image formed after reconstruction matched with the original. Design is completely reconfigurable and can be used for both FPGA and ASIC implementation.

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