IJIRCCE

e-ISSN: 2320-9801 | p-ISSN: 2320-9798

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN COMPUTER & COMMUNICATION ENGINEERING

Volume 12, Issue 1, January 2024

INTERNATIONAL STANDARD SERIAL NUMBER INDIA

Impact Factor: 8.379

International Journal of Innovative Research in Computer and Communication Engineering

| e-ISSN: 2320-9801, p-ISSN: 2320-9798| www.ijircce.com | |Impact Factor: 8.379 | A Monthly Peer Reviewed & Referred Journal |

|| Volume 12, Issue 1, January 2024 ||

| DOI: 10.15680/IJIRCCE.2024.1201067 |

Based on Domino Logic Technique Using EDA Tool

K. Sneha[1] , Mrs. S.I. Padma[2], Dr. K. Madhan Kumar[3], Mrs. X.M. Binisha[4]

PG Scholar [Communication System], Department of ECE, PET Engineering College, Vallioor, Tamilnadu, India[1]

Associate Professor, Department of ECE, PET Engineering College, Vallioor, Tamilnadu, India[2]

Professor, Department of ECE, PET Engineering College, Vallioor, Tamilnadu, India[3]

Assistant Professor, Department of ECE, PET Engineering College, Vallioor, Tamilnadu, India[4]

ABSTRACT: In modern VLSI area efficient devices are most used because most of the devices are becoming portable. The Domino logic technique is often employed in designing the area efficient and high-speed devices. In this research paper, one-bit full adder circuit using CMOS based logic and domino-based on Microwind EDA Tool has been designed based on 0.18um technology having the supply voltage 3V. This research paper is mainly centralized on the design of area efficient and fast speed device. This work evaluates the performance CMOS and Domino logic based on full adder circuit in terms of delay and power consumption. It was found that Domino logic based one-bit full adder circuit based on CMOS logic.

KEYWORDS: Full Adder, Domino Logic, CMOS Logic.

I. INTRODUCTION

In the fast-growing VLSI industry, transistor density is increasing with rapid rate day- by-day. According to Moore's law transistor density will get doubled itself after every eighteen months As the number of transistors will increase, correspondingly area, delay and power consumption of the device will also increase. So, a technology is required by which the area can be reduced and increase the performance of the device. From the past few decades CMOS technology is being used for designing the chips in semiconductor industry, but as the number of transistors are increasing, area of the device and delay both are increasing. So, it requires switching to a technology, which uses lesser area and smaller delay. Hence, the Domino logic is used for designing the one-bit full adder and compared the various performance parameters like area, delay, and power consumption in both technologies.

A. Adder:
A circuit that adds numbers is called an added. It calculates address, table indices, and other like operations.

B. Full Adder:
Full adder is an arithmetic circuit that is used in many IC design. The block diagram of full adder is shown above. It has 3 input and 2 output.

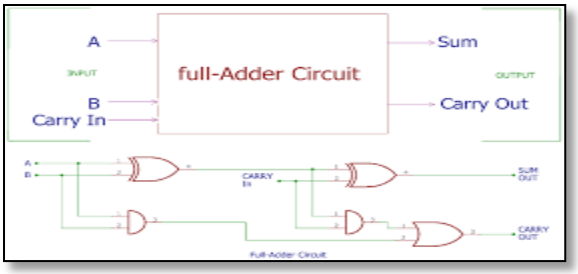

Fig 1: Full adder circuit

| e-ISSN: 2320-9801, p-ISSN: 2320-9798| www.ijircce.com | |Impact Factor: 8.379 | A Monthly Peer Reviewed & Referred Journal |

|| Volume 12, Issue 1, January 2024 ||

| DOI: 10.15680/IJIRCCE.2024.1201067 |

➢ XOR gate:

XOR is the inequality function's representation. The output of this unique kind of logic is true even in cases where the inputs disagree. The outcome is false despite the identical inputs. Three fundamental gates are combined to create an XOR gate:(AND, OR, and NOT gates).
By properly designing the XOR gate, the total adder's power consumption will be reduced. The application-oriented digital circuits design is implemented via XOR.

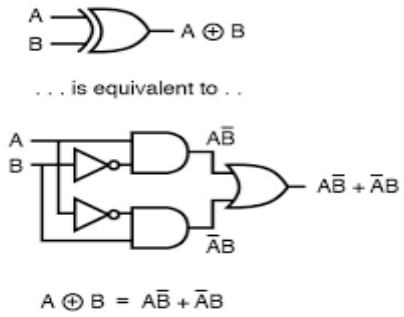

Fig 2: XOR Gate

Power dissipation:

In order to build any circuit, power dissipation is crucial. There are two main groups in terms of power.

1. First among them is Static Power Dissipation.
2. Dissipation of Dynamic Power
3. Dissipation of electricity in short circuits.

Static Power:

Static power is the power it can be seen that one of the transistor is always off when the gate is in either of logic states. and is generally determined by the formula.
Pstatic=Istatic.Vdd

Dynamic Power:

The assumption used to estimate dynamic power dissipation is that the step input's rise and fall times will be significantly longer than the repetition period.

Pcap + Ptransient = (CL + C)(Vdd)^2fN^3 is Pdynamic.

Shot Circuit Dissipation:

It depends upon charge of capacitor. Because of capacitive dissipation, the power becomes less significant as the load capacitance increases.

Pshort=Ishort.Vdd in Pd.

Delay:

The delay can be expressed as the mean of the high-to-low and low-to-high times, and is commonly calculated using the formula Tp=t(PLH)+t(PHL) / 2.

| e-ISSN: 2320-9801, p-ISSN: 2320-9798| www.ijircce.com | |Impact Factor: 8.379 | A Monthly Peer Reviewed & Referred Journal |

|| Volume 12, Issue 1, January 2024 ||

| DOI: 10.15680/IJIRCCE.2024.1201067 |

II. PROPOSED METHOD

In this project, we'll use a variety of XOR gate approaches to create a low-power complete adder. The following six methods for reducing power and delay are:

1. CMOS logic, or complementary metal oxide semiconductor
2. Logic for transmission gates (TGL)
3. PTL, or pass transistor logic
4. Logic of Dominos
5. Domino Logic with Dual Rails
6. DPL, or double pass transistor logic.

1. CMOS logic

By combining the NMOS and PMOS devices on one substrate, CMOS can be produced. It is impervious to conditions where noise occurs. Moreover, integrated circuits, microprocessors, and microcontrollers are designed using it. The robustness against voltage scaling is provided by the CMOS. It had excellent dependability and used the fewest possible transistors to deliver the necessary power.

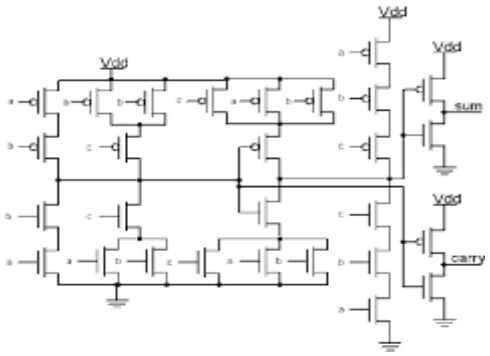

Fig 3: CMOS Full adder

2. Transmission Gate Logic:

A transmission gate functions similarly to a relay in that it can be blocked by a control signal at nearly any voltage potential or conduct in both directions. The Zhuang full adder is the name given to the Transmission Gate Logic full adder. The CMOS-based transmission gate switch allows NMOS to pass strong 0 but poor 1 and PMOS to pass strong 1 but poor 0.Both transistors can conduct when the gate is activated, which happens when the control voltage is high. The maximum voltage level at the output is provided by TGL. because it uses almost half the ability of a typical full adder.

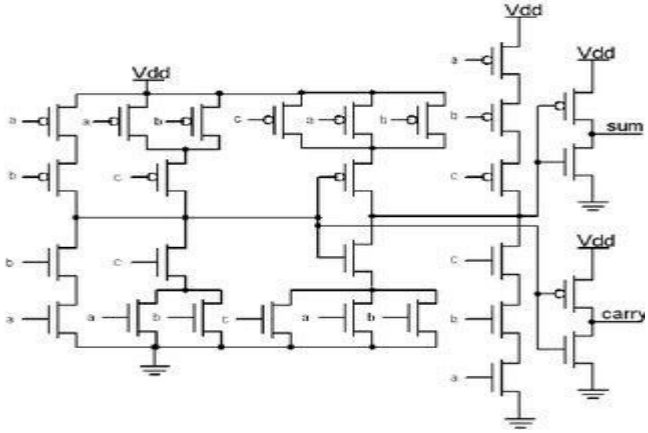

Fig 4: TGL Full adder

| e-ISSN: 2320-9801, p-ISSN: 2320-9798| www.ijircce.com | |Impact Factor: 8.379 | A Monthly Peer Reviewed & Referred Journal |

|| Volume 12, Issue 1, January 2024 ||

| DOI: 10.15680/IJIRCCE.2024.1201067 |

3. pass transistor logic

The term pass electronic transistor logic (PTL) refers to a variety of logic families used in integrated circuit design. By removing the need for transistors, it lowers the number of transistors required to create whole distinct logic gates.
Rather than being connected as switches to provide voltages, transistors are employed as switches to transfer logic levels between nodes in a circuit. As a result, there are fewer active devices.

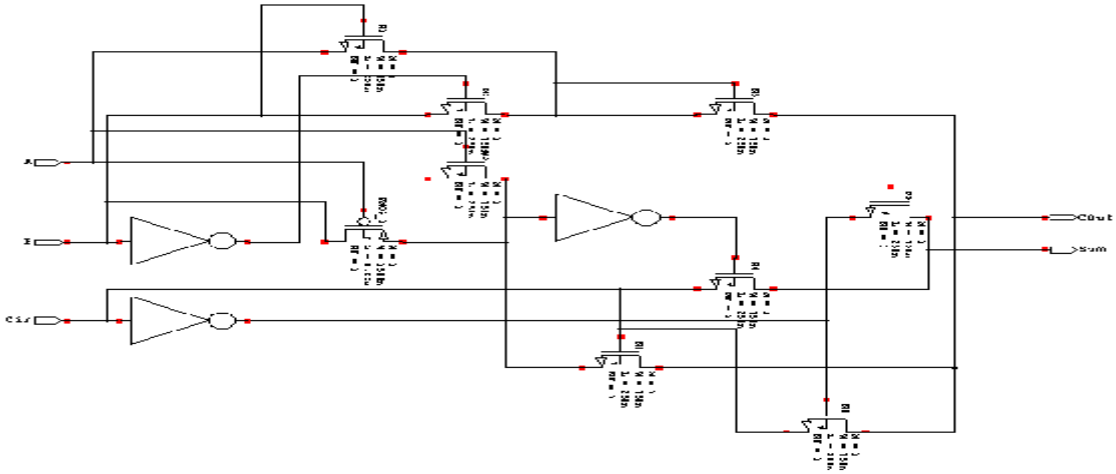

Fig 5: PTL logic gate

4. The Domino Theory

Dynamic logic may have evolved into domino logic, a CMOS-based approach. Only the clock signal matters. Only a transistor used as a precharged and evaluation switch is determined by the clock signal. It had been designed to hurry up circuits, finding the premature cascade downside, generally by adding tiny and speedy pFETs between domino stages to confine the interstate cascade rate to a curtailed a not require clock interlocks.

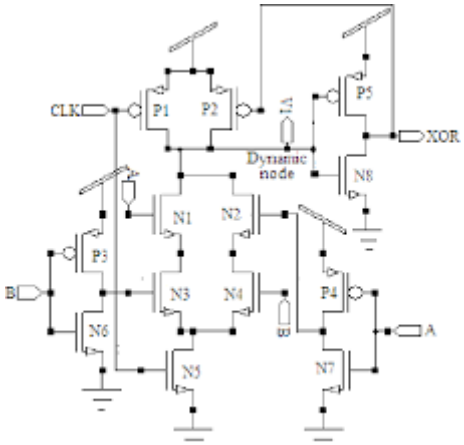

Fig 6: Domino logic full adder

5. Domino logic with dual rails

The clocking power is added to the dual rail domino's inverting and non-inverting operations. First of all, stage i+1 is in evaluation while stage I is still in control if the clock for stage i+1 arrives earlier than the clock for stage I. When the gate terminal of the NMOS transistors used in stage i+1 receives the "precharged" output of stage I, the NMOS transistors are turned ON, causing the output of the NMOS Block to discharge and stay at logic low indefinitely. This prevents the NMOS block from simulating the necessary functionality.

| e-ISSN: 2320-9801, p-ISSN: 2320-9798| www.ijircce.com | |Impact Factor: 8.379 | A Monthly Peer Reviewed & Referred Journal |

|| Volume 12, Issue 1, January 2024 ||

| DOI: 10.15680/IJIRCCE.2024.1201067 |

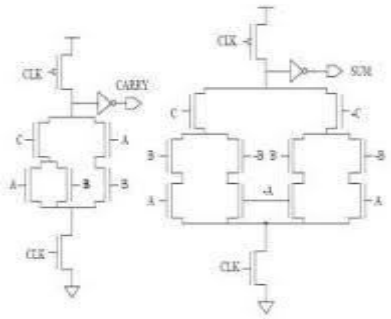

Fig 7: DRDL Full adder

6. Logic for Double Pass Transistors

An alternative to CPL in the PTL family is DPL. This solves the threshold drop issue and the need to invert after every block. DPL has been demonstrated to improve circuit performance at lower offer voltages. Its double transmission properties and symmetrical arrangement increase gate speed without raising input capacitance. We suggest utilizing CMOS double pass junction transistor logic to enforce a differential logic unit. The proposed logic unit (LU) is a small, low-power transistor variant. It uses only sixteen transistors to accomplish eight logic tasks.

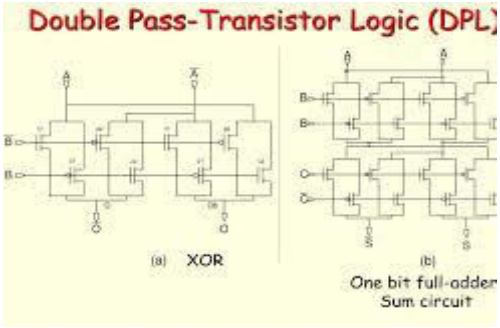

Fig 8: DPL Full adder

III. RESULT AND DISCUSSION

The MICROWIND tool was used to create the circuit for the six distinct power and delay reduction strategies of the complete adder with XOR gate. Micro wind EDA editor was used to generate the circuit's architecture, and each style's functions were confirmed.

International Journal of Innovative Research in Computer and Communication Engineering

| e-ISSN: 2320-9801, p-ISSN: 2320-9798| www.ijircce.com | |Impact Factor: 8.379 | A Monthly Peer Reviewed & Referred Journal |

|| Volume 12, Issue 1, January 2024 ||

| DOI: 10.15680/IJIRCCE.2024.1201067 |

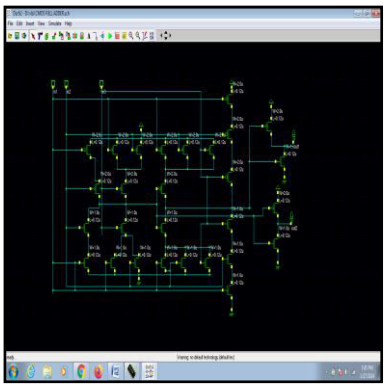

Fig:CMOS full adder circuit

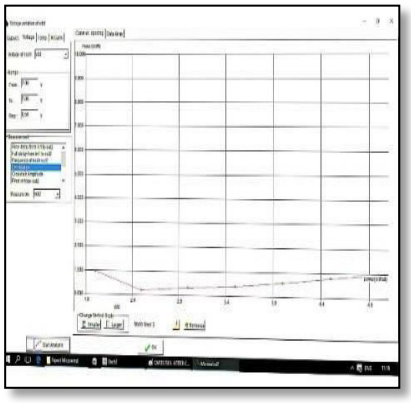

Fig: power dissipation of CMOS

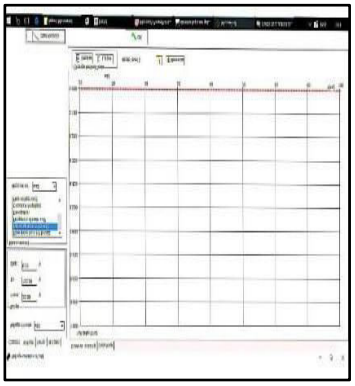

Fig: Delay of CMOS full adder

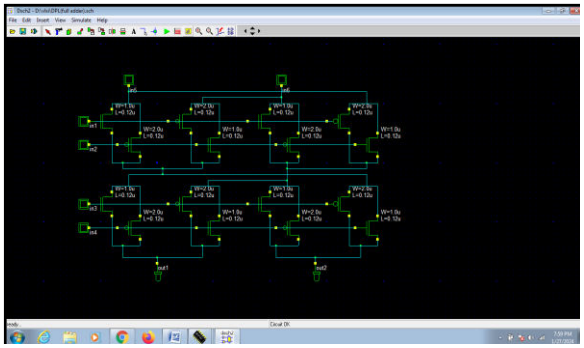

Fig: DRDL full adder circuit

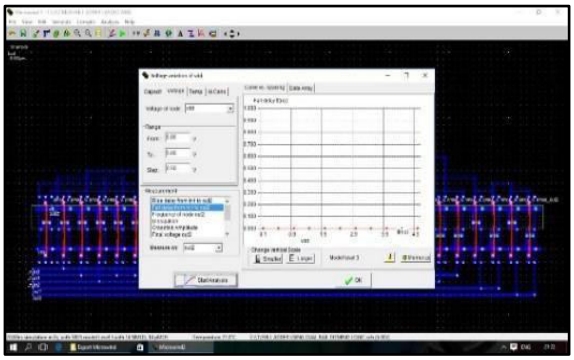

Fig : DPL power and delay

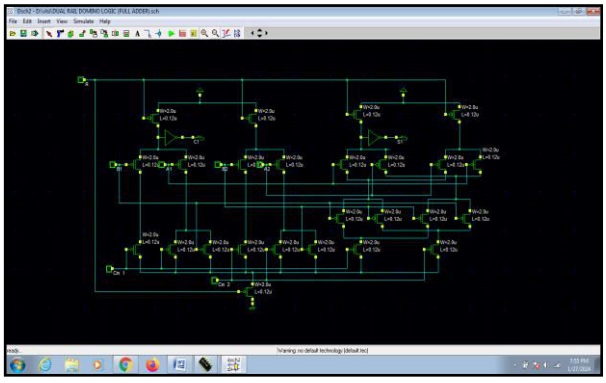

Fig: Domino logic full adder

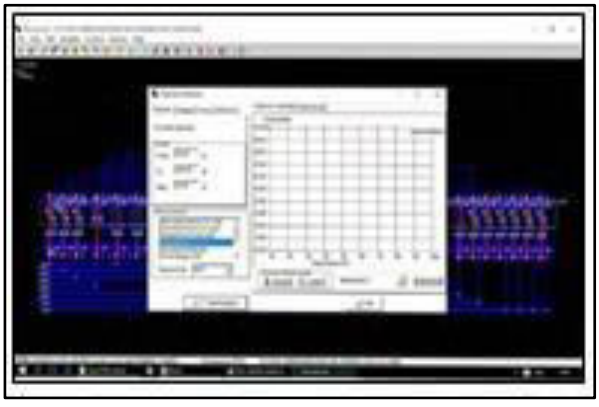

Fig: domino logic power and delay

IV. CONCLUTION

The project raises important issues that are taken into consideration while choosing appropriate power and delay reduction strategies. For a variety of technologies, including complementary metal oxide semiconductor (CMOS), transmission gate logic (TGL), pass transistor logic (PTL), domino logic, dual rail domino logic (DRDL), and double pass transistor logic (DPL) techniques, the MICROWIND tool is used to design and simulate the circuits at the layout level.

Just 16 transistors are used in double pass transistor logic, which is managed by the circuit's output. In comparison to other reduction strategies, it achieves a reduction in power and delay. It also has the benefit of not influencing the dynamic power and use of restricted area requirements because it doesn't require any additional or monitor circuitry.

| e-ISSN: 2320-9801, p-ISSN: 2320-9798| www.ijircce.com | |Impact Factor: 8.379 | A Monthly Peer Reviewed & Referred Journal |

|| Volume 12, Issue 1, January 2024 ||

| DOI: 10.15680/IJIRCCE.2024.1201067 |

REFERENCES

[1]. M Alioto, G Palumbo, "Analysis and comparison of the full adder block", IEEE Transaction on Very large scale integration, 10(6), 806-823, (2002).

[2]. Amol Kashinath Boke,Priyank Dabhade,"Analyse low power Wallace multiplier using GDI",IOSR Journal of Electronics and Communication Engineering(IOSR-JECE).Volume 12,Issne 2,ver.III,PP49-54,MarchApril 2017.

[3]. Arkadiy Morgenshtein, A Fish, Israel A Wagner, Gate- diffusion input (GDI): a power-efficient method for digital combinatorial circuits", IEEE Transactions on Very large scale integration Systems, 566-581, (2002).

[4]. M A Bayoumi, T K Dawlish , A M Shams" Performance analysis of low-power 1bit CMOS full adder cells", IEEE Transactions on VLSI System 10(1), 20 29, (2002).

[5]. A Bellaouar, M I Elmasry ,S Issam, A Khater, "Circuit techniques for CMOS low power high performance multipliers", IEEE Journal of Solid- stateCircuits, 31, 1535-1544, (1996).

[6]. Bui.H T,A1-Sheraidah, Y Wang, "New four-transistor XOR and XNOR designs", Published in Proceedings of the 2nd IEEE Asia Pacific Conference ASIC's pp. 25-28, (2000)

[7]. Reto Zimmermann and Wolfgang Fichtner ,Fellow "Low power synthesis and Cell-based design by using CMOS and path transistors",IEEE Journal of SOLID-STATE Circuits,VOL-32,NOT, July 1997.

[8]. S C. Fang, W S. Feng, J M. Wang," New efficient designs for XOR and XNOR functions on the transistor level", IEEE , of Solid-state Circuits 29 (7), 780-786, (1994).

[9]. A M Shams,M A Bayoumi, T K Darwish "Performance analysis of low-power 1-bit CMOS full adder cells", IEEE Transactions on VLSI System 10(1), 20-29, (2002).

INNO SPACE
SJIF Scientific Journal Impact Factor

Impact Factor: 8.379

doi cross ref

ISSN INTERNATIONAL STANDARD SERIAL NUMBER INDIA

निस्केयर NISCAIR

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN COMPUTER & COMMUNICATION ENGINEERING

9940 572 462 6381 907 438 ijircce@gmail.com

www.ijircce.com

Scan to save the contact details