ISSN(Online): 2320-9801
ISSN (Print) : 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 2, February 2016

Design and Implementation of Reversible Arithmetic Logic Unit

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ABSTRACT: Everyday new technology which is faster, smaller and more complex than its predecessor is being developed. The increase in clock frequency to achieve greater speed and increase in number of transistors packed onto a chip to achieve complexity of a conventional system results in increased power consumption. Reversible logic is gaining interest in the recent past due to its less heat dissipating characteristics. It has been proved that any Boolean function can be implemented using reversible gates. Reversible logic has shown potential to have extensive applications in future emerging technologies such as quantum computing, optical computing, quantum dot cellular automata as well as ultra low power VLSI circuits, DNA computing to produce zero power dissipation under ideal conditions. This paper proposes a reversible design of a 16 bit ALU. This ALU consists of eight operations, three or four arithmetic and four or five logical operations. The arithmetic operations include addition, subtraction, multiplication, division and the logical operations include NAND, AND, OR, NOT and XOR. The power and delay analysis of the various sub modules is performed and a comparison with the traditional circuits.

KEYWORDS: Reversible Logic Gates, Reversible Arithmetic Unit, Reversible Logic Unit, Reversible ALU.

I. INTRODUCTION

Reversible logic has received great attention in the recent year due to their ability to reduce the power dissipation which is the main requirement in low power VLSI design. The complexity of VLSI circuits increases with each year due to packing more and more logic elements into smaller volumes. Hence power dissipation has become the main area of concern in VLSI design. According to this, traditional irreversible circuits generate heat due to the loss of information during computation. In order to avoid this information loss the conventional circuits are modelled using reversible logic. In 1961 Landauer showed that the circuits designed using irreversible element dissipation heat due to the loss of information bits. It is proved that the loss of one bit of information results in dissipation of KT*log2 joules of heat energy where K is the Boltzmann constant and T is the temperature at which the operation is performed. In 1973 Benett showed that this heat dissipation due to information loss can be avoided if the circuit is designed using reversible logic gates.

In this paper we design a 16 bit reversible ALU that performs eight operations simultaneously. The eight operation include arithmetic and logical operation are addition, subtraction, multiplication, AND, OR, NOT and XOR. All the modules are simulated and synthesised using Xilinx ISE 14.7.

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II. REVERSIBLE GATE

A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. Also in the synthesis of reversible circuits direct fan-out is not allowed as one- to- many concepts is not reversible. However fan-out in reversible circuit is achieved using additional gates. A reversible circuit should be designed using minimum number of reversible logic gates. From the point of view of reversible circuit design, there are many parameters for determining the complexity and performance of circuits.

DEFINITION:

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Reversible Logic: If there is one to one correspondence between inputs and outputs in function 'K' (K has "n" inputs and "n" outputs), 'K' is reversible. Thus the inputs vector is uniquely, determinable from outputs vector.

Garbage Output: If the output of a gate is used nowhere of a circuit, this output called garbage output.

Constant Inputs: For make an m×n function 'K' reversible, some inputs are added to it. These inputs called constant inputs. In reversible circuits constant inputs refer to inputs that is permanently '1' or '0'.

Quantum Cost: Number of 1×1 or 2×2 reversible logic gates, needed to make the reversible gate because the quantum gates larger than 2×2 are not directly realizable in the quantum technology.

BASIC REVERSIBLE GATE:

NOT Gate:

This is the only gate among the conventional logic gates. This is a 1×1 gate with quantum cost of zero.

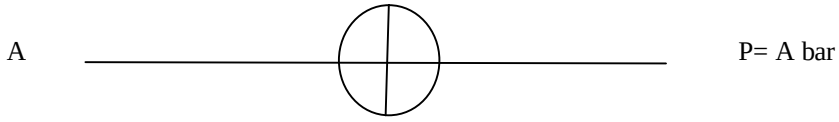

Figure. NOT gate

FEYNMAN Gate:

This is a 2×2 gate having mapping (A, B) to (P=A, Q=AB) where A, B are inputs and P, Q are outputs respectively. Since it is 2×2 gates it has a quantum cost of one.

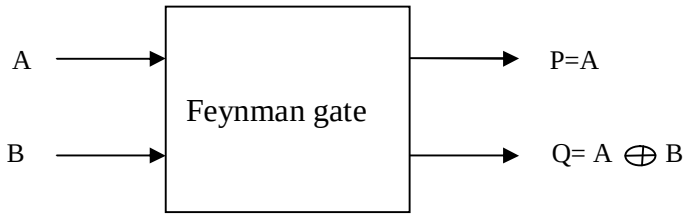

Figure. Feynman or CNOT gate

FREDKIN Gate:

Fredkin gate is a 3×3 conservative reversible gate. It maps (A, B, C) to (P=A, Q=A'B+AC, R=AB+A'C), where A, B, C are the inputs and P, Q, R are the outputs, respectively. Fredkin gate can be implemented with a quantum cost of 5 and it requires 2 dotted rectangles, 1 V gate and 2 CNOT gates.

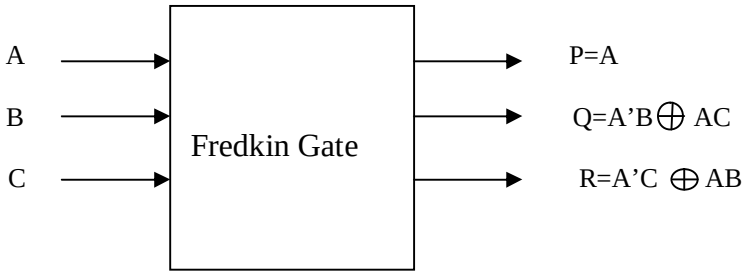

Figure. Fredkin gate

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III. INTRODUCTION TO REVERSIBLE GATE DESIGN

Reversible gate can generate unique output vector from each input vector, and vice versa, i.e., there is a one to one correspondence between the input and output vectors. Thus, the number of outputs in a reversible gate or circuit has the same as the number of inputs, and commonly used traditional NO gate is the only reversible gate. Each Reversible gate has a cost associated with it called Quantum cost. The Quantum cost of a Reversible gate is the number of 2*2 Reversible gates or Quantum logic gates required in designing. One of the most important features of a Reversible gate is its garbage output i.e., every input of the gate, which is not used as input to other gate or as a primary output is called garbage output.

IV. REVERSIBLE ALU DESIGN

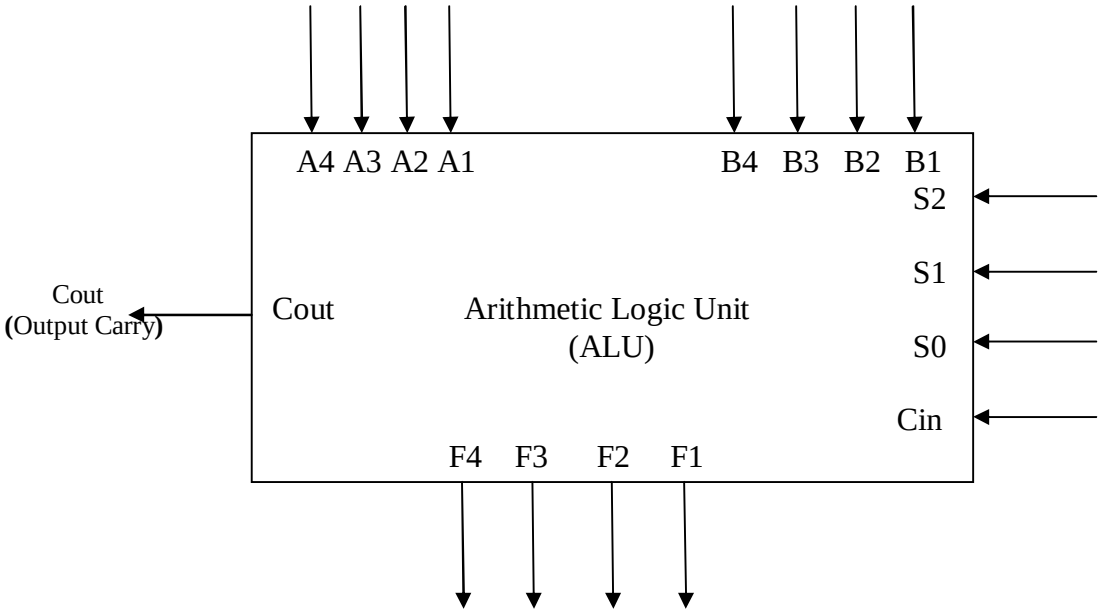

Figure. Arithmetic Logic Unit

The figure shows the basic design of an ALU. For implementing a reversible ALU each of basic components is implemented using reversible logic. The various sub modules in the design are adder, subtractor, multiplier and a logical unit. All the operations are performed simultaneously. On the basis of control signal, the required result is provided at the output.

16 Bit Adder/Subtractor Design:

The binary full adder/subtractor handles each input along with a carry in/ borrow in that is generated as carry out/ borrow out from the addition of previous lower order bits. If two n bit binary numbers are to be added or subtracted then n binary full adder/ subtractors should be cascaded. A parallel adder/ subtractor is the interconnection of a number of full adder/ subtractor and applying the inputs simultaneously. In this a 4 bit parallel adder/ subtractor circuit is designed using a 5×5 reversible JRC gate. Figure drawn below shows reversible JRC gate. This gate can acts as an adder or subtractor depending on its control input “sel”. When “sel” is zero the gate behaves as a full adder and when “sel” is one the gate behaves as a subtractor.

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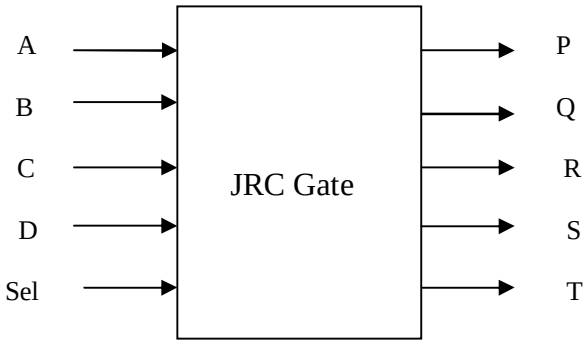

Figure. JRC gate

For implementing a 4-bit reversible adder/subtractor, 4 JRC gates are required. Hence the total gate count for a 4 bit adder/subtractor is 4 and that for a 16 bit adder/subtractor is 16. Here the carry in (carryborrow) is propagated from one gate to another gate. The module is designed using VHDL, simulated and synthesized using Xilinx 14.7

V. SIMULATION RESULTS

All the blocks are modelled using VHDL. The RTL logic used to design the modules and schematic is used to show the output in Xilinx ISE 14.7

VI. CONCLUSION AND FUTURE WORK

The 16 bit Reversible ALU is designed by integrating various sub modules that includes Adder, Subtractor, Multiplier and Logical Unit. The Logical Unit performs AND, OR, NOT, XOR, NAND. The performance evaluation of the various sub modules are carried out using synopsis tools and it was found that the circuits designed using reversible logic showed a reduced delay and power. As a future work a reversible divider can be designed and included into this ALU.

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