ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 4, April 2016

Review on Alternatives for Conventional Transistor Technology

Neelam Bedwal[1], Renu Mehla[2], Archna Aggarwal[3], Bal Krishan[4]

M.Tech Student, Dept. of E.C.E., YMCAUST, Faridabad, Haryana, India[1,2]

Associate Professor, Dept. of E.C.E., YMCAUST, Faridabad, Haryana, India[3]

Assistant Professor, Dept. of E.C.E., YMCAUST, Faridabad, Haryana, India[4]

ABSTRACT: The physical features of bulk MOSFETs is aggressively scaled down and these typical MOSFETs devices will shortly be experiencing slight advancement due to the scaling down. In order to achieve performance improvements,new alternative architectures are demanded. As the scaling of MOSFET into sub-50nm regime, SOI and DG-MOSFET are anticipated to replace conventional bulk MOSFET. These recent MOSFET devices will prove as strong competitors for RF applications in wireless substrate is proving itself as a bright candidate for sub-40nm technology nodes. DG-MOSFET devices gives better control of threshold voltage(Vt) by employing electrostatic coupling from the two gates on each side of the channel.The latest developments are largely based on noble materials and new structures that comprise strained Si, high-K/metal gate, multiple gates, SOI technology. In the proposed paper all the above mentioned technologies will be discussed which will definitely bring change to the present CMOS technology.

KEYWORDS: SOI,Highk,DG MOS.

I. INTRODUCTION

From the last 30 years, the MOSFET have frequently been scaled down in size in channel length from micrometers to submicrometers and then from sub micrometers range to nanometer range following the Moore's Law. These nanoscale devices have a remarkable prospective to revolutionize and to certainly uprise the fabrication,integration of electronic systems and scale beyond the discerned scaling restarints of fundamental CMOS [1]. From the last four decades, the cost-per-function and the implementation of integrated circuits(IC) have been enhanced greatly by rigorous scaling of planar bulk Si CMOS devices. Although, the capacitive control of the channel potential by the gate becomes more strenuous [2],as the gate length (Lg) reduces.Alternatively, the source and drain effects remarkably the channel potential, emerging in serious short channel effects (SCE), like increased off-state leakage current (IOFF), threshold voltage (VT) roll-off, i.e., smaller VT at shorter gate length (Lg), and drain-induced barrier lowering (DIBL), which means smaller VT at larger drain voltage (Vd) because of modulation of source-channel potential barrier by drainvoltage.To lower some issues associated with scaling down of cmos ,some noble CMOS proposals and approaches such as stained Si, SOI technology, multigate transistors and high-K/metal gate have been studied carefully. From long term viewpoint, almost around 5nm technology all the advanced CMOS approaches will start showing somw physical limitations [2]. In that case, conventional microelectronics technology will be switched to nanotechnology where carbon nanotube field effect transistors (CNTFETs) are approached to provide higher transistor performance with increasing energy efficiency.

II. ALTERNATIVE CMOS APPROACHES

Several advanced techniques are discussed here to reduce the drawbacks of CMOS scaling:

A. *SOI:*

Silicon on insulator (SOI) technology is exceptionally captivating in the terms of performance (low power consumption ,high speed, radiation-hard) and improved scalability. In comparison to conventional silicon, the desgin of SOI MOSFETs is much flexible because a larger number of parameters—like substrate doping, buried oxide thicknesses of film and back gate bias—may be utilized for the optimization as well as scaling.It is widely known that

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 4, April 2016

the short-channel effects are dramatically decreased in SOI films.Thedesgin of SOI devices is almost similar to the bulk CMOS. An insulation layer is inserted directly below(underneath) the device on the silicon substrate. In contrast to a bulk CMOS ,this insulation layer presents lower coupling capacitance from the conducting channel to the substrate, while the fabrication process employed is similar to the bulk CMOS process. The advantages of an SOI MOSFET are also comprised of higher current drive which results in smaller delays, as doping free channels have a little greater mobility. [3] A buried oxide insulation layer reduces leakage current from the drain/source junction to substrate to maximize the network life by minimizing the total transmission energy using energy efficient routes to transmit the packet.

Generally SOI MOSFETs are of two types:

- Partially depleted SOI MOSFET
- Fully depleted SOI MOSFETs

They both have their unique features in terms of process, performance and applications.

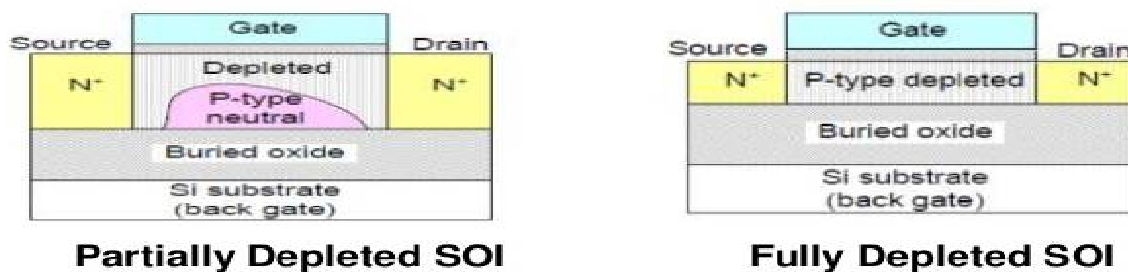

Fig.1. Partially Depleted SOI and Fully Depleted SOI

A fully depleted SOI MOSFET has a narrow top silicon layer,therefore the channel is entirely depleted of the majority carriers under strong inversion. Consequently, the SOI layer is considerably smaller in dimension as compared to the depletion width of the device.Also, its potential is firmly controlled by the gate. As a result,there remains no neutral region of the body of the MOSFET which can be charged. The benefits of the FD SOI MOSFET involves the removal of the floating-body effect and improved short channel behavior.For Partially Depleted SOI device, the thickness of the SOI layer is more in comparison to the maximum depletion width of the gate. Generally the silicon film thickness is higher than 50nm, which attenuates the limitation on device threshold voltage and its sensitivity, Also by using PD SOI devices manufacturing becomes easier and the process and device design are more suited than with the bulk CMOS. But the major issue related with the partially depleted device is its floating body effect.The thicker top silicon layer of the partially depleted SOI MOSFETs gives ample room for the depletion layer.So that it does not extend to the buried oxide layer as shown in Figure 1 above.

B. *Multigate technology:*

Multigate transistors are more favourable choice for upgrading the performance and scaling characteristics of device. The short channel effects such as DIBL, threshold voltage roll off can be alleviated and a perfect control over channel current can be maintained. DG-MOSFET with aligned planar gate structure contributes to improved and enhanced channel control but the challenging part is its fabrication process. Further FinFET and Trigate FETs have come out to be superior in terms of their ease of fabrication. FinFET can be desgined on both bulk as well as SOI.

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 4, April 2016

a) *Double Gate:*

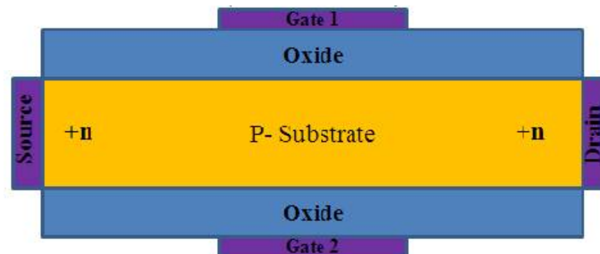

Fig.2. Double Gate MOSFET

For utmost scaled CMOS technology generations, the double-gate (DG) transistor is referred as one of the most propitious devices[2]. Surely, due to a good electrostatic control of the channel by both the gates, it is surmised to give lower short channel effects (SCE), near ideal sub-threshold slopes and larger drive currents in comparison to single-gate (SG) transistors.The notion of a Double-gate MOSFET is that it controls the channel effectively from gates on each side of the channel as that of one gate in planar bulk MOSFETs. Controlling the channel by multiple (i.e. double, triple, surround, etc.)gates has its proficiency of improved control on the channel inversion, thus the short channel effects are minimized. More precisely, minimizing the current leakage and nullifying the drain-induced barrier lowering (DIBL) effect are examples of supremacy in double-gate MOSFETs over bulk mosfet [4, 5] The desgin of a DG-MOSFET based on the silicon on insulator(SOI) technology is shown in Figure 2, where the two aligned gates are utilized to modulate electric fields and better controls channel charges from both the side. For the better control of electrostatic coupling, two gates are used so that the quantity of current flow in the channel is properly enhanced by the electric field.

Types of DG-MOSFET

Depending upon the voltages applied to the gate terminal, DG-MOSFETs may be classified as following [7]

i. *Symmetric DG-MOSFET:*

A DG-MOSFET is named to be symmetric when the applied workfunction of both the gates are same i.e. the material used for both the front and back gate are similar and hence if N+ poly-Si is used as the material of front gate then back gate will also have the same material type and same metal or doping is used for both front and back gate electrode. This permits both gates to effect the operation of the device in a similarmanner. InSDG same voltages are applied at both the gates and also it is structurally symmetrical at both the top and back gate with identical oxide thickness [8]. Here, each gate is completely independent of the another and can control half of the device and its operation.

ii. *Asymmetric DG-MOSFET:*

An asymmetric DG-MOSFET has synchronized but dissimilar input voltages are applied to both of the identical gates, or if the same input voltage is applied to both gates their work functions should be different [7]. The name of "symmetric" and "asymmetric" basically describes presence or absence of symmetry and uniformity of the electric field in the channel of the DG-MOSFET [7].

b) *FinFET:*

FinFETs are basically the variation of the fundamental DG configuration. This new structure elucidates a number of scalability problems and also signifies suppressed short channel effects(SCEs) compared to the basic MOSFET. FinFETs are beneficial in terms of their easy fabrication process and low source/drain resistance over usual double gate devices. A highly doped poly-Si film forms the electrical connection with the device which folds around the fin and the body of the MOSFET is served by the thin gently doped Si in FinFET [9]-[10]

In addition, this superior device is well matched with the planar CMOS fabrication platform and therefore regarded economical. FinFET is also suitable for scaling and it is one of the most hopeful self-aligned structures that have been recommended so far. It have a thin Si fin with gate running all over the fin in a self-aligned way. Figure shows the FinFETstructure .

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 4, April 2016

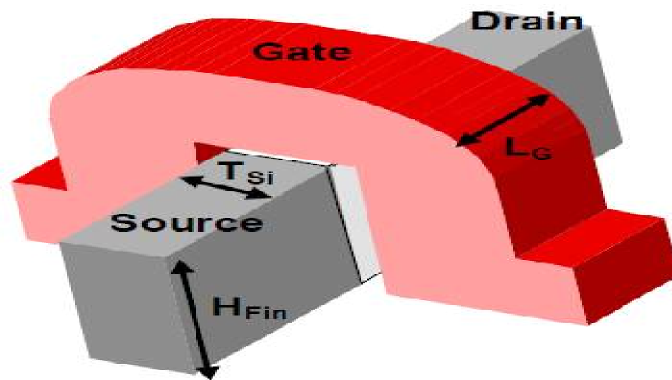

Fig.3. FINFET

c) *High k-Dielectric:*

SiO2 has been used as an effective gate dielectric since the emergence of MOS devices over past 40 years. The necessity for enhanced speed at continual power density has led to shortening of MOSFET dimensions and the oxide thickness is also minimized in step as per scaling rules.With scaling approaching sub nanometer technology nodes, the introduction of novel materials became inescapable as scaling of SiO2 increases a significant perturb in terms of tunneling current and oxide breakdown [12].In order to avert direct gate tunneling in very thin gate oxides, the SiO2 is substituted by novel materials with greater permittivity and larger physical thickness. However, the establishment of these high-k dielectrics posses various issues, such as bi-dimensional electrostatic effects which may have a considerable effect on the device performances when the gate dielectric thickness becomes equivalent to the device gate length.

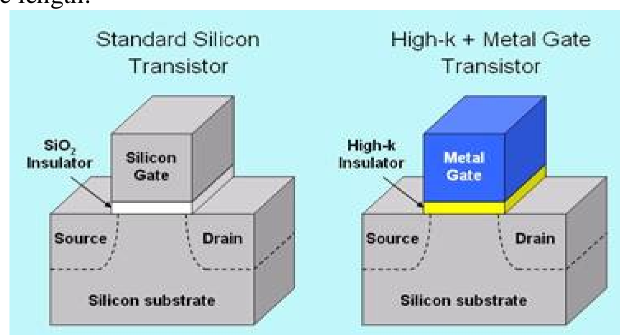

Fig.4.View of Standard Transistor and High-k Metal Gate Transistor

Using an insulator with higher dielectric constant is one of the solutions to continue scaling in nanometer regime with suppressing the SCEs. The alternative insulator should have the following properties [11] : (i) chemical and electrical stability on silicon, (ii) uniform oxide thickness during fabrication, (iii) high breakdown voltage, (iv) thermal stability up to 1000○C, (v) pinhole free and negligible defects, (vi) low charge trapping and ionic impurities, (vii) high life time under normal operating conditions, (viii) low interface state density for high carrier mobility, (ix) small gate-leakage current (x) low hot-carrier degradation, (xi) low diffusivity of boron and phosphorous at typical processing conditions. Some of these properties depend on the material as well as on the processing technology. At first Campbell et al. introduced TiO2 as the potential high-k gate dielectric [2]. Later various research groups work on the feasibility of other alternative high-k dielectric (e.g. Al2O3, ZrO2, Ta2O5, HfO2, ZrSixOy, Y2O3, Ya2O3) for submicron MOSFET. The various dielectric materials are shown with their properties in table1. All these high-k materials have some practical limitations [11].

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 4, April 2016

Gate dielectric material	Dielectric constant (k)	Energy band gap Eg (Ev)	Conduction band offset ΔEc (Ev)	Valence band offset ΔEc (Ev)
SiO_2	3.9	9	3.5	4.4
Al_2O_3	8	8.8	3	4.7
TiO_2	80	3.5	1.1	1.3
ZrO_2	25	5.8	1.4	3.3
HfO_2	25	5.8	1.4	3.3
Ta_2O_5	25	6	1.5	3.4
Y_2O_3	13	6	2.3	2.6
Ya_2O_3	27	4.3	2.3	0.9

Table . 1. High-k dielectric materials and their properties

III. CONCLUSION

In this paper, review on various advanced CMOS techniques and nanotechnology based concepts have been done. To extend the roadmap for few decades several advanced CMOS techniques such as strained Si, high K/metal gate, SOI and multi gate transistors have been introduced to reduce the scaling limits. But semiconductor industry has faced various challenges after the employment of new materials. Consequently, new scaled device structures will not allow conventional approach for further use. To overcome these challenges, there has been a paradigm shift from microelectronics to nanotechnology on a time scale of decades.

REFERENCES

1. AThomas Ernst, SorinCristoloveanu, Gérard Ghibaudo,ThierryOuisse, Seiji Horiguchi, Yukinori Ono, Yasuo Takahashi, and Katsumi Murase " Ultimately Thin Double-Gate SOI MOSFETs", IEEE Trans. on Electron Devices, Vol. 50, No. 3, March 2003.
2. J. Bansal, N. Sharma, S. P. Kumar, R.Chaujar, M.Gupta and R. S. Gupta, "Two-Dimensional Analytical Sub-Threshold Model of Double Gate MOSFET with Gate Stack",Proceedings of International Conference on Microwave, 08.
3. Pin Su, Samuel K. H. Fung*, Stephen Tang, FariborzAssaderaghi and Chenming Hu, "Partial-Depletion SO1 MOSFET Model for Deep-Submicron CMOS Designs",IEEE Custom Integrated Circuits Conference, 2000.
4. Julie Widiez, JérômeLolivier, Maud Vinet, Thierry Poiroux, Bernard Previtali, FrédéricDaugé, MireilleMouis,"Experimental Evaluation of Gate Architecture Influence on DG SOI MOSFETs Performance'' , IEEE Trans. on Electron Devices, Vol. 52, No. 8, Aug. 2005.
5. Sedra Smith, "Microelectronic Circuits", 2008.
6. SyafeezaBinti Ahmad Radzi, Electronics and Telecommunication "Simulation of 0.18 micron mosfet and its characterization", M.Tech. Thesis under faculty of Electrical Engineering University Technology Malaysia, pp- 47, 55, 71-76, October 2005.
7. Vinay K. Yadav and AshwaniK.Rana, "Impact of channel-doping on DGMOSFET parameters in Nano Regime-TCAD simulation", International Journal of Computer Applications, Vol 37, No. 11, pp.36-40, January 2012.
8. L.Chang, S.Tang, T.-J.King, J.Bokor, and C.Hu, "Gate length scaling and threshold voltage control of double-gate MOSFETs," IEEE International ElectronDevices Meeting, pp. 719-22, 2000.
9. S. Jooyoung, Y. Bo, Y. Yu, and T. Yuan, "A Review on Compact Modelling of Multiple Gate MOSFETs," Circuits and Systems I: Regular Papers, IEEE Transactions on Electron Devices, vol. 56, pp. 1858-1869, 2009.
10. W. Xingsheng, A. R. Brown, C. Binjie, and A. Asenov, "Statistical variability and reliability in nanoscaleFinFETs," in Electron Devices Meeting (IEDM), IEEE International, 2011, pp. 5.4.1-5.4.4. International Journal of Scientific & Engineering Research, Volume 6, Issue 2, February-2015 ISSN 2229-551819
11. M. H. Chowdhury, M. A. Mannan and S. A. Mahmood, "High-k Dielectrics for Submicron MOSFET", IJETSE International Journal of Emerging Technologies in Sciences and Engineering, Vol-2, No.2, pp-8-10, July 2010.
12. Vinay K. Yadav and AshwaniK.Rana, "Impact of channeldoping on DGMOSFET parameters in Nano Regime-TCAD simulation", International Journal of Computer Applications, Vol 37, No. 11, pp.36-40, January 2012.

BIOGRAPHY

Neelam Bedwal is a M.Tech Student(C&I) in Electronics Engineering Department, YMCA university of science & Technology, Faridabad.Her research interests are Control Electronics Engineering and MOSFET.

Renu Mehla is a M.TechStudent(VLSI Design) in Electronics Engineering Department, YMCA university of science & Technology, Faridabad.Her research interests are VLSI Desgin,Electronics Engineering.

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 4, April 2016

ArchnaAggarwal, She is an associate professor in electronics engg. Deptt. At YMCA University of science &technology, Faridabad . Her various research interests include artificial neural networks, fuzzy logic, renewable energy & control systems.

BalKrishan,Assistant Professor,Electronics Engineering Department,YMCA University of Science and Technology,Faridabad,Haryana-121006,India; B.E.(Electronics and Communication Engineering), M.Tech, (Nanotechnology), Ph.D. (pursuing).He has published 28 numbers of papers in various International & National Journals &conferences.His research area:Nanoelectronics&Devices,VLSIDesign,Electronics Engineering.