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Design of High Speed DDR3 SDRAM Controller

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ABSTRACT: As system bandwidth has expanded, memory technologies have become more popular for high-speed operation and performance.The third generation of DDR memories, DDR3 SDRAM, is distinguished by high density, high memory bandwidth, and low device cost. However, because of high-speed interface technology and complex instruction-based memory, a special-purpose memory controller is required to optimize burst access and increase data throughput. This research presents a dedicated DDR3 controller for high performance table lookup, as well as a corresponding lookup circuit based on the Hash Cam approach.Key words: DDR3, SDRAM, VHDL, HASH CAM

I. INTRODUCTION

DDR3 SDRAM, a 64-bit synchronous dynamic random access memory, has a higher bandwidth and can carry data at up to 64 times the memory clock speed in MB/s. It is capable of supporting chip capacities of up to 8 gigabits. Content Addressable Memory (CAM)-based algorithms are extensively employed in network equipment for rapid table lookups. To replace pure CAM-based lookup circuits, a HASH-CAM circuit with equivalent performance, higher memory density, and lower cost has been proposed. For lookup workloads with brief and random memory access patterns, efficient DDR bandwidth use is a considerable difficulty. This paper presents the design of a high-speed DDR3 SDRAM controller using Xilinx FPGA technology.

In fact, DDR3 SDRAM is a kind of third incarnation of DDR SDRAM principles. As a result, we have every right to compare DDR3 and DDR2 SDRAM here. Furthermore, this comparison will not take long.

DDR3 SDRAM is the third generation of memory, with improved performance and decreased power consumption. In comparison to previous generations of DDR1/2 SDRAM, DDR3 SDRAM is a higher density device with higher bandwidth due to an increase in clock rate and a reduction in power consumption due to 1.5V power supply at 90 nm fabrication technique. DDR3 memory is more versatile to access with fewer bank conflicts because it has 8 distinct banks.

II. DESIGN SYSTEM

DDR memory allows data to be retrieved on both the rising and falling edges of a clock cycle, thus doubling data rate. Timing for DDR1 is determined by a sequence of numbers such as 2-3-2-6-T1,3-4-4-8, or 2-2-2-5. Lower values indicate speedier operations, whereas higher values imply the amount of clock pulses necessary for certain tasks. One of the operations indicated by these figures is CL (Column Address Strobe) latency, which is the time it takes for memory to provide data after being requested by the processor. tRCD (ROW Address Strobe to CAS Delay) represents the time between activating the row and column where data is saved. tRP (RAS Precharge) is the time between blocking access to one row and commencing access to another. Before commencing the next access, the memory must wait for tRAS (Active to Precharge Delay). CMD (Command Rate) is the amount of time that passes between the activation of a memory chip and the first command issued. The burst write/read mode and multi-bank design of SDRAMs enable concurrent operations on many banks, allowing for high memory bandwidth by scheduling access to each.

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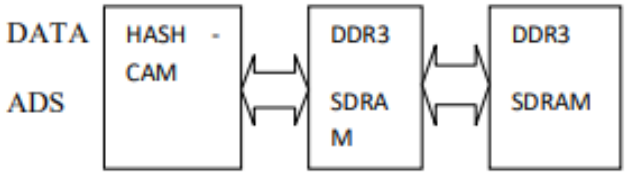

Figure 1 Data ADS

SDRAMs are frequently employed to boost system performance by concentrating on bank control and data access sequences. A new memory-interface design is presented to improve memory bandwidth and power usage in video applications. To reduce the number of overhead cycles required for row activations in synchronous DRAM (SDRAM), this architecture employs an address-translation approach. The present architecture of video processing units in consumer systems is often based on different forms of processor hardware, such as MPEG encoders and decoders and high-end television systems.

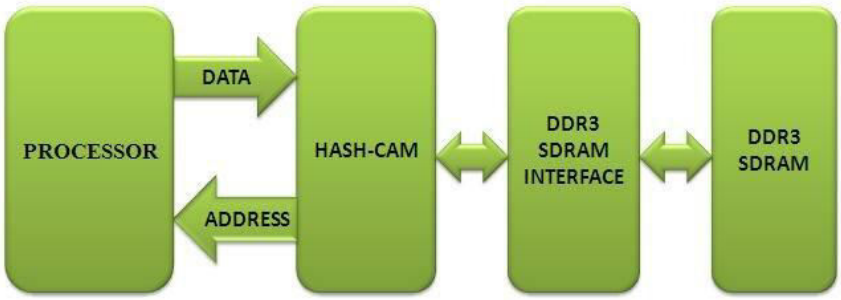

Figure.2 HASH -CAM

DDR3 SDRAM devices are the DDR SDRAM family's next generation, with 1.5V signaling for high-speed operation. They are more versatile and employ a differential clock given by the controller, resulting in fewer bank conflicts. When the address value is sent from the DDR3 SDRAM interface, the proposed Hash-CAM based lookup circuit saves original data and reference address information, which is translated by the Hash-CAM circuit.

Along with the data, a bidirectional data strobe (DQS) is transmitted for data capture at the receiver. The DDR3 SDRAM device and controller test memory device and memory interface write and read accesses. When it is center aligned with data for writes and edge aligned data for reads, the DQS is strobe delivered by the DDR3 SDRAM device during reads and by the controller while writing DQS.

DDR3 SDRAM has a double data rate architecture to achieve high-speed operation. The 8n-prefetch architecture with the double data rate interface is intended to carry two data bits at the I/O pins each clock cycle. A single read or write access to DDR3 SDRAM consists of a single 8n-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight matching n-bit-wide, one-half-clockcycle data transfers at the I/O pins. Externally delivered with the data is the differential data strobe (DQS, DQS#) for use in data capture at the DDR3 SDRAM input receiver.

DQS is focussed on the data for WRITEs. DDR3 SDRAM transfers read data that is edge-aligned to the data strobes.

III. RESULT AND DISCUSSION

This paper describes a DDR3 SDRAM controller with 64-bit data transfer that can synchronize data flow between DDR RAM and external peripheral devices. Because to 90nm fabrication technology, the controller's off-chip power dissipation is 39mW, and a doubled prefetch buffer to 8 bits enhances performance. The experimental results back up

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the suggested architecture's predicted performance, demonstrating that DDR3 peak memory bandwidth can be attained for a given random lookup.

IV. CONCLUSION

Based on a 256K table entry prototyped DDR3 Hash-CAM circuit, this study proposes an improved DDR3 memory controller architecture for high performance table lookup. When compared to other types of SDRAM, the DDR3 SDRAM controller offers benefits such as faster data transfer, lower manufacturing costs, and synchronization, making it a successful design using XILING 13.1 HDL.

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