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Design of Efficient Non-volatile SRAM cell for Instant On-Off Operation

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ABSTRACT: In modern technological world of nanoscale CMOS IC energy is consumed more and is getting serious problem. So there is need to minimize this energy consumption and for this Non-volatile Static random access memory cell (NVSRAM) have been proposed. In this paper, we deals with the design and analysis of high speed performance Non-volatile SRAM cell for future search engines to develop low power consumption and no loss of store data in a cell even if the power supply is turn off. Considering increasing demand for larger data storage capacity has driven the fabrication technology and memory development towards more compact design rules and, consequently, toward higher data storage densities. Also to design the CMOS layout of NVSRAM cell, we are using "microwind3.1" based on 45nm CMOS technology.

KEYWORDS: Static Random Access Memory (SRAM); Non-volatile Static Random Access Memory (NVSRAM); CMOS; 45nm technology; microwind3.1.

I. INTRODUCTION

In recent years, power dissipation has been one of the most important concerns for highly integrated advanced complementary metal-oxide-semiconductor (CMOS) logic circuits, since it constrains their performance and the degree of device integration. So there is need to minimize this power dissipation. In this paper, we look at conceptualization, propose and modelling of memory cell as a part of a Non-volatile Static Random Access Memory (NVSRAM) architecture using Static Random Access memory (SRAM) as a volatile core. A typical Non-volatile Static Random Access (NVSRAM) cell forms a SRAM cell that has two n-type and two p-type MOS transistors, which requires both VDD and GND connections as well as well-plugs within each cell. Construction of a SRAM cell with nonvolatile memory which is called as Nonvolatile SRAM can be fabricated as an extension to a CMOS process technology with nanoscaled geometry, addresses the main thread of current NVSRAM research towards reduction of power consumption. Power dissipation in CMOS logic circuits can be divided into two components, dynamic and static power However, static power dissipation gives rise to severe problems for CMOS logic circuits with very large scale integration. Recently proposed power-gating architecture based on multithreshold voltage CMOS (MTCMOS) technology is expected to be very effective at reducing static power dissipation in CMOS logic circuits. Therefore NVSRAM cells have the potential for significant saving in power dissipation.

Power has become one of the most important paradigms of design convergence for multi gigahertz communication systems such as optical data links, wireless products, microprocessor also power dissipation has been one of the most important concerns for highly integrated advanced complementary metal-oxide-semiconductor (CMOS) logic circuits, since it constrains their performance and the degree of device integration. This paper introduces design aspects for layout design of Non-volatile static RAM memory cell using VLSI technology. These cells are designed using latest 45nm CMOS technology parameters, which in turn offer high speed performance at low power. There are wide variety of categories of memories available ranging from Flash to MRAM, PROM to EEPROM, and many more.

II. RELATED WORK

From the rigorous review of related work and published literature, it is observed that many researchers have designed Non-volatile SRAM by applying different techniques. Researchers have undertaken different systems, processes or phenomena with regard to design and analyze NVSRAM and attempted to find the unknown parameters. Since in the real world today VLSI/CMOS is in very much in demand, from the careful study of reported work it is observed that very few researchers have taken a work for designing NVSRAM cell with CMOS/VLSI technology.

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Mr. Sunil Jadav, Mr. Vikrant, Dr. Munish vashisath [3] worked under Design and performance analysis of ultralow power 6t sram using adiabatic technique to reduce average power dissipiation. This adiabatic technique for reducing average power is proved to be very effective.

K dhanumjaya, M sudha, Dr MN.Giri Prasad , Dr K.Padmaraju [4] presented dynamic column based power supply Memory cell. This proposed memory cell achieved improved read stability, read current and leakage current.

Pankaj Kumar Pal, Brajesh Kumar Kaushik and Sudeb Dasgupta [2] proposed a double dielectric or dual-*k* spacers technology to enhance the electrostatic integrity of underlap FinFETs. The primary goal in SRAM cell includes maximizing stabilities and minimizing access times besides achieving minimum leakages. The SymD-*k* architecture exhibits excellent electrostatic integrity over the channel that improves device performance and SRAM design metrics.

Wei Wei, Kazuteru Namba, Jie Han and Fabrizio Lombardi[1] presented a novel NVSRAM circuit .The proposed cell offers better non-volatile performance (in terms of operations such as "Store", "Power-down" and "Restore") and achieved a significant reduction in energy for its operation required for "Instant-on" operation when compared with other NVSRAMs cells.

Considering all this constraint regarding the demand of today's fast communication world, the research has been taken to design low power NVSRAM using 45nm VLSI technology.

III. PROPOSED WORK

A. *Proposed NVSRAM cell structure:*

Fig[1] illustrates general model for Non-volatile SRAM cell and fig [2] illustrates NVSRAM cell with cross-coupled inverters. NVSRAM is a type of cell that can combine the benefit of a simple access and a nearly unlimited "Store" capability of a SRAM with a non-volatile element, such as an EEPROM (electrically erasable programmable ROM). An NVSRAM cell has three different states it can be in: standby where the circuit is idle, reading when the data has been requested and writing when updating the contents. The NVSRAM to operate in read mode and write mode should have "readability" and "write stability" respectively[4].

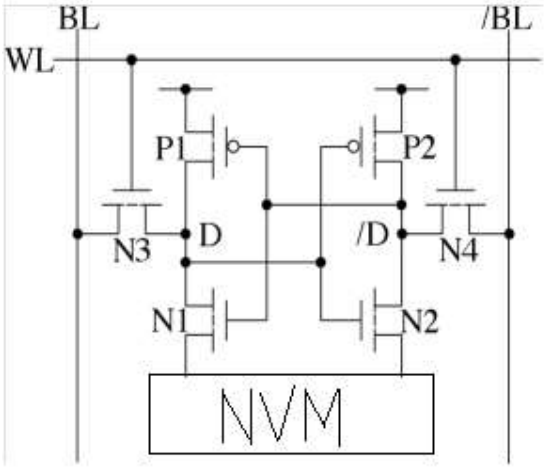

Fig. 1. General model for NVSRAM Cell

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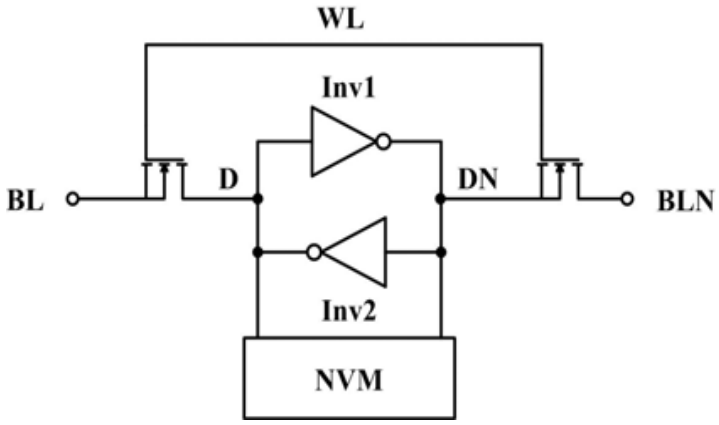

Fig. 2. NVSRAM cell with cross-coupled inverters

Fig. [3] illustrates the layout design of proposed 6T1R NVSRAM cell

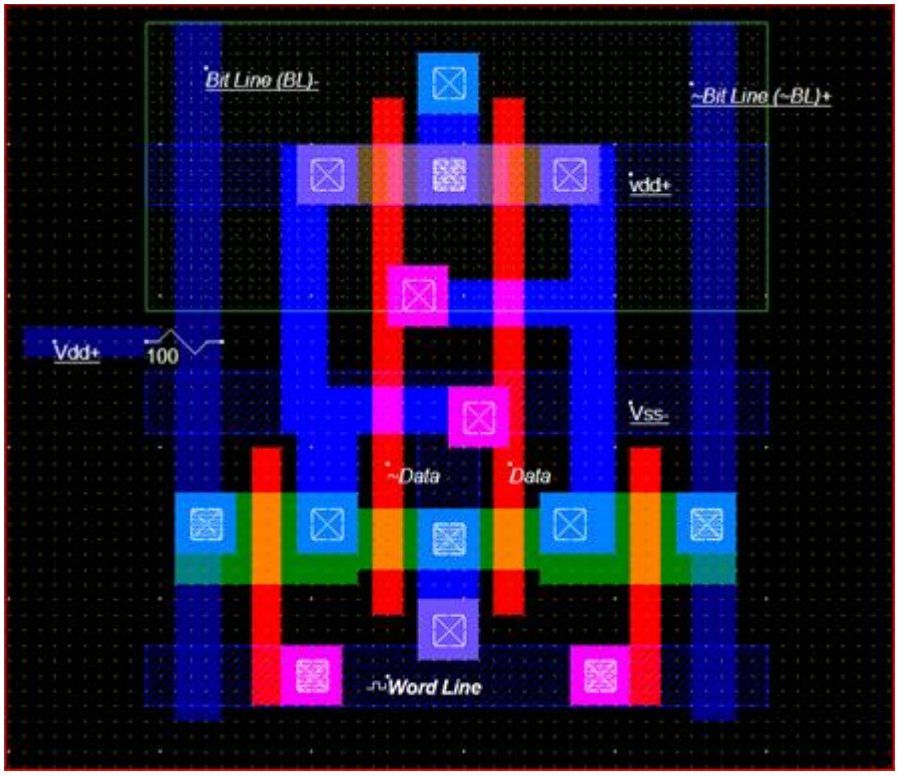

Fig. 3. Layout design of 6T1R NVSRAM cell

From this fig.[3] it is observed that 6-T NVSRAM cell is made up of 4 N-type MOS transistors and 2 P-type MOS transistors. Resistance of 100ohm is connected to the bit line. Bit line and inverted bit line are similar to the data and inverted data line in the schematic. 4-transistors in the centre form two cross-coupled inverters. Output of 1st inverter is given to the input of 2nd inverter i.e. polysilicon and vice-versa. P-type MOS transistors are enclosed by n-well so that there should not be any short circuit and to get better conductivity. Also this p-type MOS transistor acquires more silicon area as compare to n-type MOS transistor. The supply used V_{dd} is a DC supply of 0.40V.

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IV. SIMULATION RESULTS

We simulate the proposed layout of NVSRAM cell using the following design steps shown in the flow chart and obtained the results. Following are the 4 steps:

1. Schematic design of proposed NVSRAM using CMOS transistors.
2. Formal simulation and verification of the above for different parameters.
3. CMOS layout for the proposed NVSRAM using VLSI backend.
4. Verification of CMOS layout and parameter testing.

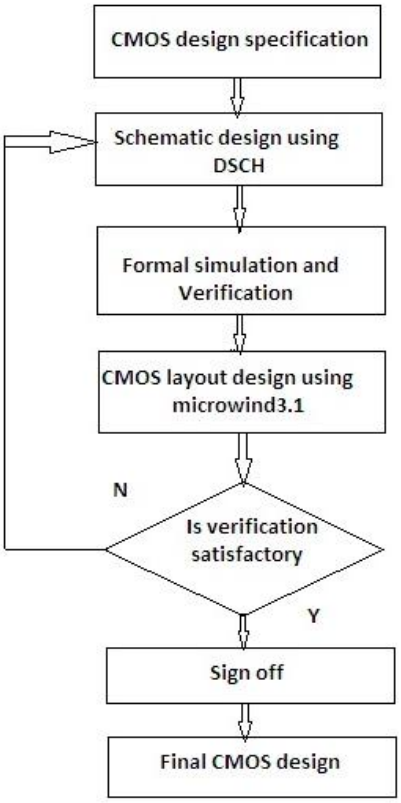

Fig. 4. Design flow chart

If the goal is achieved for all proposed parameter including detail verification, sing off for the design analysis and design will be ready for IC making. If detail verification of parameters would not complete then again follow the first step with different methodology. The operational voltage is usually from 0.2 V to 1.8 V, depending on the technology variant. In Microwind, it decided to fix VDD at 0.4 V in the cmos45nm.RUL rule file, which represents a compromise between all possible technology variations available for this 45-nm node. Effort has been taken to design Low Power, High performance Non-volatile SRAM cell (NVSRAM) cell, using VLSI technology. The design process, at various levels, is usually evolutionary in nature. It starts with a given set of requirement. When the requirements are not met, the design has to be improved. More simplified view of the VLSI technology consists of various representations, abstractions of design, logic circuits, CMOS circuits and physical layout. Here for the design using VLSI technology microwind3.1 VLSI Backend software is used. This software allows designing and simulating an integrated circuit at physical description level. The proposed work is designed using 45nm CMOS/VLSI technology in Microwind 3.1 software [14].

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Compared to 65nm technology most 45nm technologies must offers:

- 30% increase in switching performance
- 30% less power consumption
- 2 times higher density
- X 2 reduction of the leakage between source and drain and through gate oxide.

Considering the advantage of 45nm technology over 65nm technology proposed work is done with 45nm technology.

We simulate the proposed layout of NVSRAM cell and simulation waveform of it is as shown in below fig. [5]. As shown in the following figure, the start of a write cycle begins by applying the value to be written to the bit lines. If we wish to write a 0, we would apply a 0 to the bit lines, i.e. setting BL bar to 1 and BL to 0.In the following fig. bit line is kept at low value and bit line bar at high value. A '1' is written by inverting the values of the bit lines. WL is then asserted and the value that is to be stored either '0' or '1' is latched in. Also through appropriate cell or cells data is then read. Also the corresponding data and inverted data lines are shown in the following figure. The data line is at logic 0 and corresponding inverted data line is at logic 1.

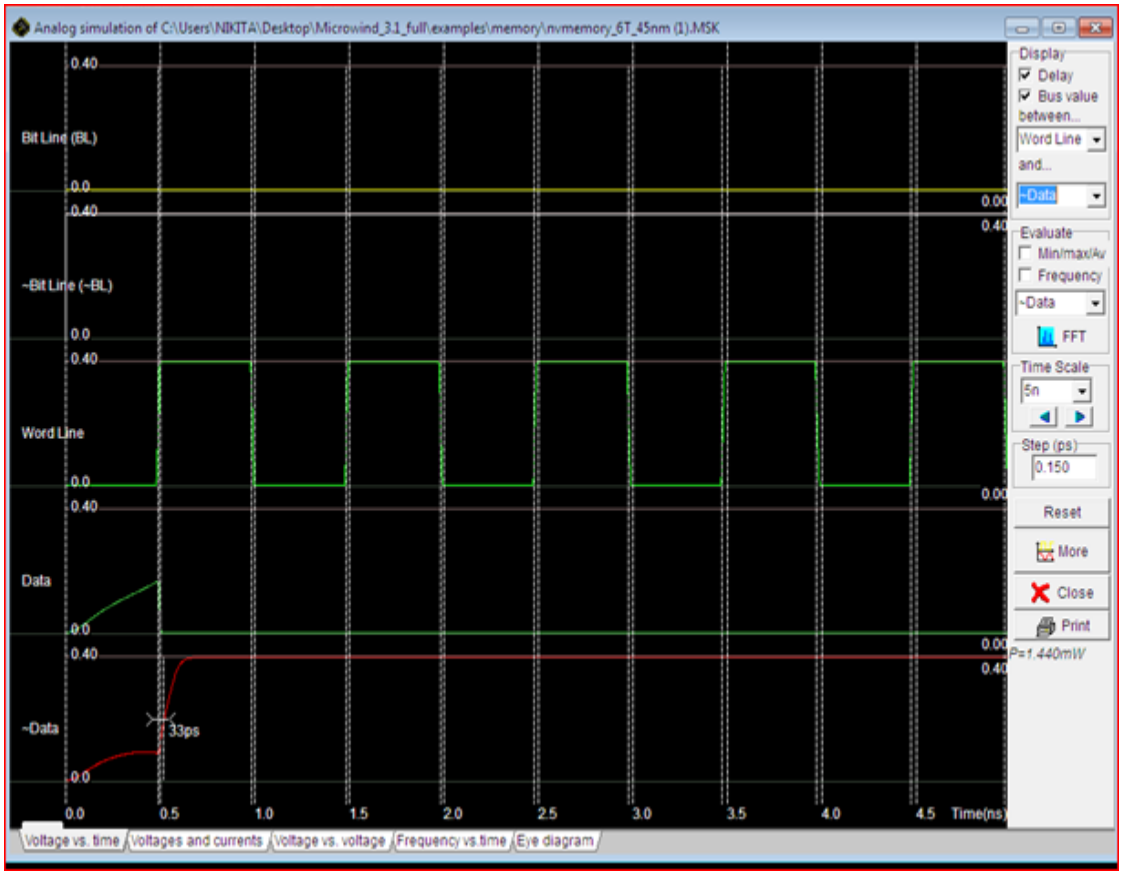

Fig. 5.Simulation waveform of 6T1R NVSRAM cell

Above fig shows the simulated waveform for 6T1R NVSRAM cell. When word line has logic 1 data of bit line get sampled means data of bit line get written on data line and when word line has logic 0 the data which previously get written on data line will now get read on data line and thus read-write cycle is continued. When word line has logic 0 at that time also data of the bit line will get read to the data line (data which was previously written on the data line) this means that even if the power supply is turned off input data is offered to the output data. Power consumed by 6T1R NVSRAM cell is 1.440mW.

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The proposed layout of NVSRAM cell is simulated and we obtained the performance parameter of it as shown in the following table. Performance parameter of NVSRAM cell is obtained based on 45 nm CMOS technology. The parameter like Area is measured in micrometer, Static power for logic '0' and average power is measured in milliwatt, and static power for logic '1' is measured in microwatt. The total area required for CMOS layout of NVSRAM cell is 1.40 μm^2. Static power required for logic 0 operation is 1.440mW and for logic 1 operation is 0.017 µw. Also average power required is 0.72mW.

Table1:Performance parameter of NVSRAM cell

Parameter		CMOS technology(45nm)
Area		1.40µm^2
Power	Static 0	1.440mW
	Static 1	0.017µw
	Average power	0.72mW

V. APPLICATIONS

1. In case of external power failure NVSRAM can hold data without autostore feature.
2. Medical equipment and high end servers can use NVSRAM to store their data.
3. Networking, aerospace where preservation of data is critical and where batteries are impractical.
4. Analog computations embodied a whole area of research which, unfortunately, were not as scalable, reproducible, or dependable (or politically expedient in some cases) as digital solutions.
5. The memory is required to search the data i.e. to read the data in Mozilla, Google, etc.

VI. CONCLUSION

The proposed Memory (NVSRAM) is designed using 45 nm CMOS/VLSI technology with Microwind 3.1. The Software used in program allows us to design and simulate an integrated circuit at physical description level. The nonvolatile characteristic and nanoscaled geometry of the SRAM cell i.e. NVSRAM with CMOS process technology increases the memory cell packing density, reduces power dissipation and provides for new approaches towards power reduction without loss of stored data. Proposed layout of NVSRAM consumes a very low power of 1.440mW.Also because of 45nm technology it covers very less area. As the main aim of the memory is to store the data whatever the input data is given to the memory , it is expected that output data should be equal to the input data.

VII. FUTURE SCOPE

As the technology increases, performance speed of chip increases, power consumption decreases, chip area decreases, etc. The same layout design of 45nm technology can be used in increasing technology such as 22nm, 18nm and so on. Non-volatile SRAM cell is used for high performance future search engines.

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