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Design and Implementation of 4-Bit ALU using FinFET Technology

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ABSTRACT: In VLSI technology, continuous scale down of the transistor proves the Moore's law which states that the number of transistors per square inch on integrated circuits had doubled every year since their invention.Scaling down in the MOS transistor increased the interconnections and limits the circuit density.There are major design issues in MOSFET due to scaling such as Gate oxide tunnelling leakage, Self-heating,Soft Error Rate,Strained-Si channel and high-K gate. Due to these design issues there are more limitations and the major challenge is power consumption.To reduce such challenges and keep shrinking the size of transistor will attain the certain level of achievements in Nano electronics with the help of FinFET. In terms of its structure, it typically has a vertical fin on a substrate which runs between a larger drain and source area. This protrudes vertically above the substrate as a fin. The gate orientation is at right angles to the vertical fin. And to traverse from one side of the fin to the other it wraps over the fin, enabling it to interface with three side of the fin or channel. This form of gate structure provides improved electrical control over the channel conduction and it helps reduce leakage current levels and overcomes some other short-channel effects.

This project mainly focuses on implementation of 4-Bit Arithmetic Logic Unit (ALU) using FinFET technology. An ALU which acts as core part of CPU is a combinational digital electronic circuit that performs arithmetic and bitwise operations on integer binary numbers. The design of 4-bit ALU of the ripple carry adder model, performs four arithmetic and four logical operations. The four arithmetic operations include addition, subtraction, increment and decrement. The four logical operations such as and, or, not & identity. In the implementation of FinFET based ALU , it is possible to operate at lower operating voltages because FinFET has lower threshold voltages, power consumption is expected to be reduced and speed performance is expected to be improved

KEYWORDS: FinFET, Tunnelling

I. INTRODUCTION

In 1947, there was the point-contact transistor. This was the very first transistor ever made, built by Walter Brattain with the help of John Bardeen. It was made of two gold foil contacts sitting on a germanium crystal. In 1951, the first big change in transistors occurred when William Shockley developed a junction transistor. The first junction transistors were sandwiches of N- and P-type germanium (germanium with an excess and scarcity of electrons, respectively). A weak voltage coming into the middle layer would affect another current traveling across the entire sandwich. The next big jump in transistor evolution came with the field-effect transistor in 1960's. Most modern transistors are field-effect transistors -- specifically metal-oxide semiconductor field-effect transistors, or "MOSFETs." Instead of being a sandwich, MOSFETs have a channel of either N- or P- type semiconductor running through a ridge on top of the other type. The working principle of MOSFET depends up on the MOS capacitor. The MOS capacitor is the main part. The semiconductor surface at below the oxide layer
and between the drain and source terminal can be inverted from p-type to n-type by applying a positive or negative gate voltages respectively. When positive gate voltage is applied, the holes present beneath the oxide layer experience repulsive force and the holes are pushed downward with the substrate. The depletion region is populated by the bound

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negative charges, which are associated with the acceptor atoms. The positive voltage also attracts electrons from the n+ source and drain regions in to the channel. The electron reach channel is formed. Now, if a voltage is applied between the source and the drain, current flows freely between the source and drain gate voltage controls the electrons concentration the channel. Instead of positive if negative voltage is applied, a hole channel will be formed beneath the oxide layer.

The Moore's law was the observation made on the scaling of transistors. This law refers to an observation made by Intel co-founder Gordon Moore in 1965. He noticed that the number of transistors per square inch on integrated circuits had doubled every year since their invention

The challenges faced due to scaling down of transistors are:

a)Effect due to Gate dielectric thickness

The gate electrode together with gate dielectric control the switching operation of CMOS transistors. The voltage of the gate electrode controls the flow of electric current across the transistor. The gate dielectric should be made as thin as possible to increase the performance of the transistor. In additional, it is critical to keep short channel effects under control when a transistor is turned on and reduce subthreshold leakage when a transistor is off. In order to maintain the electric field as CMOS transistors are scaled, the gate dielectric thickness should also be shrunk proportionally. An oxide thickness of 3 nm is needed for CMOS transistors with channel lengths of 100 nm or less. This thickness comprises only a few layers of atoms and is approaching fundamental limits which is around 1 to 1.5 nm. The thin oxide layer gives rise to a gate leakage current that increases exponentially as the oxide thickness is scaled down. This tunnelling current can initiate a damage leading to the fallible of the dielectric.

b) Effects due to Short channel

Short channel enables faster switching operation since less time is needed for current to flow from source to drain. Howbeit, several negative effects could arise from it. A high off-state drain leakage current, I_{off} flow even though the transistor is turned off. The band diagrams in Figure 1.5(c) and 1.5(d) represent the energy barrier that majority carriers in the source terminal needs to overcome to enter the channel for the original device and scaled version, respectively. As we can see in Figure 1.5(d), the barrier height is lowered thus reduces the threshold voltage used to form a depletion layer. Both ends of this short-channel may merge when a sufficiently large reverse-bias voltage is applied to the drain terminal. Consequently, many majority carriers start to flow from source to drain even if the gate voltage is below the threshold value, which result in punch-through, drain-induced barrier lowering (DIBL) and threshold voltage roll-off. These three problems cause drop in threshold voltage level, subsequently leakage currents.

c) Effects due to lowering power and threshold voltages

Scaling the power supply voltage enables the reduction in dynamic power dissipation. While reducing the power supply of a chip might seem straightforward, nevertheless, it leads to issues such as noises and possibly signal levels compatibility problems in multichip systems using various supply voltages. Reduction in power supply, which also reduces threshold voltage also increases static power during transistor off due to leakage current. As threshold voltage is reduced as well, the transistor cannot be completely turned off. The transistor operates in a weak-inversion mode, with a subthreshold leakage between source and drain. The reduction of threshold voltage of about 85 mV will increase the subthreshold leakage current by 10 times. Hence, it results in degradation of power and speed efficiency

d) Effects due to High electric fields

As mentioned above, the supply voltage cannot be reduced in proportion to channel length, hence the scaling will increase the electric field strength across the gate oxide. Carrier mobilities are degraded due to higher vertical electric fields in MOSFET channel which in worst cases can cause breakdown of the barrier and hence higher leakage currents which can cause damage to the device.

e) Effects due to parasitic resistances and capacitances

As transistor dimensions are reduced, parasitic resistances and capacitances both scale unfavourably with reduced pitch. Therefore, influence of parasitic elements on oncurrent increases significantly. These parasitic elements will diminish the performance gain by transistor scaling.

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f) Effects due to Increasing channel doping

In order to control short channel effects, it is desirable to increase the channel doping. In a heavily doped channel, carrier mobility decreases severely due to high transverse electric field and impurity scattering. The on-state drain current, Ion, is reduced due to larger capacitance in high depletion-charge channel. In addition, a high channel doping will also result in band to band tunnelling leakage. Therefore, increasing the channel doping will negatively impact the CMOS performance and functionality.

g) Hot-carrier Effect

When carriers possess high energies having effective temperature greater than the lattice temperature, they are said to be hot. These carriers are not in thermal equilibrium with the lattice because they cannot transfer their energies to the lattice atoms fast enough. They are generated in inverted channel region when MOSFET is operating in linear or saturation mode. The main problems which arise due to hot carriers are parasitic gate currents, drain current degradation, decrease in trans-conductance, and shift of threshold voltage with time. Using graded drain profile reduces generation of hot carriers

h) Effects due to Interconnect delays

Reduction of the wire width increases the resistance and hence increases the delay. This reduces the speed and hence device may not function much faster due to large interconnect delays. The purpose of scaling is not only to increase the device density on chip but also to increase its speed

At the current pace of scaling, the industry predicts that planar transistors will reach feasible limits of miniaturization by 2010, concurrent with the widespread adoption of 32 nm technologies. At such sizes, planar transistors are expected to suffer from undesirable short channel effect, especially "off-state" leakage current, which increases the idle power required by the device.

A multi-gate device or multiple-gate field-effect transistor (MuGFET) refers to a MOSFET (metal–oxide–semiconductor field-effect transistor) that incorporates more than one gate into a single device. The multiple gates may be controlled by a single gate electrode, wherein the multiple gate surfaces act electrically as a single gate, or by independent gate electrodes. A multi-gate device employing independent gate electrodes is sometimes called a **multiple-independent-gate field-effect transistor** (**MIGFET**). Multi-gate transistors are one of the several strategies being developed by CMOS semiconductor manufacturers to create ever-smaller microprocessors and memory cells, colloquially referred to as extending Moore's law.

II. FINFET

Introduction of FinFET

A FinFET is classified as a type of multi-gate Metal Oxide Semiconductor Field Effect Transistor (MOSFET). It was first developed at the University of Berkley, California by Chenming Hu and his colleagues. A multi-gate transistor incorporates more than one gate in to one single device. In FinFET, contrast to planar MOSFETs the channel between source and drain is built as a three dimensional bar on top of the silicon substrate, called fin. A thin silicon film wrapped over the conducting channel forms the body. The name has been derived from the fact that the structure, when viewed, looks like a set of fins. The thickness of the device determines the channel length of the device. The channel length of a MOSFET is said to be the distance between the source and drain junctions. It is a non-planar, double gate transistor which based either on the Bulk Silicon-On-Insulator (SOI) or on silicon wafers. It is based on the single gate transistor design.

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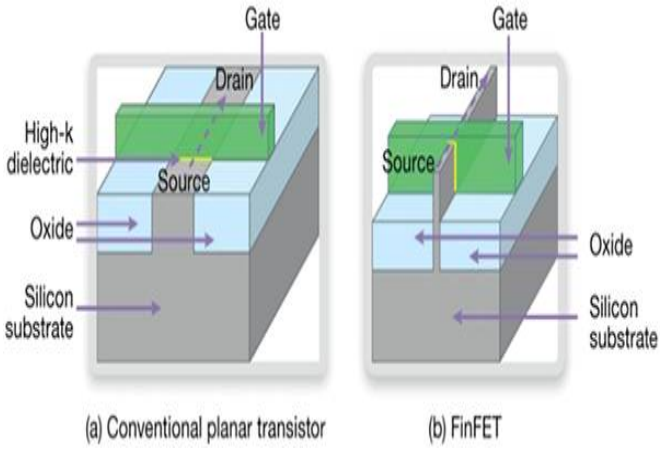

Fig.2.1 Conventional transistor vs FinFET

The gate of the FinFET is wrapped around (a wrap-around gate!) which reduces leakage current thereby increasing effectiveness.
There are two types of FinFETS:

1. Bulk FinFET
2. SOI FinFET

The 'types' of FinFETS are nothing but the 'base' onto which it is fabricated. This means that FinFETS can be made either on SOI wafers or regular silicon wafers.

Working Principle of FinFET

The working principle of a FinFET is similar to that of a conventional MOSFET. The MOSFET can function in two modes: enhancement mode and depletion mode for both p-channel and n-channel MOSFETs.The channel shows maximum conductance when there is no voltage on the gate terminal. As the voltage changes to positive or negative, the conductivity of the channel reduces.

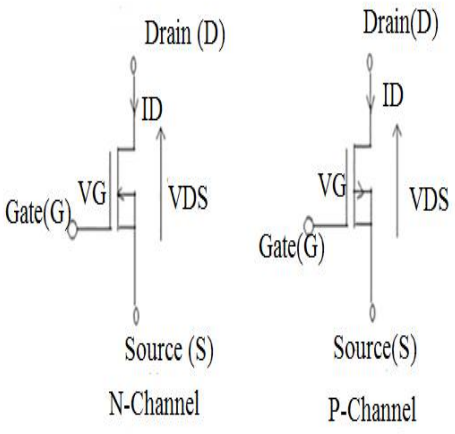

Fig.2.2 Depletion mode of MOSFET

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In enhancement mode of MOSFET, when there is no voltage on the gate terminal, it does not conduct. Unlike the depletion mode, in enhancement mode, the device conducts better when there is more voltage on the gate terminal.

The main aim of the MOSFET is to control the flow of voltage and current between the source and drain terminals. A high quality capacitor is formed by the gate terminal. The gate is composed of the silicon oxide layer, the p-body silicon and gate metallization and the p-body silicon. This capacitor is the most vital part. The semiconductor surface at the below oxide layer which is located between source and drain terminal. This is inverted from p-type to n-type by applying a positive or negative gate voltage respectively. When a small amount of voltage is applied to this structure (the capacitor), keeping gate terminal positive with respect to source, a depletion region is formed. This depletion region is formed at the interface between the silicon and the SiO2.The positive voltage applied attracts electrons from the source terminal, the drain terminal as well as the n+ source. This forms the electron reach channel. If voltage is applied between the source and drain terminals, current will flow between source and drain terminals. The concentration of electrons is controlled by the gate voltage (Vg).

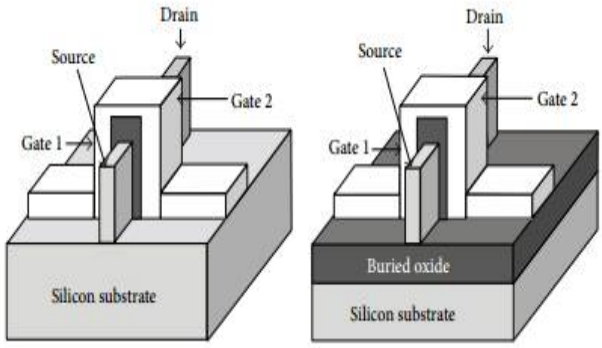

Fig 2.3. Representation of FinFET

If a negative voltage is applied, a hole channel will be formed under the oxide layer. Now, the controlling of source to gate voltage is responsible for the conduction of currentbetween source and the drain. If the gate voltage exceeds a given value, only then does the conduction begins.

Arithmetic Logic Unit

An arithmetic logic unit (ALU) is a digital circuit used to perform arithmetic and logic operations. It represents the fundamental building block of the central processing unit (CPU) of a computer. Modern CPUs contain very powerful and complex ALUs. In addition to ALUs, modern CPUs contain a control unit (CU).

Most of the operations of a CPU are performed by one or more ALUs, which load data from input registers. A register is a small amount of storage available as part of a CPU. The control unit tells the ALU what operation to perform on that data and the ALU stores the result in an output register. The control unit moves the data between these registers, the ALU, and memory.

Design of 4 bit ALU using FinFET

The design of 4-bit ALU of the ripple carry adder model using FinFET, which performs four arithmetic and four logical operations. The four arithmetic operations include ADD, SUBTRACT, INCREMENT and DECREMENT. The four logical operation are AND, OR NOT and IDENTITY. 4-bit ALU is designed by cascading four I-bit ALU blocks. Each 1bit ALU is composed of the following four components:

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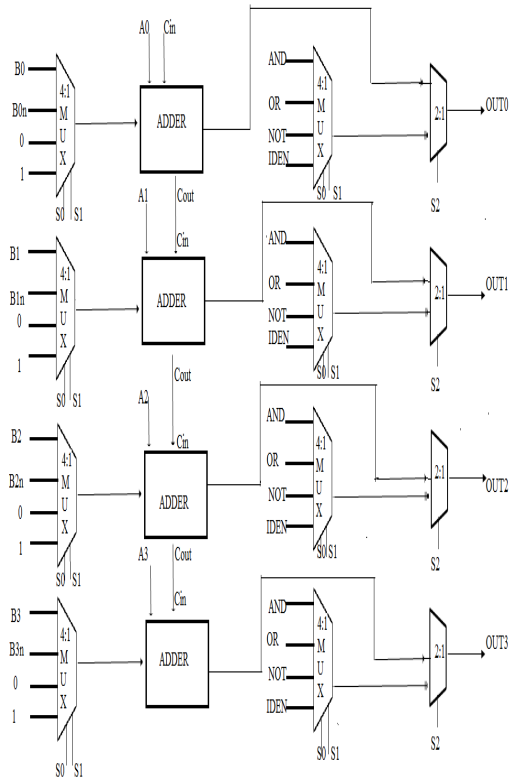

Fig 2.4. Block Diagram of 4-bit ALU

l. Arithmetic 4: 1 multiplexer,
2. Full adder,
3. Logical 4: 1 multiplexer,
4. 2: 1 multiplexer to select either arithmetic or logical operation

Each bit uses three multiplexers and one full adder.
The block diagram of 4-bit ALU is shown in the figure .The 4: 1 multiplexers have two select inputs SO and SI. The MUXs are used to provide the proper input signal for the adder circuit depending on the operation being performed on the proper input signal and also to pass the output of the full adder to 2:1 multiplexer for further selection. The select line S2 used for 2: 1 MUX for selecting the arithmetic function (S2=O) and logical function (S2=1), as shown in table.

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Table 2.1. Operation of ALU

S2	S1	S0	Mnemonics	Description
0	0	0	Addition	Add Data-A and Data-B Data-A + Data-B = Result C is Carry for Addition
0	0	1	Subtraction	Subtract Data-A and Data-B Data-A - Data-B = Result C is Borrow for Subtraction
0	1	0	Increment	Increment Data-A by 1 Data-A + 1 = Result Carry bit has to be 1 Data-B has to be 0
0	1	1	Decrement	Decrement Data-A by 1 Data-A - 1 = Result Carry bit has to be 0 Data-B has to be 1
1	0	0	AND	Logical AND for Data-A and Data-B Data-A & Data-B = Result C is Don't Care
1	0	1	OR	Logical OR for Data-A and Data-B Data-A | Data-B = Result C is Don't Care
1	1	0	NOT	Logical NOT for Data-A (~Data-A) = Result C is Don't Care
1	1	1	IDENTITY	Logical IDENTITY for Data-A Data-A + 0 = 0 and Data-A + 1 = 1 C is Don't Care

In the figure, the logical operations are performed using the basic logic gates, the delay for each logic operation would be delay through the gate. The Arithmetic operations make use of the complete adder. Increment and decrement operations are special cases of addition and subtraction. Increment operation is equivalent to an addition by l and subtraction is equivalent to 2's complement addition. The delay for each arithmetic operation is more complex than that of the logical operation as it depends not only on the type of logic used to construct the SUM and CARRY units of the full adder, but also input pattern and the critical paths in the circuit. Optimizing the design of the full adder optimizes all operations to some extent.

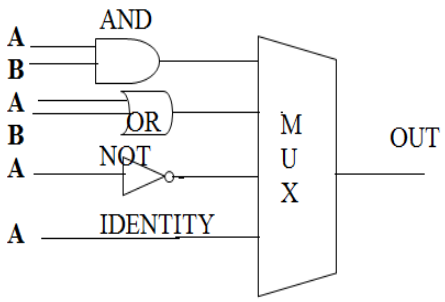

Fig 2.5. Block diagram of 4: I MUX performing logical operation

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Working of ALU

The blocks designed while developing the 4-bit ALU that performs eight different operations are:

- Exclusive -OR, AND, OR and INVERTER gates
- 2:1 Multiplexer
- 4:1 Multiplexers
- Full Adder block

Logic Gates and Buliding Blocks of ALU

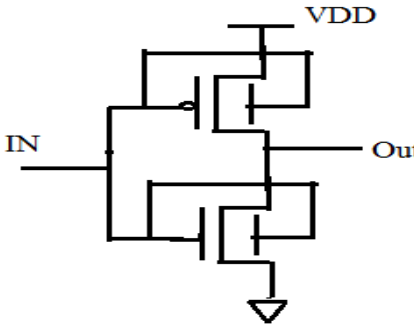

Fig 2.12. INVERTER using FinFET

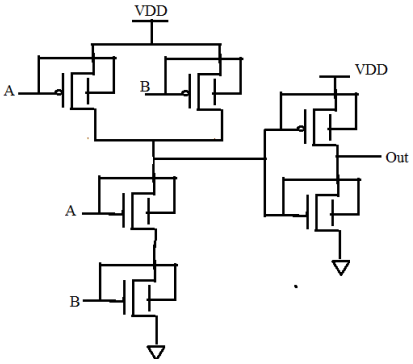

Fig 2.13. AND gate using FinFET

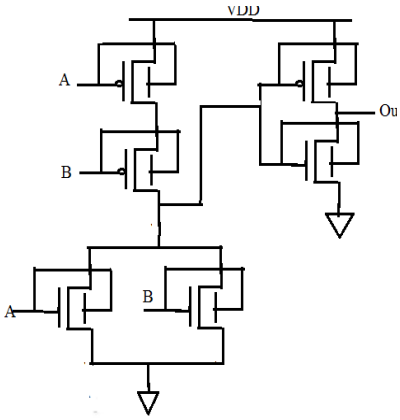

Fig 2.14. OR gate using FinFET

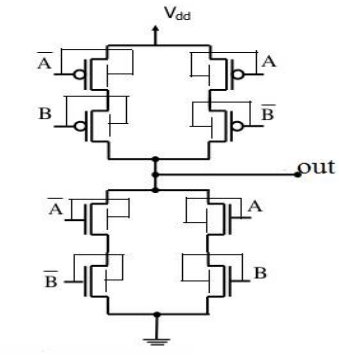

Fig 2.15. XOR gate using FinFET

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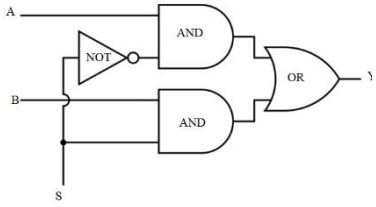

Fig.2.10 2:1 Mux

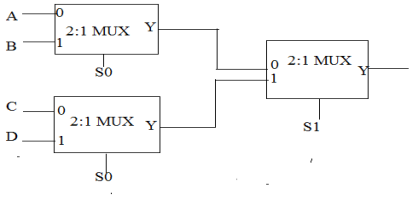

Fig.2.11. 4:1 Mux using 2:1 Mux

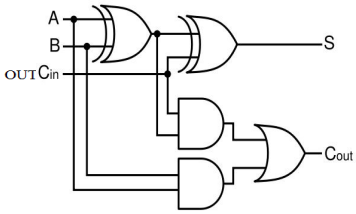

Fig.2.12. Schematic of Full Adder

III. GATE DIFFUSION INPUT

Introduction of Gate Diffusion Logic (GDI)

Among the forceful investigation in the field of low power, high speed digital applications due to the growing demand of systems like phones, laptop, palmtop computers, cellular phones, wireless modems and portable multimedia applications etc., has directed the VLSI technology to scale down to Nano-regimes, allowing additional functionality to be incorporated on a single chip. The designer's novel purpose in the field of multifaceted digital circuit design is minimization of power consumption. These investigations are responsible for special design techniques for digital circuits distant from conventional CMOS design style. A large body of investigate has been performed to expand and advance conventional Complementary Metal Oxide Semiconductor (CMOS) techniques for the fabrication of ULTRA low power integrated circuits (ICs). The purpose of this study is to expand a faster, lower power, and reduced area substitute to standard CMOS logic circuits. Mod-GDI technique is one such new technique for minimization of power consumption in the digital circuit design field.

Morgenshtein.A investigated a high-speed and multipurpose logic style for low power electronics design, known as Gate Diffusion Input (GDI), with reduced area and power necessities, and proficient of implementing a broad variety of logic functions. Fig.3.1 shows basic GDI logic cell, which is used for implementing verity of logic functions and circuits at low power and high speed design where G, P and N are three inputs and output is taken from D terminal. Table represents the logic functions which can be implemented with the help of this basic GDI cell.

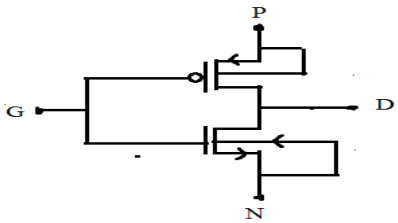

Fig 3.1. GDI logic

Table 3.1. Truth table for GDI

N	P	G	OUT	Function
0	B	A	A'B	F1
B	'1'	A	A'+B	F2
'1'	B	A	A+B	OR
B	'0'	A	AB	AND
C	B	A	A'B+AC	MUX
'0'	'1'	A	A'	NOT

Modified GDI Logic:

Power dissipation becomes most important restriction in high performance applications. Optimizations for basic logic gates are fundamental in order to get better the performance of a variety of low power and high performance devices. These limitations can be overcome by modified gate diffusion input (Mod-GDI) logic style. This technique allows reducing power consumption, delay and area of digital circuits. Fig shows basic Mod-GDI logic style. In contrast with the basic GDI cell, Modified-GDI [Mod-GDI] cell contains a low-voltage terminal SP configured to be connected to a high constant voltage (i.e. supply voltage) and a high-voltage terminal SN configured to be connected to a low constant voltage (i.e. Ground). Including terminals these ensures that the Mod-GDI cell can be implemented with all current CMOS technologies

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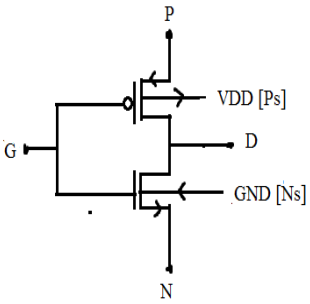

Fig 3.2. Modified GDI logic

Table 3.2. Truth table for modified GDI logic

N	Ns	P	Ps	G	D	Function
0	0	1	1	A	A’	INVERTER
A	A	0	A	B	AB	AND
1	0	A	D	B	A+B	OR
A’	0	A	1	B	A’B+AB’	XOR
A	0	A’	1	B	AB+A’B’	XNOR
0	0	B	B	A	A’B	FUNCTION1
B	0	1	1	A	A’+B	FUNCTION2
B	0	B	1	A	A’B+AC	MUX

Logic Gates using Mod-Gdi Logic

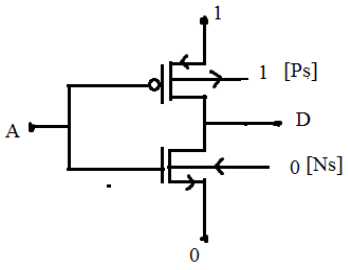

Fig 3.3. INVERTER using FinFET in Mod-GDI

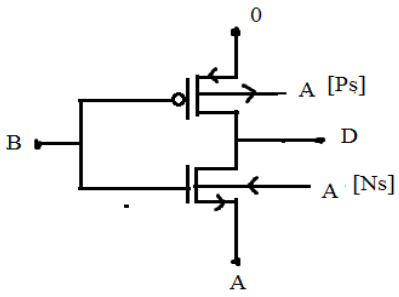

Fig 3.4. AND gate using FinFET in Mod-GDI

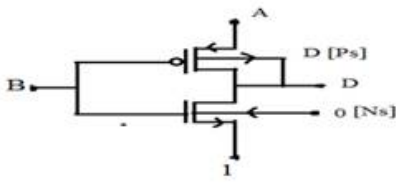

Fig 3.5. OR gate using FinFETS in Mod-GDI

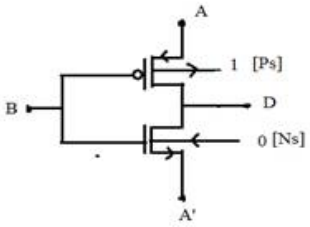

Fig 3.6. XOR gate using FinFET in Mod-GDI

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IV. IMPLEMENTATION

By Cascading the blocks of arithmetic mux, Full adder, Logical Mux and 2;1 Mux both in Conventional logic and Modified Gdi Logic operations of ALU can be performed.

V. SIMULATIONS AND RESULTS

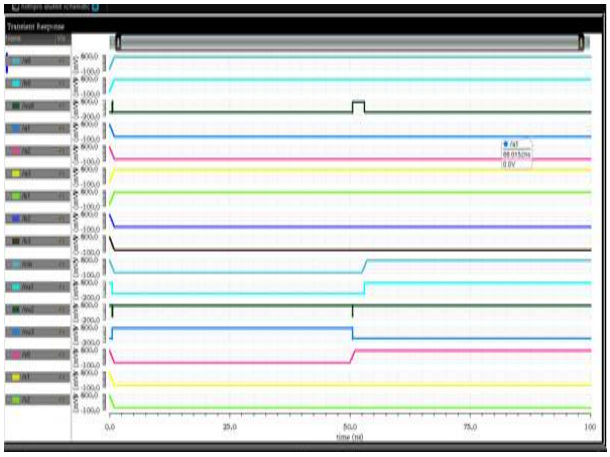

Fig 5.1. Addition and Subtraction Simulation Results of 4-bit ALU

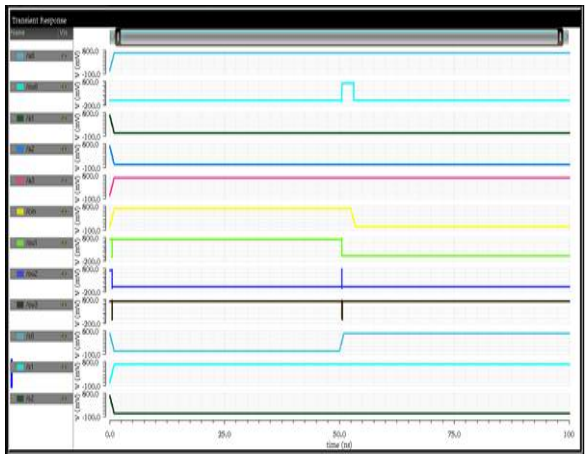

Fig 5.2. Increment and Decrement Simulation Results of 4-bit ALU

Using FinFETusing FinFET

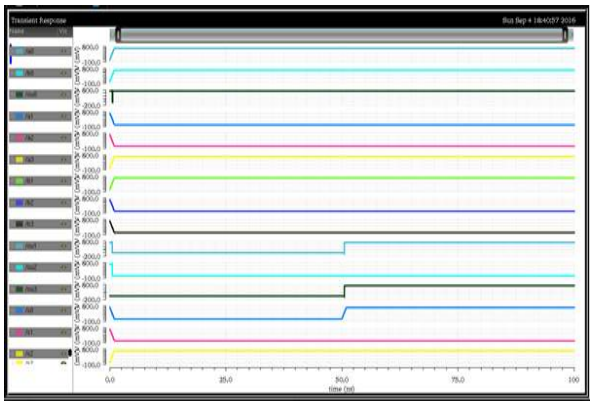

Fig 5.3. AND and OR Simulation Results of 4-bit ALU using FinFET

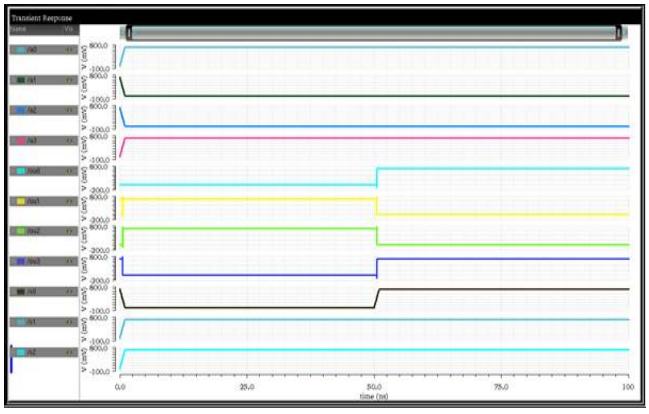

Fig 5.4. Not and Identity Results of 4-bit ALU using FinFET

Analysis :

Logic gates required for ALU i.e Inverter, And, Or and Xor are designed using Modified- GDI logic and the power dissipation of these logic gates are reduced using Modified GDI logic. Now the Full adder and Mux are designed using these basic logic gates so that the power dissipation of Full adder and Mux are reduced in Modified-GDI logic compared to conventional logic.

All these basic blocks are cascaded and 4-Bit ALU is designed in Modified-GDI logic. We can observe that the power dissipation of 4-bit ALU is reduced in Modified GDI logic compared to conventional Logic from the Table 5.1

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Table 5.1: Power analysis of conventional and Mod-GDI FinFETALU

S.NO	TYPE OF GATE	POWER IN FINFET(mw)	POWER IN Mod-GDI LOGIC using FinFET(mw)
1	INVERTER	0.693	0.660
2	OR	1.493	0.183
3	AND	1.986	0.610
4	XOR	2.699	0.991
5	FULL ADDER	12.076	2.763
6	MUX2X1	3.628	0.249
7	MUX4X1	12.933	0.607
8	ARITHMETIC MUX	10.976	1.042
9	LOGICAL MUX	19.708	0.829
10	1-BIT ALU	46.62	16.415
11	4-BIT ALU	54.028	37.97

VI. CONCLUSION

The design of the 4-bit ALU have been designed by using the sub blocks of full Adder, 4xl and 2xl multiplexers, and gates like exclusive-or, and, or and inverter in both conventional FinFETs and in Mod-GDI logic. The ALU performs a total of eight operations, out of which four are arithmetic and remaining are logical operations. The four arithmetic operations performed are Addition, Subtraction, Increment and Decrement and the four logical operations are And, Or, Invert and Identity. The selections of these operations are made by the selection lines S(2), S(1) and S(0). The average power dissipated for 4-bir ALU in conventional and Mod GDI logic is 54.028 mw and 37.97 mw respectively.

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