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High Resolution and Low Power Frequency Divider by Multi Pre-Scalar

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ABSTRACT: The demand for lower cost, lower power, and multiband RF circuits increased in conjunction with need of higher level of integration. In this project a low-power single-phase clock multiband flexible divider for Bluetooth, Zigbee, and Network standard's 802.15.4 and 802.11 a/b/g Wireless LAN frequency synthesizers is proposed based on pulse swallow topology and is implemented. The frequency synthesizer, usually implemented by a phase-locked loop (PLL), is one of the power-hungry blocks in the RF front-end and the first-stage frequency divider consumes a large portion of power in a frequency synthesizer. The proposed pre-scalar based approach reduces the area and power significantly. The multiband divider consists of a proposed wideband multi modulus 32/33/47/48 pre-scalar and an improved bit-cell for swallow (S) counter and can divide the frequencies in the three bands of 2.41–2.483 GHz, 5.14–5.30 GHz, and 5.715–5.815 GHz with a resolution selectable from 1 to 25 MHz The proposed multiband flexible divider is silicon verified and consumes power of 0.96 and 2.2 mw in 2.3-and 5-GHz bands, respectively, when operated at 1.8-V power supply. The proposed pre-scalar is achieved by without using any additional flip flops. It gives a solution to the low power PLL synthesizers for wide range of communication applications.

KEYWORDS: Pre-scalar, Dynamic logic, pluse- swallow topology, PLL synthesizer, Zigbee, Bluetooth.

I.INTRODUCTION

Wireless LAN (WLAN) in the multi gigahertz bands, such as HIPER LAN II and Network standards like a 802.11a/b/g, are recognized as leading standards for high-rate data transmissions, and standards like Network protocol 802.15.4 are recognized for low-rate data transmissions. . The integrated synthesizers for Wireless LAN applications at 5GHz reported in and consume up to 24 mw in CMOS realizations, where the first-stage divider is implemented using an Injection-locked divider which consumes large chip area and has a narrow locking range in [12] .The best published frequency synthesizer at 5 GHz consumes 9.6 mw at 1-V supply presented in[3], where its complete divider consumes power around 6 mw, where the first-stage divider is implemented using the source-coupled logic (SCL) circuit, which allows higher operating Frequencies but uses more power. Dynamic latches are faster and consume less power compared to static dividers.

High speed divide-by- counter (also called pre-scalar) is a fundamental module for frequency synthesizers. Its design is crucial because it operates at a higher frequency and consumes higher power consumption. A divide-by-counter consists of flip-flops (FF) and extra logic, which determines the terminal count. Conventional high speed FF based divide by counter designs use current-mode logic (CML) latches [1] and suffer from the disadvantage of large load capacitance. This not only limits the maximum operating frequency and current drive capabilities, but also increases the total power consumption. Alternatively, FF based divide-by designs adopt dynamic logic FFs such as true single-phase clock (TSPC) [2]–[4].

The designs can be further enhanced by using extended true single phase clock (E-TSPC) FFs for high speed and low power applications [5]–[10]. E-TSPC designs remove the transistor stacked structure so that all the transistors are free of the body effect. They are thus more sustainable for high operating frequency operations in the face of low voltage supply. Past optimization efforts on pre-scalar designs focused on simplifying the logic part to reduce the circuit complexity and the critical path delay. For example, an E-TSPC design embedded with one extra P-MOS/N-MOS transistor can form an integrated function of FF and AND/OR logic [7]. Moving part of the control logic to the first FF to reduce unnecessary FF toggling yields another version of pre-scalar design [8].These two classic designs each contains 16 transistors only and the mode control logic uses as few as 4 transistors. To achieve such circuit

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simplicity, it calls for a rationed structure in the FF design. Despite its distinct speed performance, the incurred static and short circuit power consumptions are significant. Latest designs presented in [10] adopt a general TSPC logic family containing both rationed and ratio less inverter alternatives. Since the maximum height of transistor stacking is up to 5, these designs lose their performance advantages when working under a low scenario. In [11], a power gating technique by inserting an extra PMOS between and the FF is employed in two novel divide-by-2/3 counter designs. The unused FF can be shut down when working in the divide-by-2 mode. Due to the increase in the number of transistor stacking (up to 4), these designs are not suitable for low operations. Due to the quadratic dependence of power consumption on supply voltage, lowering is a very effective measure to reduce the power at the expense of speed performance. .In particular, here focus on low operations for power saving without sacrificing the speed performance. In this design, rationed E-TSPC FFs are employed due to its circuit simplicity and speed performance. Only one pass transistor is needed to implement the mode control logic. The proposed design in capable of working at a maximum frequency of 531 MHz when the supply voltage is as low as 0.6 V.

The TSPC and E-TSPC designs are able to drive the dynamic latch with a single clock phase and avoid the skew problem [13]. However, the adoption of single-phase clock latches in frequency dividers has been limited to PLLs with applications below 5GHZ. The frequency synthesizer reported in [6] uses an E-TSPC pre-scalar as the first stage divider, but the divider consumes around 6.25 mw. Most Network protocol 802.11a/b/g frequency synthesizers employ SCL dividers as their first stage, while dynamic latches are not yet adopted for multiband synthesizers. In this paper, a dynamic logic multiband flexible integer-N divider based on pulse-swallow topology is proposed which uses a low-power wideband 2/3 pre-scalar and a wideband multi modulus 32/33/47/48 pre-scalar as shown in Fig. 1. The divider also uses an improved low power loadable bit-cell for the Swallow counter.

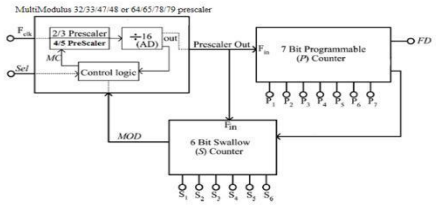

Fig.1: Proposed dynamic logic Multiband flexible divider

II.DESIGN CONSIDERATIONS

The key parameters of high-speed digital circuits are the propagation delay and power consumption. The maximum operating frequency of a digital circuit is calculated and is given by

$$F_{max} = \frac{1}{T_{PLH} + T_{PHL}} \quad (1)$$

The total power consumption of the CMOS digital circuits is determined by the switching and short circuit power. The switching power is linearly proportional to the operating frequency and is given by the sum of switching power at each output node as in

$$P_{switching} = \sum_{i=1}^{n} f_{clk} C_{li} V_{dd}^2 \quad (2)$$

Where n is the number of switching nodes, f_{clk} is a clock frequency C_{Li} is the load capacitance at the output node of the ith stage, and Vdd is the supply voltage. Normally, the short-circuit power occurs in dynamic circuits when there exists direct paths from the supply to ground which is given by

$$P_{sc} = I_{sc} V_{dd} \quad (3)$$

The short-circuit power is much higher in E-TSPC logic circuits than in TSPC logic circuits. However, TSPC logic circuits exhibit higher switching power compared to that of E-TSPC logic circuits due to high load capacitance. For the ETSPC logic circuit, the short-circuit power is the major problem. The E-TSPC circuit has the merit of higher operating frequency than that of the TSPC circuit due to the reduction in load capacitance, but it consumes significantly more power than the TSPC circuit does for a given transistor size.

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III.PROPOSED SYSTEM

The implementation of proposed system is shown in figure 1 and each modules are discussed below.

A. Wide band E-TSPC 2/3 Pre-scalar

The E-TSPC 2/3 pre-scalar consumes large short circuit power and has a higher frequency of operation than that of TSPC 2/3. The wideband single-phase clock 2/3 pre-scalar used in this design do not consist of two D-flip-flops and two NOR gates embedded in the flip flops as in Fig. 2. The first NOR gate is embedded in the last on DFF1, and the second NOR gate is embedded in the first stage of DFF2.

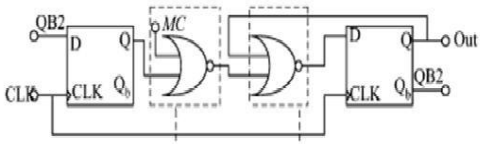

Fig.2: Wideband Single-Phase clock 2/3 Pre-scalar

B. Multimodulus 32/33/47/48 Pre-scalar

The proposed wideband multi modulus pre-scalar which can divide the input frequency by 32, 33, 47, and 48 is shown in Fig.3. It is similar to the 32/33 pre-scalar but with an additional inverter and a multiplexer. The proposed pre-scalar performs additional divisions (divide-by-47 and divide-by-48) without any extra flip flop, thus saving a considerable amount of power and also reducing the complexity of multi band divider.

Case 1: sel='0'

When sel='0', the output from the NAND2 gate is directly transferred to the input of 2/3 pre-scalar and the multi modulus pre-scalar operates as the normal 32/33 pre-scalar, where the division ratio is controlled by the logic signal MOD. If MC=I, the 2/3 pre-scalar operates in the divide-by-2 mode and when MC=O, the 2/3 pre-scalar operates in the divide-by-3 mode. If MOD=I, the NAND2 gate output switches to logic "I" (MC=I) and the wideband pre-scalar operates in the divideby-2 mode for entire operation. The division ratio N performed by the multi modulus pre-scalar is

$$N=(AD*N1)+(0*(N1+1))=32 \quad (4)$$

Where N =2 and AD=16 is fixed for the entire design. If MOD=O , for 30 input clock cycles MC remains at logic "1", where wideband pre-scalar operates in divide-by-2 mode and, for three input clock cycles, MC remains at logic "0" where the wideband pre-scalar operates in the Divide-by-3 mode. The division ratio N+ 1 performed by the multi modulus pre-scalar is

$$N+1=((AD1)*N1)+(1*(N1+1))=33 \quad (5)$$

Case 2: sel ='l'

When sel=' 1', the inverted output of the NAND2 gate is directly transferred to the input of 2/3 pre-scalar and the multi modulus pre-scalar operate as a 47/48 pre-scalar, where the division ratio is controlled by the logic signal MOD. If MC= 1, the 2/3 pre-scalar operates in divide-by-3 mode and when MC=O, The 2/3 pre-scalar operates individe-by-2 mode which is quite opposite to the operation performed when sel='O' If MOD=I, the division ratio N+ 1 performed by the multimodulus pre-scalar is same except that the wideband pre-scalar operates in the divide by-3 mode for the entire operation given by

$$N+1=((AD*(N1+1))+(0*N1)) = 48 \quad (6)$$

If MOD=I, the division ratio N performed by the multi modulus pre-scalar is

$$N=((AD-1)*(N1+1))(1*N1) = 47 \quad (7)$$

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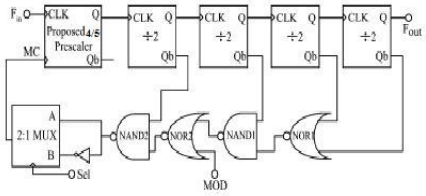

Fig.3: Proposed Multi modulus 32/33/47/48 Pre-scalar

C. Multiband Flexible Divider

It consists of Multi modules 32/33/47/48 pre-scalar, a 7-bit programmable counter and 6-bit swallow counter. Here the pre-scalar is briefly discussed in the section. The control signal SEL decides whether the divider is operating in lower frequency band (2.3 GHZ) or higher band (5-5.75 GHZ).

D. Swallow (S) Counter

The 6-bit s-counter consists of six asynchronous loadable bit-cells, a NOR-embedded DFF and additional logic gates to allow it to be programmable from 0 to 31 for low-frequency band and from 0 to 47 for the high-frequency band. The asynchronous bit cell used in this design shown in Fig.4. Is similar to the bit-cell except it uses two additional transistors M6 and M7whose inputs are controlled by the logic signal MOD. If MOD is logically high, nodes S 1 divide-by-48) and P, S counters start down counting the input clock cycles. When the S-counter finishes counting, MOD switches to logic "1" and the pre-scalar changes to the divide-by-n mode (divide-by-32 or divide-47) for the remaining P-S clock cycles.

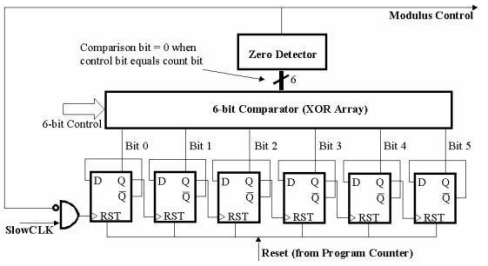

Fig.4: Block Diagram of A 6-bit Swallow Counter

E. Programmable (P) Counter

The programmable P-counter is a 7-bit asynchronous down counter which consists of 7 loadable bit-cells and additional logic gates. Here, bit P7 is tied to the Sel signal of the multi modulus prescaler and bits P 4 and P7 are always at logic "1." The remaining bits can be externally programmed from 75 to 78 for the lower frequency band and from 105 to
122 for the upper frequency band. When the P-counter finishes counting down to zero, LD switches to logic "1" during which the output of all the bit-cells in S-counter switches to logic "1" and output of the NOR embedded DFF switches to logic "0" (MOD=O) where the programmable divider get reset to its initial state and thus a fixed division ratio is achieved.

IV. SIMULATION AND SYNTHESIS REPORTS

The proposed system is implemented by using Xilinx software and the simulation waveforms of each module are shown below:

*Pre-scalar:*Pre-scalar can divides the given frequency based on mode selected i.e. 2/3 modes. When 'MC' control generates by Swallow counter the pre-scalar starts the division of input clock frequency. The simulation waveform is shown in figure5.

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Top Module: The final output is by the total contribution of pre-scalar, program counter and Swallow counter which gives a combination of two different counts and frequency division. The simulation waveform is shown in figure 6.

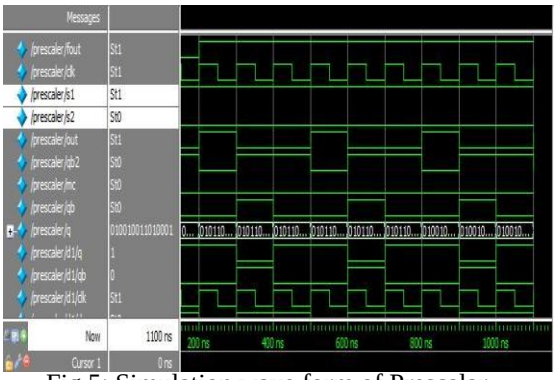

Fig.5: Simulation wave form of Prescalar

Fig.6: simulation waveform of Top Module

Comparisons with Other Systems

In table I, Comparisons of divide by 2 modes and divide by 3 modes at 2.5GHz in [6] and [12] is shown. In table II Comparison of proposed methods with existing methods [9] and [6] are presented.

Table I
Comparisons of Divide Modes

Design Parameters	[6]	[12]	Proposed
Process(µm)	0.18	0.18	0.18
Supply Voltage(V)	1.8	1.8	1.8
Max. Frequency (GHz)(Sim/Measured)	6.7/5.3	7.5/6	8/6.5
Power(mW)(Sim/Measured) Divide-by-2 mode	1.88/1.92	1.63/2.2	0.82/0.97
Power(mW)(Sim/Measured) Divide-by-3 mode	2.18/2.26	1.85/2.62	1.61/1.78

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Table II
Device Performance

Reference	[9]	[6]	Proposed
Process(µm)	0.18	0.25	0.18
Supply Voltage(V)	1.0	1.8	1.8
Frequency Range (GHz)	2.4-2.7/5.14-5.7	5.14-5.7	2.4-2.484/5-5.825
Resolution(MHz)	9.375/20	20	1,2,5,10,20
Power(mW)	2.7	6.25	0.9602.2

V. CONCLUSION

In this paper demonstrated that pass transistor logic system has considerable implementation. It is proposed for power reduction. The operations of Multimodulus pre-scalar are according to their modes of operation. Here the input frequencies are divided into multiple ranges while the power consumption is reduced. A Multimodulus pre-scalar is verified and multiband flexible divider is verified in [14] . In this project provides solution to the low power, PLL synthesizer is implemented. The proposed multiband flexible divider consumes power 52 mw.

In future work, we are going to reduce the power consumptions and achieve maximum operating frequency and also reducing the complexity of the circuits using pass transistor logic. Since the Multimodulus 32/33/47/48 pre-scalar has maximum operating frequency of 6.2 GHz, the values of P- and S-counters can actually be programmed to divide over the whole range of frequencies from 1 to 6.2 GHz with finest resolution of 1 MHz and variable channel spacing. However, since interest lies in the 2.3- and 5–5.725-GHz bands of operation, the P- and S-counters are programmed accordingly.

The Proposed multiband flexible divider also uses an improved loadable bit-cell for Swallow S-counter and consumes a power of 0.96 and 2.2 mw in 2.3- and 5-GHz bands, respectively, and provides a solution to the low power PLL synthesizers for Bluetooth, Zigbee, Network standards 802.15.4, and 802.11a/b/g Wireless LAN applications with variable channel spacing.

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