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A Review on Extended Golay Encoder and Decoder Design

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ABSTRACT*:* An proficient implementation in the area of field programmable gate array (FPGA) by using both binary Golay code (G_{23}) and extended binary Golay (G_{24}) can be performed with the help of number of encoding scheme such as block code, Turbo codes, Hamming code, CRC-cyclic redundancy check-based etc. High speed with less complexity and low-latency architecture is the main concern area when working on FPGA. To avoid the complexity and for the accomplishment of the need of the system this paper present a review on number of scholars and on the bases of that a new scheme is proposed in future for FPGA using both binary Golay code (G_{23}) and extended binary Golay (G_{24}).

KEYWORDS: FPGA, CRC cyclic redundancy check, Golay code, Extended Golay code, Encoding, Decoding, Hardware optimization.

I. INTRODUCTION

In communication system which is wireless in nature the signal travel in the atmosphere will be scattered, reflected, diffracted and refracted because of the difficulty introduced by the obstacle presents in the atmosphere which simply defines the system is in a non-Line-of-sight (NLOS) environment. On the other hand when passing through different environment of atmosphere the signal gets distorted and there may be error present in the information. So the main area to work is to reduce the error probability of digital signal in real time communication system. The distortions that are introduced here is due to the noise that are received at the time of transmission and multipath interference. To overcome this problem channel coding technology is better option. In view of the fact that this technology must add some extra bits to the original data at the time of transmission the channel coding must add extra bits to the original data called parity bit or redundant bits, as a consequence of that we can detect and correct the error bits of signal. By appending the additional bit to the data as parity energy of the symbol gets reduces of the received signal as an effect of that receivers symbol error rate increase. Although more error bits can be corrected to compensate for the symbol error rate that increases by the decreasing the energy of the symbol, the bit error rate of the entire received signal still can be reduced. By dropping the power efficiency Eb/N0 of the received digital signal after decoding will be the condition for achieving the same bit error rate.

By avoiding more number of addition parity bits we can receive reduced symbol error rate of the received signal. To achieve this we have to set threshold value of signal to noise ratio and to achieve the coding gain, this the signal-to-noise (SNR) of the received signal Eb/N0 should reach to that threshold. The decoding mechanism is not accountable for this reduction in the symbol rate and cannot reimburse for this loss. As a result, the selection of coding rate is very important; or we can say that for every system having its unique specification requirement for different encoding modes and different coding rates should be adopted. The decoding ability of the channel code is affected by the coding rate that determined by the number of information bits and parity bits.

In a wireless communication channel the coding environment for the technology used improve the bit error rate of signal in transmission. To accomplish the lower bit rate at the same transmission power the bandwidth is customized the excess part of the bandwidth is taken out. On the other hand, the quality required for the communication can be received at lower transmitted power; though we achieve the coding gain of the channel code. These can be satisfied only when we achieved the Eb/N0 threshold of received signal are reached. The most common problem in wireless

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channel environment is the noise and interference from different environments, obstacles and user moving. Accordingly, problems in coding is encountered due to the event encountered of the burst errors to solve this problem block interleaving is one of the most suitable method to break up the burst error in to discontinuous random error to bring the ability of channel coding to correct errors. One more difficulty encountered at the time of coding and decoding that appending of more redundant bits increases the system complexity and the need of storing that bits is also become complicated for the large memory, complex buffers, software and hardware design is become very complicated. One of the best possible ways to present the coder and decoder and a new advance way to remove the errors is use Golay code to encrypt the data the main idea of using this code is to controlled the amount of errors as much as possible. For that additional bits were appended to the messages is one of the best idea by which facilitate to find out or correct the errors that may have occurred. This paper presents a specific type of error-correcting codes, Golay codes (23) and the extended Golay code (G24). Three steps to transfer the data, a channel transmit, and a receiver. At the time of transmission the data is changed to noise so to avoid this condition use error correction codes.

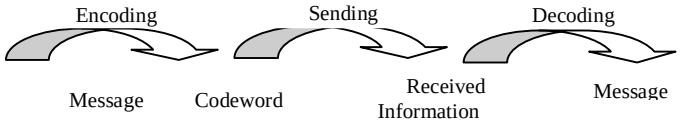

Fig: 1 Message Encoder

Fig. 1 show that a message is encoded into a codeword by appending extra bits, and that codeword it is sent to the receiver through a channel, And during the transmission process the possibility of introducing an error increases, and the receiver want to obtain the original message by decoding the word. The transmission of message depends on what we have received and what is send. Some important properties that give a complete description of the extended Golay are described as follows:

Data (12-bit)	Appended zeros	Operation
101000100111	00000000000	
101011100011		. 12-bit xor
000011000100	0000	. 1-bit shift
10101110	0011	. 12-bit xor
01101010	00110	. 1-bit shift
1010111	00011	. 12-bit xor
0111101	001010	. 1-bit shift
101011	100011	. 12-bit xor
010110	1010010	. 1-bit shift
10101	1100011	. 12-bit xor
00011	0110001000	. 1-bit shift
10	1011100011	. 12-bit xor
01	11011010110	. 1-bit shift
1	01011100011	. 12-bit xor
0	10000110101	
	<Check-bits>	

Fig 2 Long Division of Data for Check bits generation

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1) First property shows that a message m of length k out of some finite field F generates sequence of k symbols, so m = (m1: mk) belongs to F^k. Then an n-code Cover a finite field F is a set of vectors in F^n, where $n \leq k$. Since we will be commerce with a binary code only.

2) Second property defines that the error of p probability introduced only when 0 is received in place 1that was send by the sender was sent, or 1 is received when 0 was sent.

3) Third property says that the function F^n is a non-zero elements and hamming weight of a vector belongs to that function.

4) Fourth property says that the humming distance of two vectors is part of function F^n is the number of place where they differ. The scheme is that an n-code C is a strict subset of F^n in which we expect the Hamming distance between any two vectors to be as large as possible. As a result, the minimum Hamming distance is a main characteristic of the code.

5) Fifth property says that the minimum Hamming distance d of a code C is defined as d = min {dist(x, y) I x, y belongs to C} where c is the code.

Golay Code Encoder Algorithm

The Golay code encoding is explained using example in fig. 2

The encoding procedure depends on the following steps that are used for the encoding procedure:

1) Characteristic polynomial is preferred for check bits generation.

2) Long division method is use to contribute 'M' bit data with the characteristic polynomial. So, 11 zeros are added to the right of data message M.

3) The check bits for G (23) are generated by the most significant bit (MSB)obtained at the end of the division operation.

4) The encoded Golay code (23, 12, 7) codeword are generated by adding check bits with the message.

5) For conversion of binary Golay code into extended binary Golay code (24, 12, 8) a parity bit is appended. If the weight of binary Golay code is odd, then parity bit 1 is appended, otherwise 0 is appended.

Golay Code Decoder Algorithm

Steps that are used for the decoding procedure tis enlisted as follows:

1) For the received codeword 'W' and matrix 'H', where H = [I / B] Compute the Syndrome 'S'.

2) Error vector, E = [S, 0], $wt(S) \leq 3$.

3) If $wt(S+Bi) \leq 2$, then E = [S+B*i*, I*i*].

4) In this step second syndrome SB can be computed

5) If $wt(SB) \leq 3$, then E = [0, SB]

6) If $wt(SB+Bi) \leq 2$, then E = [I*i*, S+B*i*]

If E is still not determined then it is required to be retransmitting the data.

The first section presents an introduction about the problem encounter at the time of transmission and the reason why they occur and also give the solution to resolve it to achieve high performance system. The second section presents the literature review that presents the work of others. Third section is conclusion and forth is the last section is about the reference paper.

II. RELATED WORK

In Reference [1] is an IEEE Transaction paper which proposed an efficient hardware implementation based on CRC (Cyclic Redundancy Check) encoding scheme to encoder and decoder for both prototype binary Golay code (G23), extended binary Golay code (G24).Virtex-4 FPGA is used to design high speed with low latency architecture. This paper also gives a short review for various applications in the field of high speed communication links, ultrasonography and photo spectroscopy. Reference [2] is a paper written by Mr. Golay himself. This paper presents lossless binary coding scheme to declare the reception of the correct data. This paper also gives the solution to the problem of power loss which is introduced by ternary coding scheme, and this can be achieved by a 23 binary symbols which yields the power saving one and a half db to reduce the probability of errors and this code is called Golay code. And another code is also introduced by him called extended Golay code but it is not that much efficient in terms of power it yields the power saving up to 3 db.

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Reference [3] this paper presents a hard decision decoding to outperformance the extended Golay code. And compare the performance of the binary Golay code and extended binary Golay code under the ML (maximum likelihood) conditions. Reference [4] presents the overview about the Golay codes and their properties. This paper also gives the comparative study of (G11) is ternary Golay code and (G23) binary cyclic code. Reference [5] presents GF (2m) Galois field encoder & decoder and its implementation on FPGA using the NIST chosen irreducible polynomial. Software used to do this is Xilinx ModelSim 10.0 that simulated complete verification of multiplication & implemented on FPGA. The paper proposed a simple circuit and performs high speed operation by increases protection during communication dialogue and decreasing the number of logic gates. Reference [6] proposed an algorithm depends on simplified soft decoding that is used to correct up to four errors for extended binary Golay code .The results achieved by this process shows the less complex calculation were required with this method and also work on the efficiency hardware implementation on FPGA platform. This paper also presents the detailed architecture of soft decoder and also gives the comparative study with the other algorithms in terms of power, cost, gain, and hardware complexity. Reference [7] proposed a method to build a concept of the binary Golay code (24, 12, 8) by using two array codes involving four component codes. Two of them are symmetric code and its extended version and two are simple linear block codes.

Reference [8] presents review on Golay Complementary Sequence. These sequences are introduced by Marcel Golay in the perspective of infrared spectrometry and also give the properties and applications in different fields. Reference [9] proposed a new algorithm that algorithm is used to decode the binary systematic (23, 12, 7) and (14, 21, 9) QR codes. The proposed method by using lookup table directly determines the error locations without the operation of multiplication over a finite field. The explanation why this paper presents the use of FLTD because with this CPU time is half of the LTD algorithm. In terms of both speed and memory need in real time system FLTD algorithm is better approach as compare to the existing ones. Reference [10] proposed a symbol –by –symbol soft in/ soft out APP decoding algorithm for the Golay code. This decoding algorithm is appropriate for convolution codes and block code with simple trellis structure.

Reference [11] proposed block product turbo code (BPTC) and simulated its efficiency. The proposed method used hamming (15, 11), hamming (13,9) and block channel code in combination with the construct a BPSK modulation . With this combination obtain results are better and robust against BPSK Golay code and MSK Golay. Application based on proposed algorithm is in the wireless communication system. Reference [12] proposed scheme which is just opposite to the conventional Golay code (24, 12, 8) which maps 24- bit vector into 12 bits message words. In this method each information is represented by 24 bit vector at the same time we consider 1 bit probability distortion through bit modification. As a result, this work proposed a hash table of 4096 entries that is fault-tolerant. This allows organizing a direct recovery of a neighbourhood of 24-bit vectors with two or possibly more mismatches. A recovery capability of the proposed system and the expected hash distribution is achieved by the simulation experiments. Reference [13] proposed a methodology of constructing a sequence of phase-coded waveform for which ambiguity function is free of ranges side lobes along doper shift. The problem introduced with Golay code is that it has ideal ambiguity along zero Doppler-axis but is very much responsive to nonzero Doppler shifts. And the application of pulse coded waveform is communication using radar.

Reference [14] proposed an error correction Golay code for clustering large amount of Big data Streams by using error correction Golay codes and this approach is applicable in the field where the requirement to accumulate multidimensional data. In Reference [15] the proposed methodology in combination with the special Fractional Fourier Transform (FRFT) to fulfill the requirement reducing the peak to average ratio (PTAR). This can be achieve to obtain low complicity Golay sequence coder in order to provide optimal de-correlation between signal and noise. Reference [16] proposed an algorithm based on FPGA for the hardware implementation of (24, 12, 8) Golay code. To overcome the complexity of arithmetic operations this arises in the existing algorithm. The proposed algorithm chooses the absolute value in place of bit error probability to obtained better results as compared to the existing algorithms. Reference [17] proposes a method to fulfill the requirement of faster responsive decoding for the Gosset Lattice, Leech Lattice and Golay code. The proposed design introduced two different method to first when charge in of length n and taking soft decoding algorithm at an arbitrary point R^n in to the adjacent code word and second a decoding algorithm for a lattice A in R^n changes an arbitral point of R^n into a neighbouring lattice point.

Reference [18] proposed an efficient soft-decision decoder of the (23, 12, 7) binary Golay code up to the four errors and nearly all patterns of three errors and all fewer random error can be corrected with the help of proposed algorithm.

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III. CONCLUSION AND FUTURE WORK

This paper presents a review on different research work presented in the field FPGA based speed optimization bust error reduction etc. Different coding and decoding methods were introduced in the reference papers to control the errors and for the speed optimization. Here, the main aim is to present systems which remove the complexity of system on fulfillment the requirement of high speed application and low latency data. So that a new scheme is proposed in future for FPGA using both binary Golay code (G_{23}) and extended binary Golay (G_{24}).

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