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Design and Analysis of Multiplexer in Different Low Power Techniques

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ABSTRACT: With more devices becoming portable and battery operated, the power dissipation in a device is increasingly becoming important. At the same time with technology changing, the number of transistors in a chip is also increasing at a rapid rate. With more number of transistors in a given area, the power dissipation in the form of heat becomes more. Adiabatic circuits are low power circuits where the power dissipation is very less compared to standard CMOS. Adiabatic logic circuits use energy recovery to minimize power dissipation. The present paper discusses the design of Multiplexer in different Adiabatic Logic circuits and proposed CMOS based design. All the simulation is done using Tanner EDA Toolv15.0 at 180nm technology and frequency at 200MHz.

KEYWORDS: Adiabatic Logic, Multiplexer, Low Power, Tanner Tool, CMOS, Low Power VLSI, PFAL, ECRL.

I. INTRODUCTION

Power dissipation is increasingly becoming a concern nowadays as the computing power is increased and the number of transistors switching has also increased. With more power dissipated in the form of heat, different cooling techniques have to be adopted. The ever famous logic for implementing different functions is CMOS logic. CMOS is known for its low static power consumption. The problem with CMOS is it has very large switching power consumption, which directly depends upon the switching frequency. The power dissipation in CMOS is given as

$$P_{total} = P_{static} + P_{dynamic}$$
$$P_{dynamic} = C_L V_{dd}^2 f_{clk}$$

P_{static} is the static power dissipation of CMOS which constitutes leakage power and short circuit power, which is very less compared to other logic circuits. $P_{dynamic}$ is the dynamic power dissipation which depends on the switching rate f_{clk}, combined load capacitance C_L and proportional to square of supply voltage V_{dd}. The usual practices to reduce power dissipation in CMOS is to reduce V_{dd}, but it reduces the performance of the circuit. C_L is a technology parameter and it also depends on device intrinsic capacitances. In CMOS the total energy taken from the supply is given as $C_L V_{dd}^2$, in that half is dissipated in transistors and the other half is stored in capacitors. The lower bound of energy dissipation in CMOS is $\frac{1}{2}C_L V_{dd}^2$[7].

II. RELATED WORK

In [1] authors have designed adiabatic multiplexer and demultiplexer in 500nm technology, which is considered an older technology in current VLSI trends. Current VLSI trend in India is 180nm and 250nm, as in India only fabrication plants supporting the later mentioned technologies are present. With technology shrinking, the circuit area is reduced and many number of circuits can be incorporated in a given area. But the downside is larger power dissipation as we will see at the end, power dissipation compared to [1] is more. In [3], [4] and [5] the author has designed different digital logic gates in ECRL, PFAL and 2N2N2P and compared the power dissipation. In [8] the authors have designed a 4x1 multiplexer and demultiplexer using PFAL and ECRL logic and compared the power outputs.

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III. ADIABATIC LOGIC CIRCUITS

Adiabatic logic circuits are primarily used in low power VLSI circuits. They are also called as "reversible logic" because the energy taken from the supply for logic implementation is again given back to the supply. The adiabatic term is taken from thermodynamics, which means "no exchange of heat/energy". Adiabatic logic circuits are charged in a constant current charging i.e. with linear voltage charging a resistor (ON resistance of a transistor). In this way uniform charge is transferred to the load and we will see that, the larger the duration of linear voltage (less slope) the larger the power saving [2].

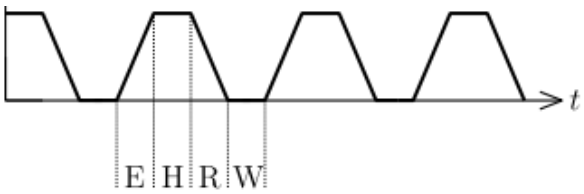

Fig. 1. Trapezoidal Power Clock

This is the reason we use a trapezoidal power clock instead of constant supply voltage. The trapezoidal voltage has four intervals, evaluate (E) interval where the outputs are evaluated, hold (H) where the stable outputs are transferred to the next stage, recover (R) where the supplied energy is recovered back and wait (W) is wait interval for symmetry property as symmetrical signals are comparatively easy to generate. The power clock is shown in Fig. 1. The circuit implementation of power clock is a major drawback of adiabatic circuits. Adiabatic circuits are classified as fully adiabatic and partially adiabatic circuits. In fully adiabatic circuitsthe adiabatic loss is not present and total energy is recovered back. In fully adiabatic logic the number of transistors required are more i.e. they are more complex. Partially adiabatic circuits are in which there is an adiabatic loss which is proportional to switching speed. Partially adiabatic circuits are ECRL, PFALand 2n2n2p circuits [2].

A. *Efficient Charge Recovery Logic (ECRL):*

ECRL is proposed by Moon and Jeong [3], this logic uses two cross coupled PMOS transistors to store the logic value. The function is computed by the NMOS tree in the pull-down. It uses differential signaling. There is a non-adiabatic loss present in ECRL which is given as $\frac{1}{2}C_L|V_{thp}|^2$ due to threshold voltage required to ON the PMOS transistors. This loss is independent of frequency and is a constant offset present at all times [3].

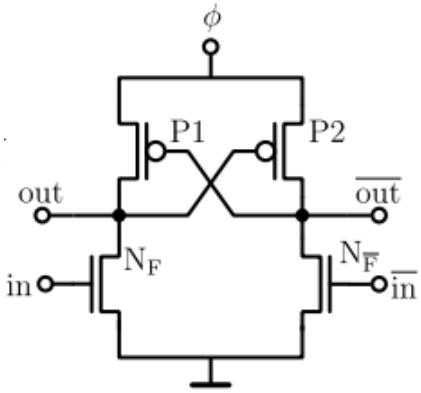

Fig. 2. ECRL Buffer/Inverter Schematic

B. *Positive Feedback Adiabatic Logic (PFAL):*

PFAL logic has two CMOS inverters connected back to back as a latching element i.e. to store the logic value. It has two NMOS trees connected in parallel to the PMOS pull-up. The other difference between ECRL and PFAL is that no output is left floating at any time because of the two cross coupled CMOS inverters. The outputs are differential as well [4].PFAL has the least power dissipation compared to other adiabatic logic circuits. It requires two extra transistors when compared to ECRL.

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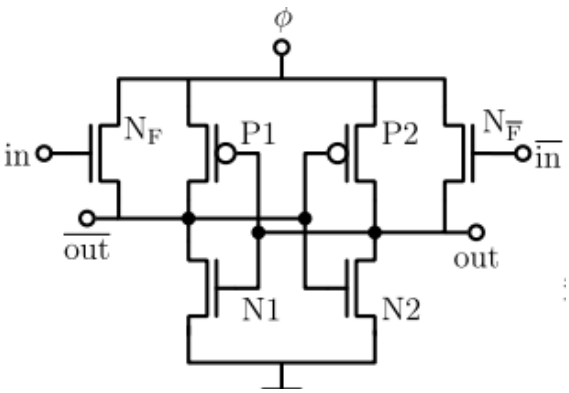

Fig. 3. PFAL Buffer/Inverter Schematic

C. *2N2N2P:*

It is similar to PFAL with two CMOS inverters connected back to back as a latch but the difference is in the NMOS logic block which is connected parallel to NMOS pull-down rather than PMOS pull-up. This logic circuits also has non-floating and differential outputs [5].

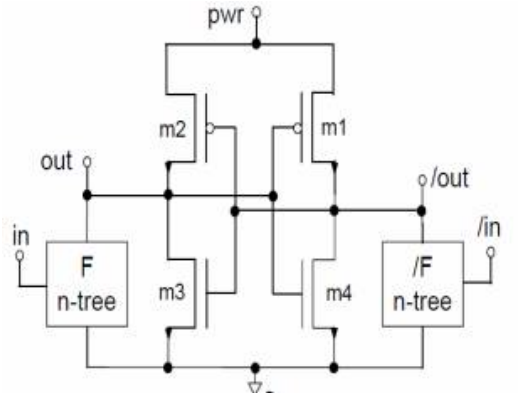

Fig. 4. 2N2N2P Schematic

IV. MULTIPLEXER DESIGN

Multiplexers are called data selectors. It has 2^n inputs, n selection inputs and 1 output. Multiplexers in digital electronics are used to implement combinational functions. In communications, it is used to multiplex different signals into a single channel. In this paper we consider an 8x1 multiplexer, which has 8 inputs, 3 selection inputs and 1 output.

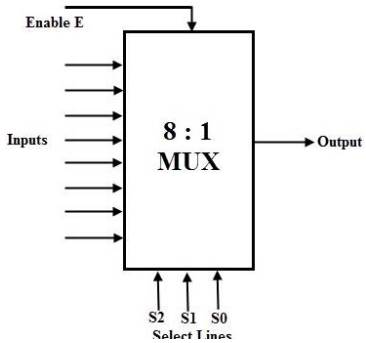

Fig. 5. 8x1 Multiplexer

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V. PROPOSED DESIGN

The proposed logic is based on CMOS logic with extra two transistors, one PMOS in pull-up and one NMOS in pull-down. This logic also uses power clock with four phases. The inverter circuit in the proposed logic is shown in Fig. 6 [1].

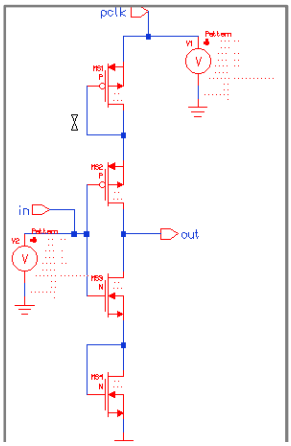

Fig. 6. Proposed Logic Inverter Schematic

- The two extra transistors are biased in saturation region as their gate and drain are shorted.

VI. CIRCUITS AND SIMULATION

All schematics are done using Tanner Tool EDA v15 and simulation is done using T-Spice. Technology is 180nm.

A. *ECRL (8x1 Multiplexer):*

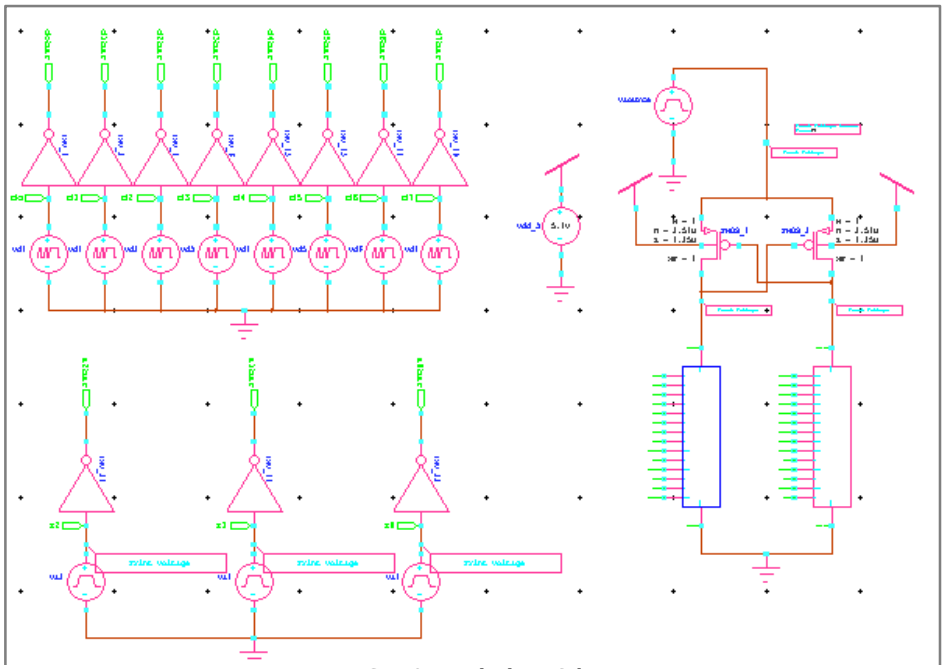

Fig. 7. ECRL 8x1 Multiplexer Schematic

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- The NMOS pull-down used for implementing the required logic is shown as a block. The required inputs and its complements are shown in the left part of the figure.
- The outputs are obtained by given the required selection inputs. Depending on the selection inputs a particular input is selected. The outputs are complementary.

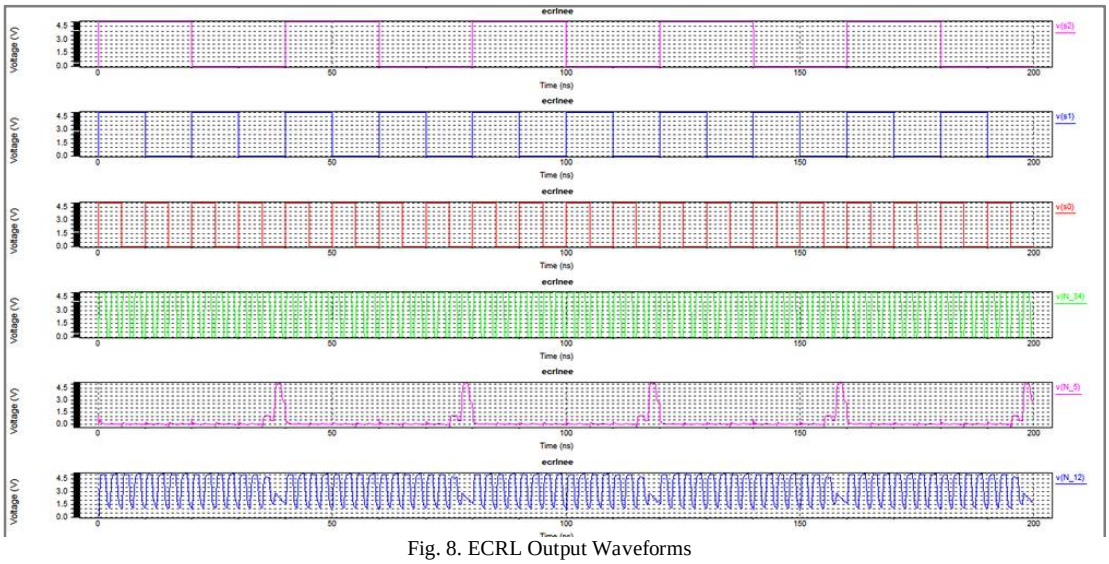

Fig. 8. ECRL Output Waveforms

B. *PFAL (8x1 Multiplexer):*

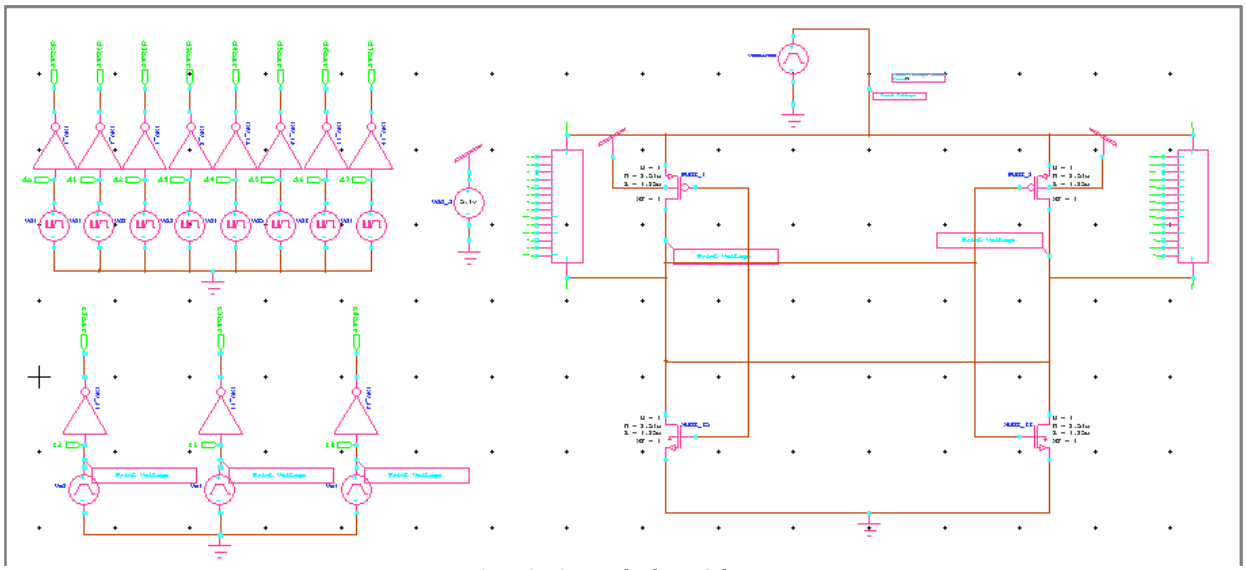

Fig. 9. PFAL 8x1 Multiplexer Schematic

- The NMOS logic implementing block is parallel to the pull-up PMOS devices. The inputs are shown in the left portion of the figure. The outputs are also complementary. The multiplexer output is shown at the end plot, it is high only according to the input combination. First three plots are the selection inputs, the next is power clock and rest are out and its complemented output.

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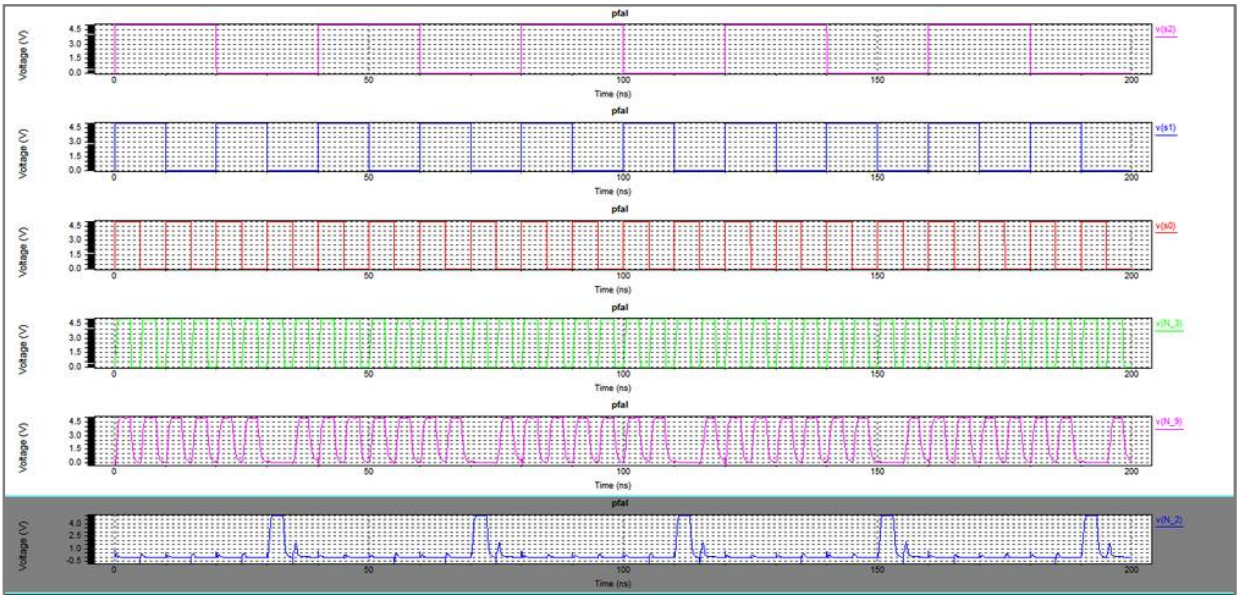

Fig. 10. PFAL Output Waveforms

C. *2N2N2P (8x1 Multiplexer):*

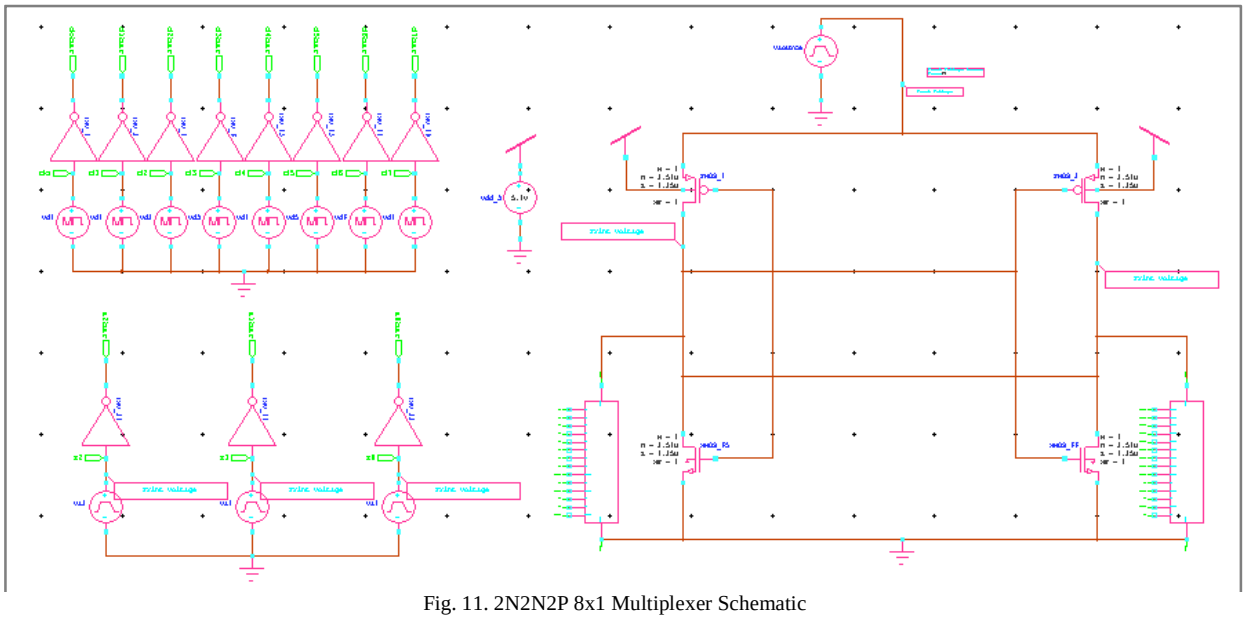

Fig. 11. 2N2N2P 8x1 Multiplexer Schematic

- The 2n2n2p schematic is shown in the above figure. Here the NMOS logic block is kept parallel to the pull-down NMOS transistors. The outputs are complementary and are shown below. The first three plots are selection inputs, next is power clock and the other two are output and its complement. Depending on the selection input combination, output is evaluated.

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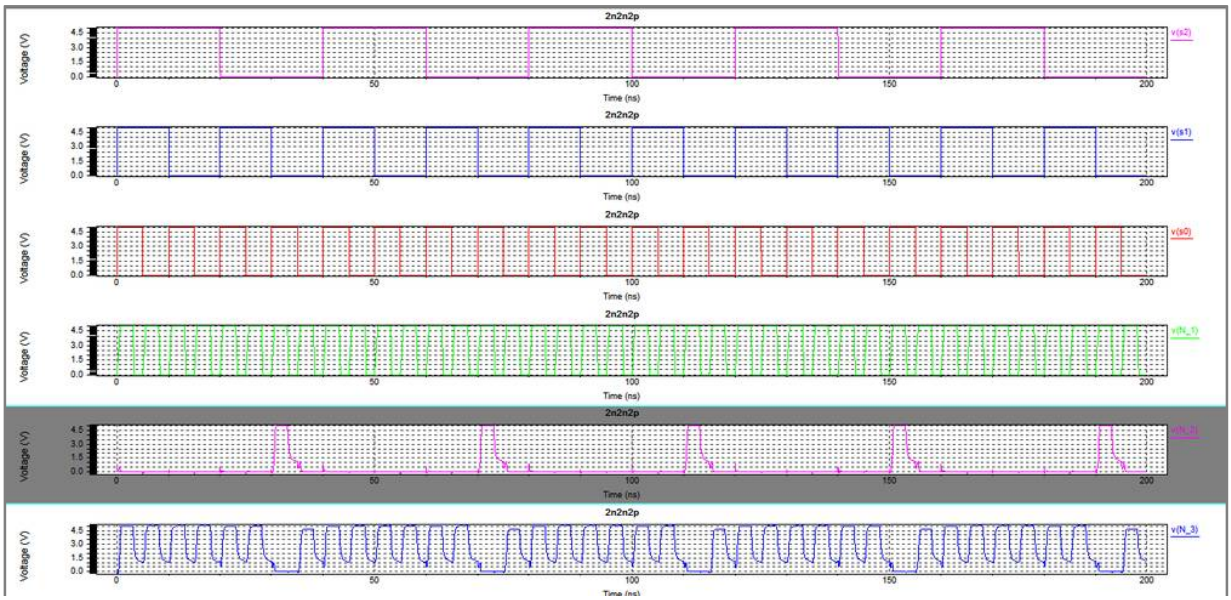

Fig. 12. 2N2N2P Output Waveforms

D. *Proposed Logic Circuit (8x1 Multiplexer):*

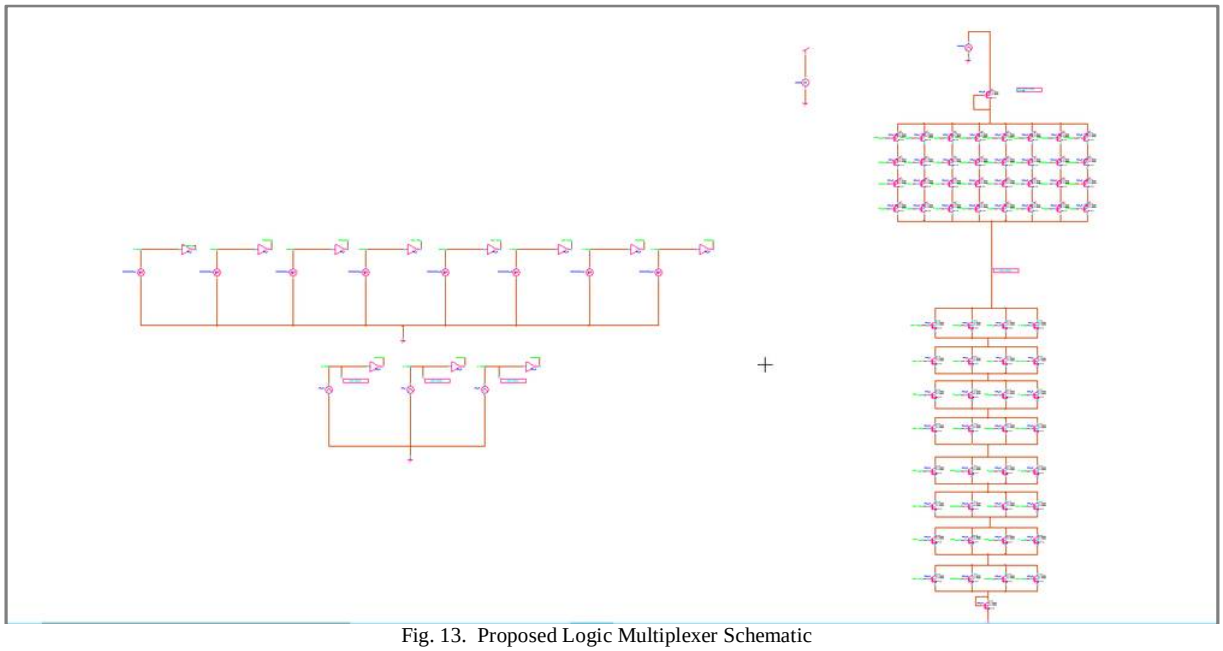

Fig. 13. Proposed Logic Multiplexer Schematic

- In the proposed logic circuit, it is similar to CMOS circuit except it uses two extra transistors. One NMOS in pull-down and one PMOS in pull-up both operating in saturation. Instead of constant supply voltage, a power clock is used.
- The proposed logic multiplexer is shown above. Here the inputs are shown in the left portion of the figure. The outputs are not complementary [1].

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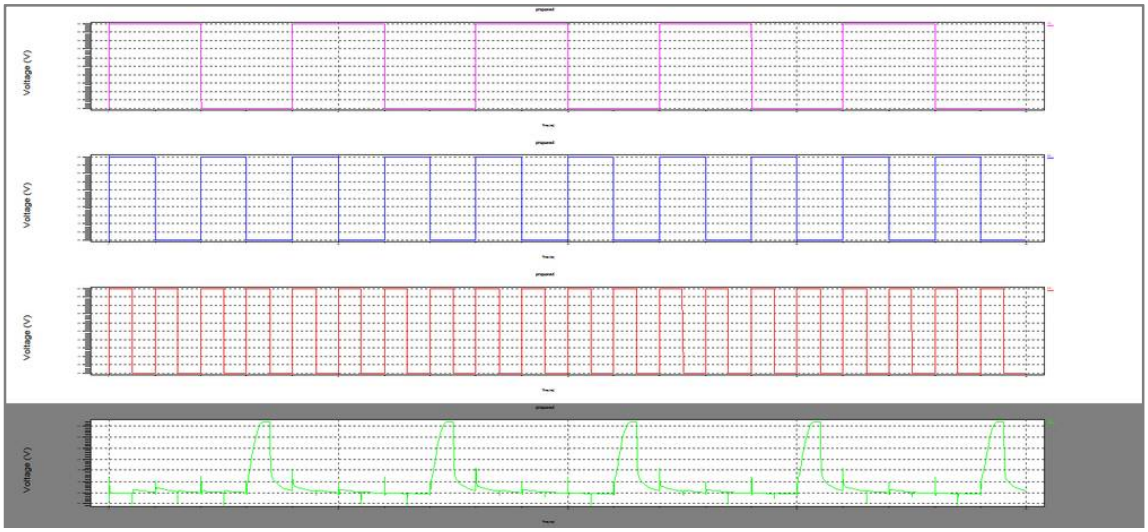

Fig. 14. Proposed Logic Output Waveforms

E. *Power outputs:*

F.

Table 1. Power Output Summary of 8x1 Multiplexer at 180nm

Different Logic Styles	CMOS	ECRL	PFAL	2N2N2P	PROPOSED
Average Power (µW) at 200MHz	483	303	248	371	104

VII. CONCLUSION

All the simulation is done using Tanner Tool EDA v15. Technology used is 180nm. The frequency of signal used is 200 MHz. 8x1 Multiplexer is designed using all the standard adiabatic logic styles, CMOS and the proposed logic style. Power dissipation for the proposed circuit is at 104µW compared to 483µW of CMOS, which is comparatively very less. To be noted this is the average power and not the peak power. When compared to other outputs also, the proposed logic circuit offers least power dissipation compared to others.

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